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A 850 μm^2 low-power Smart Temperature Sensor for IoT Applications

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ABSTRACT

This work presents a fully integrated, self-clocked temperature-to-digital converter-based smart temperature sensor for on chip thermal monitoring of Near threshold sensor node processors. The design utilizes the MOSFET sensing followed by a time-to-digital converter (TDC). The sensing methodology involves measuring temperature by comparing the output frequencies of two ring oscillators engineered with distinct temperature responses, without having an external reference. At a CMOS process of 65-nm and supply voltage of 0.5 V, the sensor occupies a small area of 850 μm^2. The power consumption of the proposed circuit is 5.5 μW. The sensor attains a resolution of 0.06℃ over the temperature range of -40°C to 125°C and limits the inaccuracy between +1.8℃ to -3.5℃ after one-point calibration with polynominal correction. Moreover, the experimental results from the proposed design achieves an energy per conversion of 0.133 nJ with a resolution figure of merit (R-FoM) of 0.46 $pJ.K^2$ at typical process corner.

Introduction

The increasing complexity and power density of system-on-chip (SoC) designs have led to significant thermal challenges, making effective on-chip temperature monitoring essential for reliable operation. Excessive temperature gradients and localized hot-spots can degrade performance, accelerate device aging, and potentially cause permanent damage, necessitating efficient thermal management strategies based on accurate temperature sensing. Traditional temperature sensing solutions are based on standalone components such as thermistors, thermocouples, and infrared sensors, commonly referred to as discrete temperature sensors. Although these sensors can offer high accuracy and wide operating temperature ranges, their reliance on external components limits system integration and increases cost, making them less suitable for highly integrated applications.

In advanced high-speed integrated systems, the widespread deployment of on-chip temperature sensors as shown in Fig.1 enables real-time detection of localized hotspots, thereby improving system robustness and preventing thermal overstress. For such applications, minimizing silicon area and energy consumption is critical to allow dense integration of temperature sensors with minimal overhead. Sensors that employ on-chip passive components, such as resistors, have been introduced due to their ability to function at very low supply voltages and their compatibility with a wide range of process technologies[1,2,3]. However, resistor-based temperature sensors generally require larger area and exhibit higher power consumption. Similarly, BJT-based temperature sensors are also limited by increased power consumption, sensitivity to process variations, larger silicon footprint, and poor scalability in modern CMOS processes[4,5,6,7,8]. As a result, integrated temperature sensing solutions implemented in standard CMOS technology have attracted significant research interest. CMOS devices inherently exhibit temperature-dependent electrical characteristics, which can be exploited to realize compact on-chip temperature sensors without additional external components. This approach enhances integration density, reduces board-level complexity, and lowers overall system cost, while offering scalability, compatibility with digital CMOS processes, and favorable yield characteristics[12,13,14].

Beyond their traditional role in thermal management for processors and large-scale SoCs, CMOS temperature sensors are increasingly employed in wireless sensor networks and Internet-of-Things (IoT) end devices. In these energy-constrained applications, sensor nodes are often powered by small batteries or energy-harvesting sources, making ultra-low-power operation a primary design objective. To extend system lifetime, many IoT sensor nodes operate at reduced supply voltages, including near-threshold voltage (NTV) regimes[9,10,11]. Operation at near-threshold voltage exposes temperature sensitivity as a first-order design constraint, fundamentally limiting the robustness and energy efficiency of low-power circuits unless explicitly addressed at the sensor and circuit levels. At such reduced supply voltages, small temperature variations induce disproportionate changes in transistor delay, leakage current, and noise margins. These effects severely restrict voltage scaling and timing robustness in energy-constrained IoT wireless sensor nodes. Consequently, temperature sensors designed to operate reliably at near-threshold

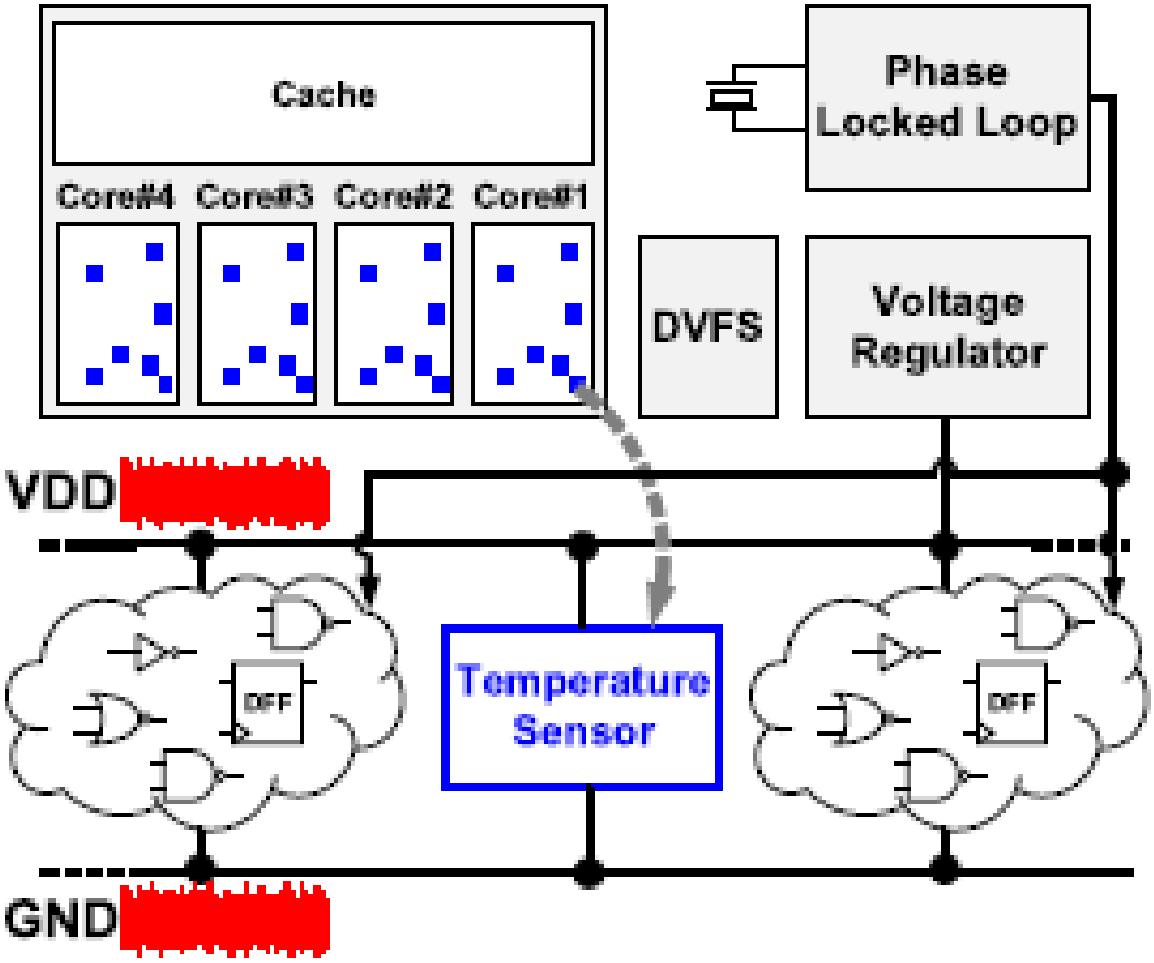


Figure 1. Embedded temperature sensor in a wireless sensor network[23].

voltages play a critical role in enabling closed-loop adaptive voltage and frequency scaling as well as leakage-aware power management. By minimizing sensor overhead while providing accurate thermal feedback, near-threshold temperature sensing becomes a key circuit-level enabler for reliable ultra-low-energy system design.

In this work, we propose a compact and low-power CMOS temperature sensor operating at near-threshold voltage, targeting battery-powered wireless sensor network and IoT applications. The proposed architecture consists of two main functional blocks: a temperature sensing block and a temperature quantization block. The temperature sensing block employs two ring oscillators intentionally designed with different temperature sensitivities to generate temperature-dependent frequency outputs, while the temperature quantization block converts these frequencies into a digitally encoded temperature value using a time-to-digital conversion (TDC) scheme. All sub-systems are carefully redesigned and optimized for near-threshold operation to ensure reliable sensing performance under tight energy and voltage constraints, making the proposed sensor well suited for energy-efficient and densely integrated IoT sensor nodes.

The remainder of this brief is presented in the following sections. Section II describes the working principle and circuit implementation of the proposed design. Section III explains temperature sensor architecture in detail. Section IV presents the results and observations, and section V concludes the brief.

1 PRINCIPLE OF OPERATION OF THE PROPOSED SENSOR

The proposed sensor determines temperature by monitoring the oscillation frequencies of two distinct ring oscillators used as sensing elements, each exhibiting a different sensitivity to temperature changes. The digitized ratio of these two frequencies corresponds to the measured temperature. In CMOS ring oscillators, temperature variations influence the oscillation frequency primarily through changes in carrier mobility and threshold voltage. The temperature co-efficient of carrier mobility and

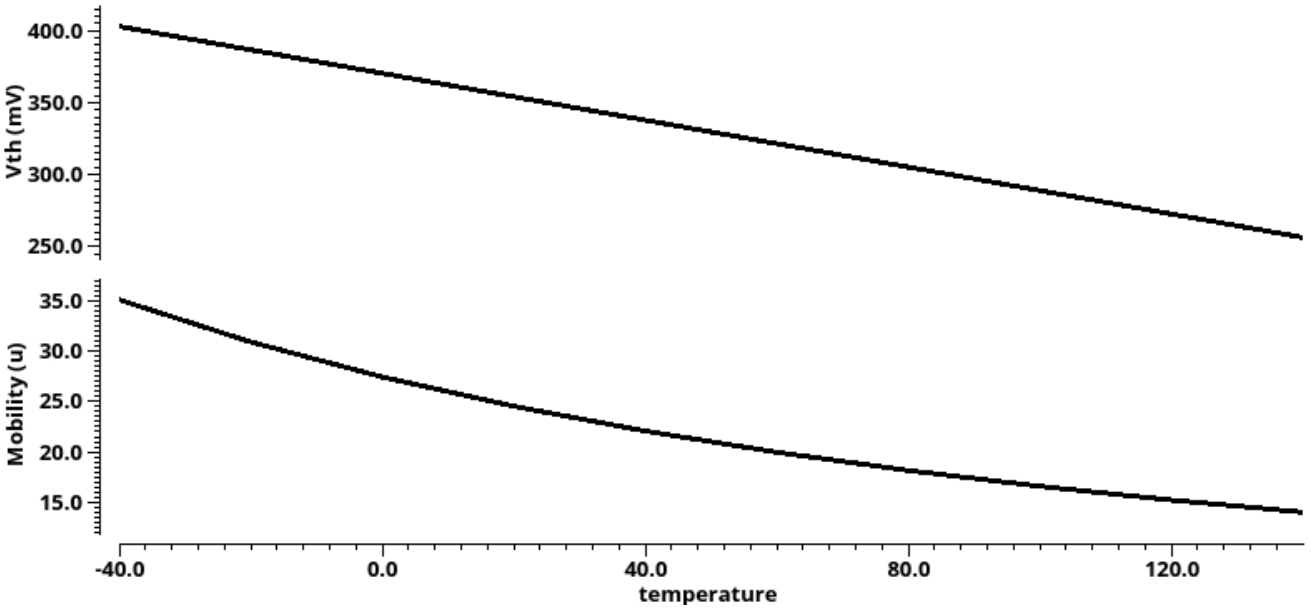


Figure 2. Mobility and threshold voltage variation with temperature for nmos device.

threshold voltage in CMOS devices is modeled as follows:

$$\mu \propto \mu_0 \left(\frac{T}{T_0}\right)^{-p} \tag{1}$$

$$V_{TH} = V_{TH0} - k(T - T_0) \tag{2}$$

where p is an empirical fitting parameter, typically in the range of 1.2–2.0. The parameter μ_0 denotes the carrier mobility at the reference temperature T_0, and V_{TH0} represents the threshold voltage at the reference temperature. The coefficient k, which characterizes the temperature sensitivity of the threshold voltage, generally lies between 1 and 3 mV/°C. Fig.2 shows the mobility and threshold voltage variations with temperature for an nmos device. These temperature-dependent variations in mobility and threshold voltage directly impact the delay characteristics of CMOS inverters and, consequently, the oscillation frequency of CMOS ring oscillators. As a result, ring oscillator–based sensors can exploit these dependencies to achieve reliable temperature sensing. The temperature sensitivity of an oscillator can be adjusted by modifying carrier mobility, threshold voltage, or the supply voltage. However, circuit designers have no control over carrier mobility, and providing multiple supply rails to a sensor embedded deep within a processor is often impractical. Consequently, threshold voltage engineering is a more feasible approach for tuning temperature sensitivity. A threshold voltage difference between two ring oscillators can be realized through several techniques. Common approaches include body biasing of the transistors or the use of multiple transistor flavors, such as high and low threshold-voltage devices along with nominal-threshold transistors. However, body-bias-based implementations typically require additional analog circuitry, including band-gap references and voltage regulators, to generate and buffer the required bias voltages. Similarly, the use of multiple flavors of transistors incurs additional fabrication cost due to the requirement of additional masks during the manufacturing process. To avoid these overheads, the proposed sensor exploits the reverse short-channel effect (RSCE) to introduce a controlled threshold voltage difference between the oscillators, thereby achieving distinct temperature sensitivities without additional analog circuitry or process modifications.

The proposed temperature sensor employs two ring oscillators, denoted as VCO1 and VCO2, each engineered to exhibit a different sensitivity to temperature variations, as illustrated in Fig.3(a). VCO2 is implemented using transistors with comparatively longer channel length than those employed in VCO1; specifically, both the NMOS and PMOS devices in VCO2 possess smaller threshold voltages than their counterparts in VCO1 because of the reverse short-channel effect (RSCE). In the near-threshold voltage (NTV) region, where the supply voltage is comparable to threshold voltage, sensitivity of both VCO1 and VCO2 frequencies are influenced by the interplay between threshold voltage and mobility variations. As temperature increases, the reduction in threshold voltage tends to increase the oscillation frequency, while mobility degradation produces an opposing effect. In VCO2, longer channel length transistors are employed, resulting in lower effective threshold voltage due to

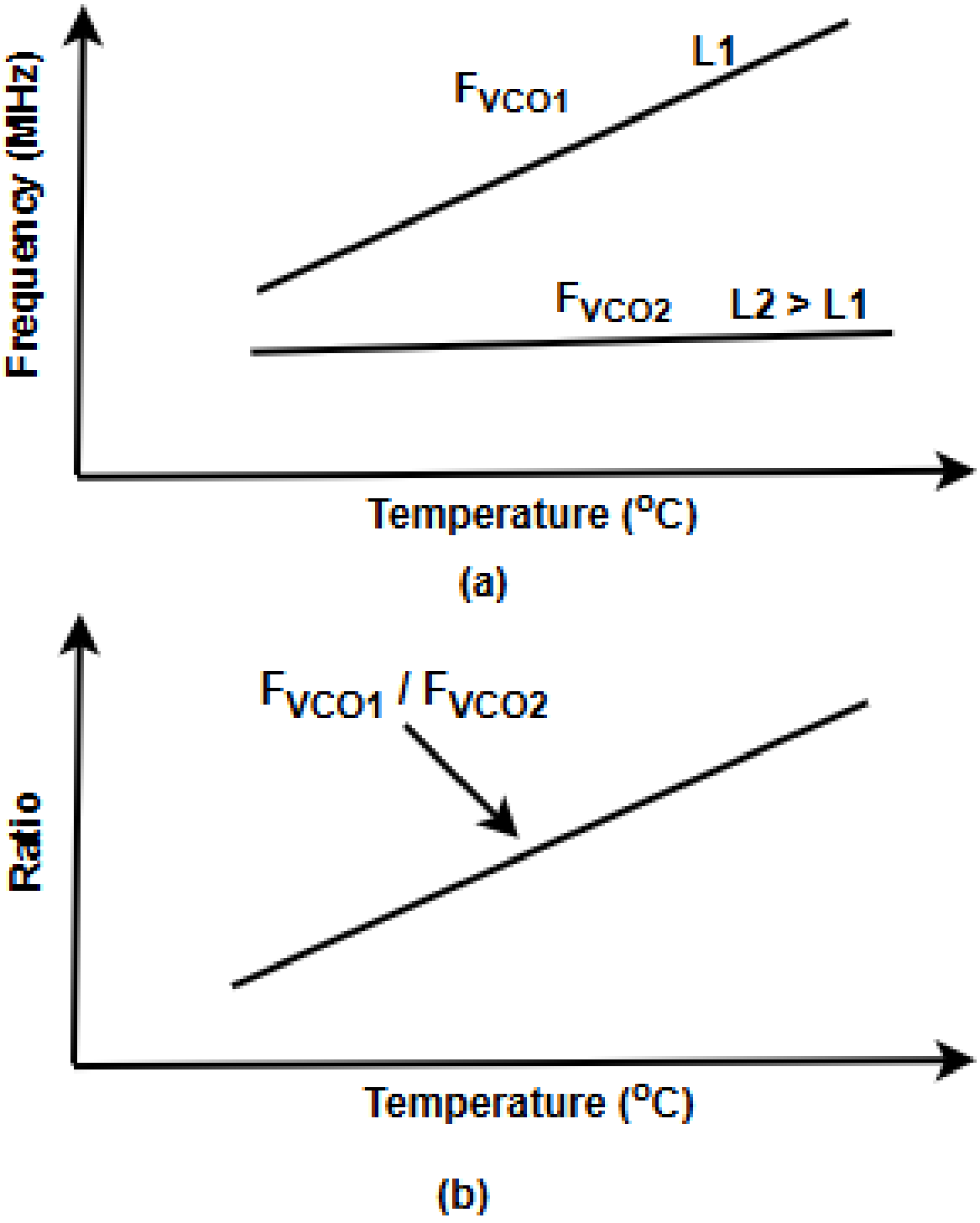


Figure 3. (a) Frequency variation with temperature. (b) Temperature dependence of frequency ratio

reverse short-channel effect (RSCE). This reduction in threshold voltage increases the overdrive margin and shifts the device operation toward a mobility-dominated regime, even under NTV bias conditions. Consequently, the compensating effects of threshold voltage reduction and mobility degradation partially cancel each other, leading to a reduced frequency–temperature slope. This flattened response enables VCO2 to function as a reference oscillator, while VCO1 maintains a stronger temperature

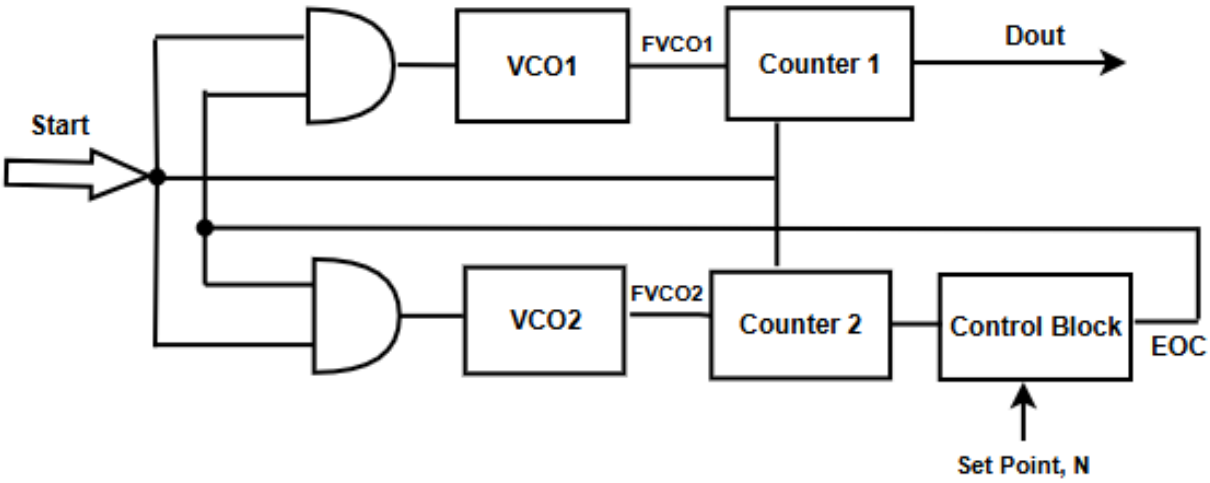


Figure 4. Basic block diagram of the proposed sensor

dependence with a higher positive slope.

The oscillation frequency of a ring oscillator is proportional to the drive current, and is expressed as

$$F_{VCO} \propto \frac{I_D}{C_L V_{DD}} \tag{3}$$

In the nearthreshold voltage (NTV) region, the drain current can be modeled as

$$I_D \propto \mu \left(V_{DD} - V_{TH}\right)^{\alpha} \tag{4}$$

where μ is the carrier mobility, V_{TH} is the threshold voltage, and α is a fitting parameter typically close to unity in the NTV region. Taking the logarithmic derivative of with respect to temperature, the normalized temperature sensitivity can be written as

$$\frac{1}{F_{VCO}}\frac{dF_{VCO}}{dT} \approx \underbrace{\frac{1}{\mu}\frac{d\mu}{dT}}_{\text{mobility contribution}} - \underbrace{\frac{\alpha}{(V_{DD}-V_{TH})}\frac{dV_{TH}}{dT}}_{\text{threshold voltage contribution}} \tag{5}$$

Since $\frac{d\mu}{dT} < 0$ and $\frac{d_{TH}}{dT} < 0$, the mobility term contributes a negative temperature co-efficient, while the threshold term contributes a positive temperature coefficient to the oscillation frequency.

The ratio of the oscillation frequencies of VCO1 and VCO2, defined as (F_{VCO1}/F_{VCO2}), demonstrates the desired PTAT behavior as illustrated in Fig.3(b). This frequency ratio is subsequently digitized to yield a digital output that is directly proportional to temperature. The digitization of frequency ratio is performed using digital logic, without an external frequency source, enabling a fully self-referenced operation.

2 TEMPERATURE SENSOR ARCHITECTURE

The proposed sensing technique aims to implement a sensor architecture exclusively using digital logic gates to achieve compactness, technology scalability, and portability. A simplified block level architecture of the new sensor circuit is shown in Fig.4. It comprises two voltage controlled oscillators (VCOs) followed by a control circuitry and frequency to digital converter using counters. When the start signal is low, the counter is reset. Upon assertion of the start signal, both oscillators will be enabled and start oscillating. The reference oscillator(VCO2) output is fed to counter 2 and once it count reaches a preset count value, the control logic generates the End of Conversion(EOC) signal. Consequently, the enable signal is deasserted, halting the ring oscillators. The output of Counter 1 is latched at this instant, and the final count value is obtained as the digital output code.

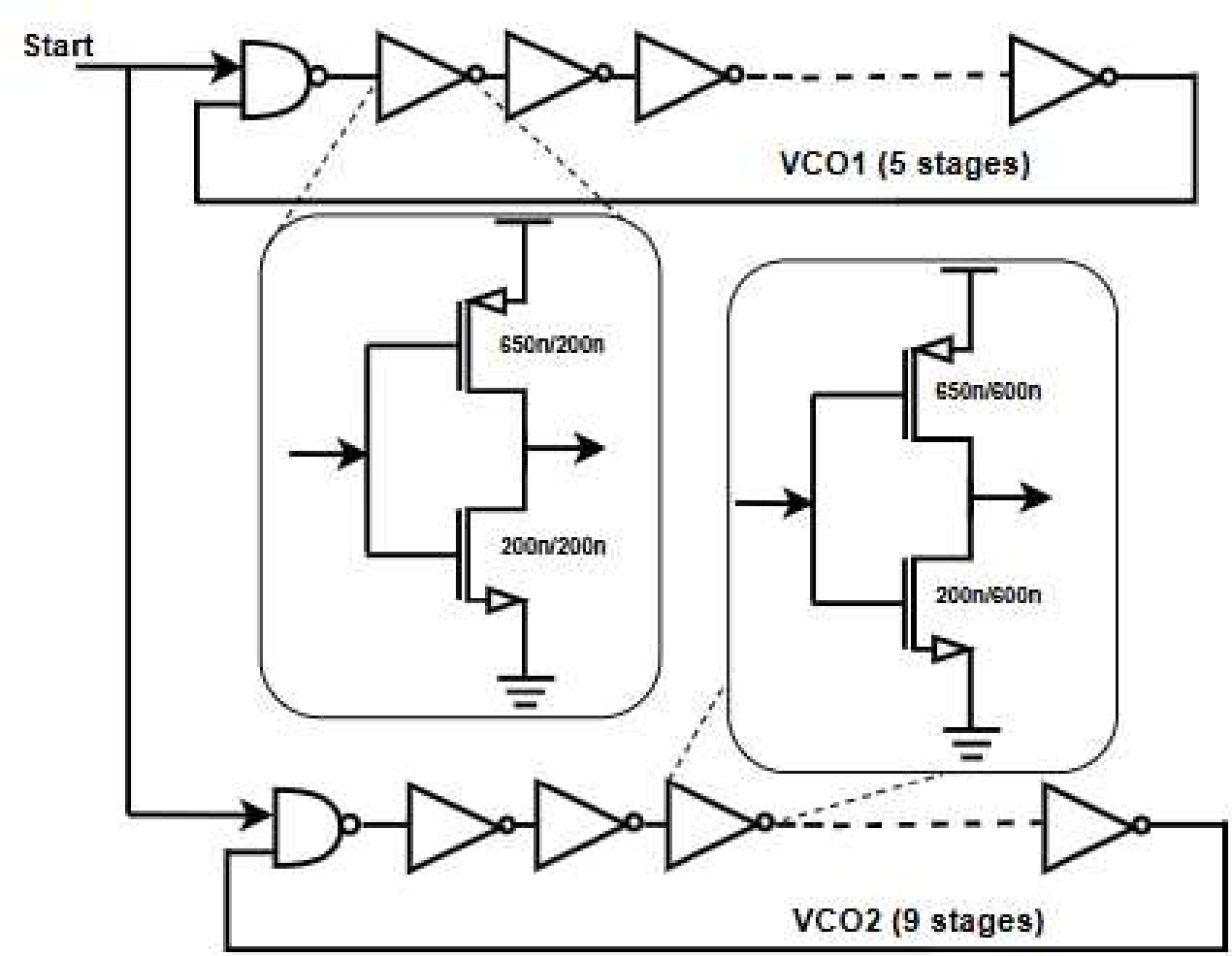


Figure 5. Detailed architecture of the sensor core.

2.1 Sensor core

The detailed sensor architecture is shown in Fig.5 with VCO1 and VCO2 employ 5 and 9 inverter stages, respectively. Increasing the number of delay stages increases the loop delay and correspondingly reduces the oscillation frequency. Operating at a lower oscillation frequency reduces power consumption in the synthesized digital processing blocks. The transistor widths in the delay cell are carefully sized to achieve equal rise and fall times under near threshold operation. Consequently, the standard cells are redesigned rather than using conventional library cells. The threshold voltage difference between the delay cell transistors in VCO1 and VCO2 is generated using the reverse short channel effect. VCO2 employs transistors with a 3× longer channel length ($L_2 = 600nm$) compared to VCO1 ($L_1 = 200nm$).

In 65-nm CMOS process, this channel-length scaling results in an approximate threshold voltage difference of 52mV for NMOS devices and 48mV for PMOS devices at room temperature under typical-typical (TT) conditions as shown in Fig.6. Across process corners, the absolute threshold voltages vary; however, the relative threshold voltage difference introduced by the channel-length scaling remains consistent under slow-slow (SS) and fast-fast (FF) corners, preserving the intended frequency offset between the two VCOs. The channel length of VCO1 is chosen through simulations such that the process variations are limited.

2.2 Temperature Quantization Module

The temperature quantization module primarily consists of two asynchronous counters, denoted as Counter1 and Counter2, as shown in Fig.4. The block diagram of an N-bit counter is illustrated in Fig.7. In the proposed implementation, Counter1 and Counter2 are realized as 13 bit and 10 bit circuits, respectively.

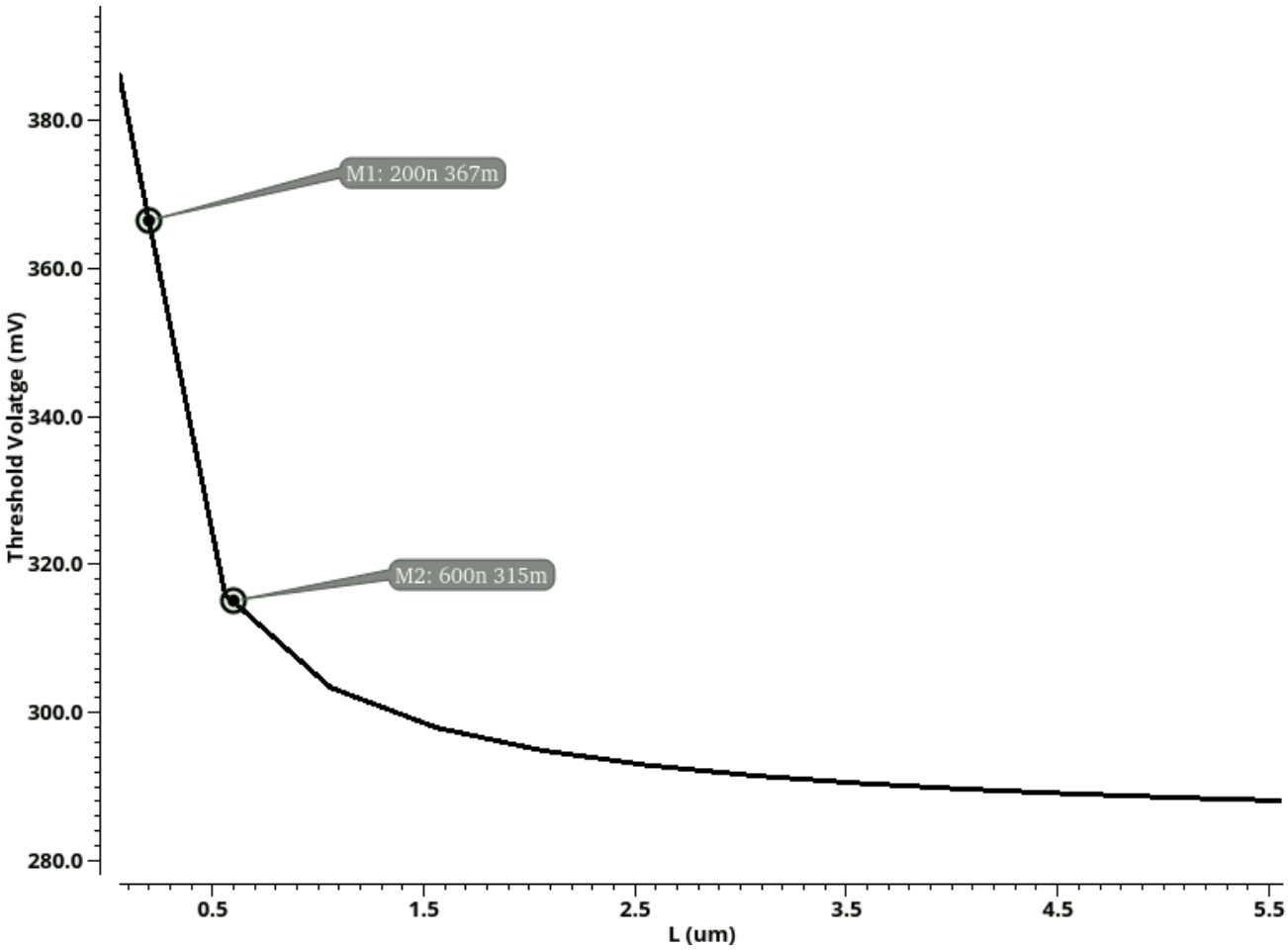


Figure 6. Reduction in threshold voltage with channel length due to RSCE.

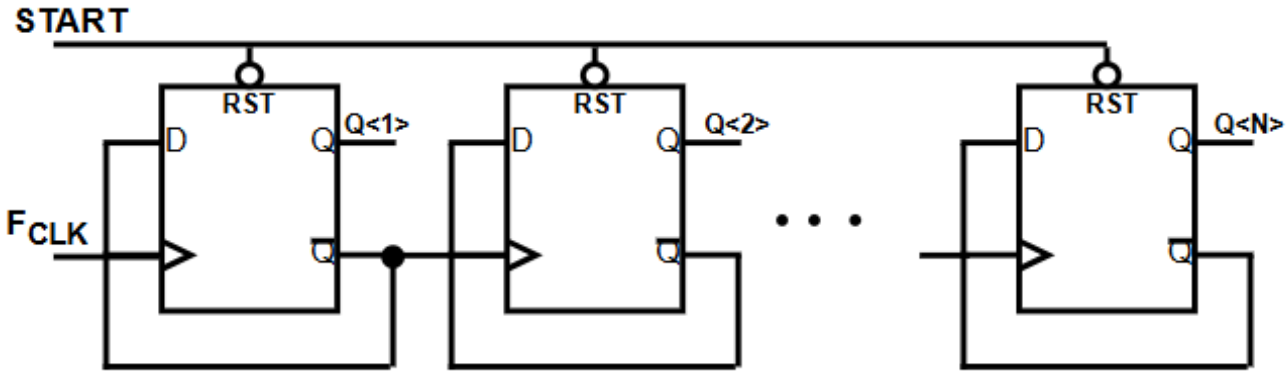


Figure 7. Asynchronous up-counter used in temperature quantization module.

The output clocks and from VCO1 and VCO2 are applied to Counter1 and Counter2, respectively, enabling on chip digital conversion. Counter 2 acts as a reference counter deciding the conversion time. The conversion time is given by

$$T_{conv} = \frac{N}{f_{\text{clk2}}} \tag{6}$$

where N is the set point, equal to 2^{10} according to the size of the reference counter. The output of Counter2 is fed to the control block (CB), which generates the end of conversion (EOC) signal. During sensing operation, Counter1 continues to count clock

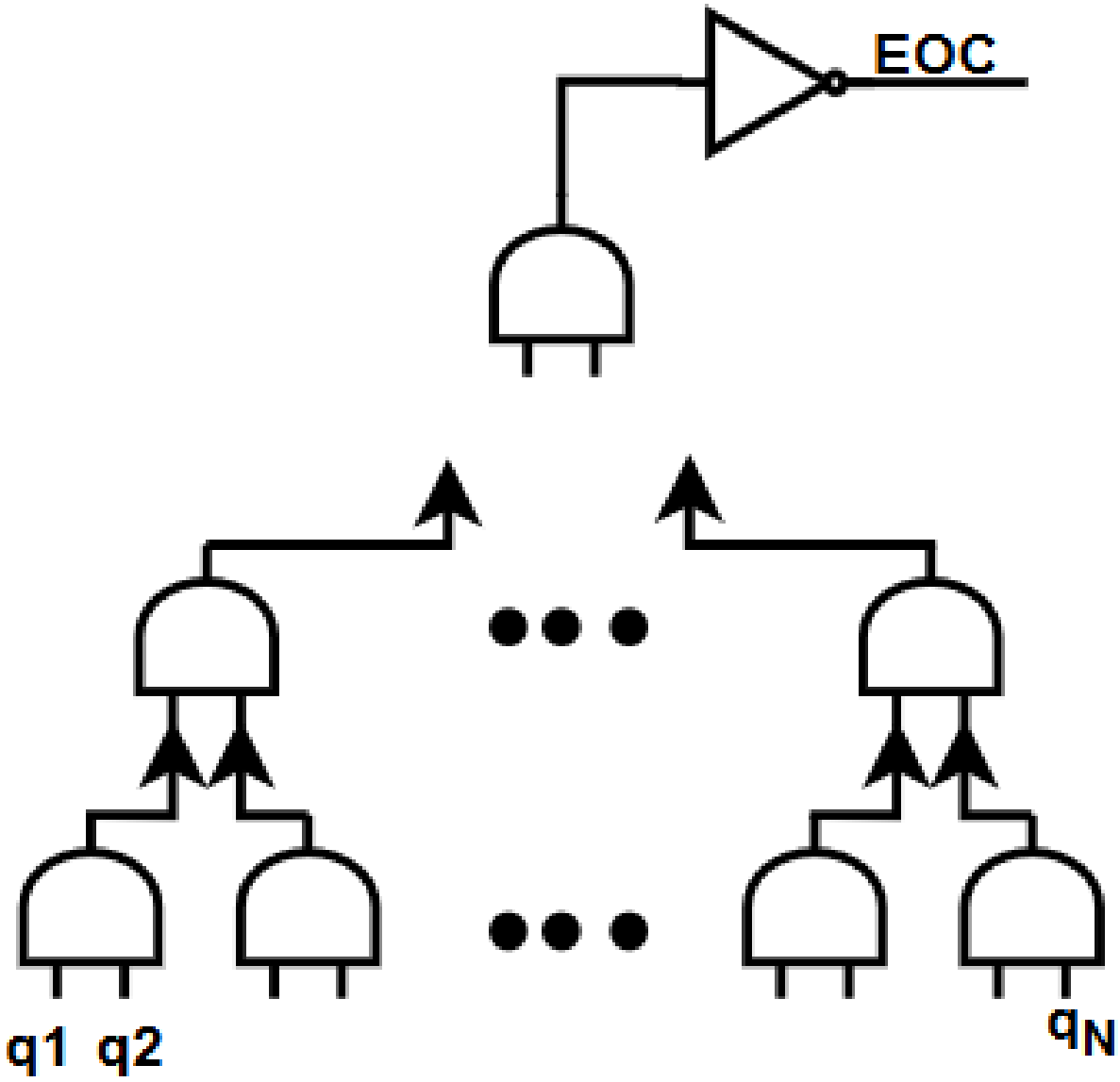


Figure 8. Control Block.

edges until EOC is asserted. Once the reference counter reaches the preset count, the CB asserts the EOC signal, terminating both counters. The resulting count value of counter 1 is latched as the digital output code (Dout).

$$T_{\text{conv}} = \frac{D_{\text{out}}}{f_{\text{clk1}}} \tag{7}$$

Combining (6) and (7), the output code is obtained as

$$D_{\text{out}} = N \times \frac{f_{\text{clk1}}}{f_{\text{clk2}}} \tag{8}$$

A higher temperature resolution can be achieved by increasing the frequency and amplification factor, or by reducing the reference clock frequency. However, higher operating frequencies increase the counter complexity and power consumption, while an excessively large amplification factor leads to a longer conversion time. In this design, reference counter size is selected to achieve high resolution while maintaining a reasonable conversion time. Consequently, the design involves a trade off among resolution, power consumption, and conversion time.

2.3 Control block

The control block (CB) is implemented using combinatorial gates such as AND and NOT gates, as shown in Fig.8. The CB is configured such that the outputs of all AND gates transition to logic high once the N bit Counter 2 completes 2^N counts. The subsequent inversion by the NOT gate generates a logic low end of conversion (EOC) signal. This EOC signal marks the completion of the conversion cycle by simultaneously disabling both oscillators and counters. All basic standard cells used in this design are appropriately sized, enabling reliable functionality and minimal delay when operating at near-threshold voltages, which is critical for ultra-low-power applications.

3 RESULTS AND ANALYSIS

The proposed design is implemented in 65 nm CMOS technology and operates at a supply range of 0.45–0.55V. Unless otherwise specified, all measured results are taken at a nominal supply voltage of 0.5V. The sensor occupies a total silicon area of 0.00085mm², as shown in the layout Fig9. The temperature dependence of the oscillation frequencies of VCO1 and VCO2 evaluated by post layout simulation results is presented in Fig.10(a) and Fig.10(b), respectively. As the temperature varies from -40°C to 125°C, the oscillation frequency of VCO1 increases from 265MHz to 483MHz, corresponding to a temperature coefficient of about +3460ppm/°C. Over the same temperature range, VCO2 exhibits a frequency variation from 35MHz to 47MHz, resulting in a least temperature coefficient of approximately +1580ppm/°C. This reduced temperature sensitivity observed in VCO2 is consistent with its lower transistor threshold voltage in the NTV region and mutual cancellation of mobility and threshold voltage variation with temperature. As a consequence, the ratio of the oscillation frequencies of the two VCOs exhibits the intended proportional to absolute temperature (PTAT) behavior, as illustrated in Fig.10(c).

The measured Dout from the TDC after post layout simulations across process corners is illustrated in Fig.11. A second order polynomial fitting relationship between the digital output and temperature is established using sufficient set of calibration temperature points. After extracting the fitting coefficients, the dout samples are applied to the inverse model to estimate temperature, and the corresponding estimation error was computed. After one point calibration at 60°C, the measured peak to peak error over the -40°C–125°C temperature range is +1.8°C to -3.5°C from the FF corner as shown in Fig.12. Monte Carlo simulations were performed to assess the impact of process variation and device mismatch on the temperature output codes. Fig.13 shows the results obtained from 1000 MC simulation runs.

The impact of supply voltage variation on temperature measurement accuracy was evaluated at 27°C. During these measurements, the supply voltage was swept over a 100mV range from 0.45V to 0.55V and the corresponding result is presented in Fig.14. The design's robustness is validated through Monte Carlo simulations, showing stability against variations in supply voltage and process corners as seen in Fig.15. Incorporating a trimming mechanism for the capacitance load in the VCO2 delay cell based on the operating supply voltage could further suppress supply sensitivity over a wide voltage range and across process corners. Post layout stability analysis for the phase noise is reported as shown in Fig.16.

The power consumption of the proposed temperature sensor was characterized over the operating temperature range, and the measured results are presented in Fig.17(a). When operating at a supply voltage of 0.5V, the sensor dissipates 5.5µW at room temperature. Of this total, approximately 2.9µW is consumed by the synthesized digital logic, while the two VCOs together account for about 2.6µW. The leakage and active power components of the sensor were characterized as a function of temperature, and the measured results are shown in Fig.17(b). As temperature increases, the oscillation frequency of the VCOs increases, leading to an increase in active (dynamic) power consumption. Elevated temperatures also cause an increase in leakage currents in both the digital logic and the VCOs. However, the proposed sensor exhibits significantly lower total power consumption compared to state-of-the-art designs, owing to its near-threshold voltage operation, making it a suitable candidate for IoT wireless sensor nodes.

Table I presents a comparison of the proposed temperature sensor with state of the art designs reported in the literature. A graphical performance comparison with previously published temperature sensors is shown in Fig.18 and Fig.19.

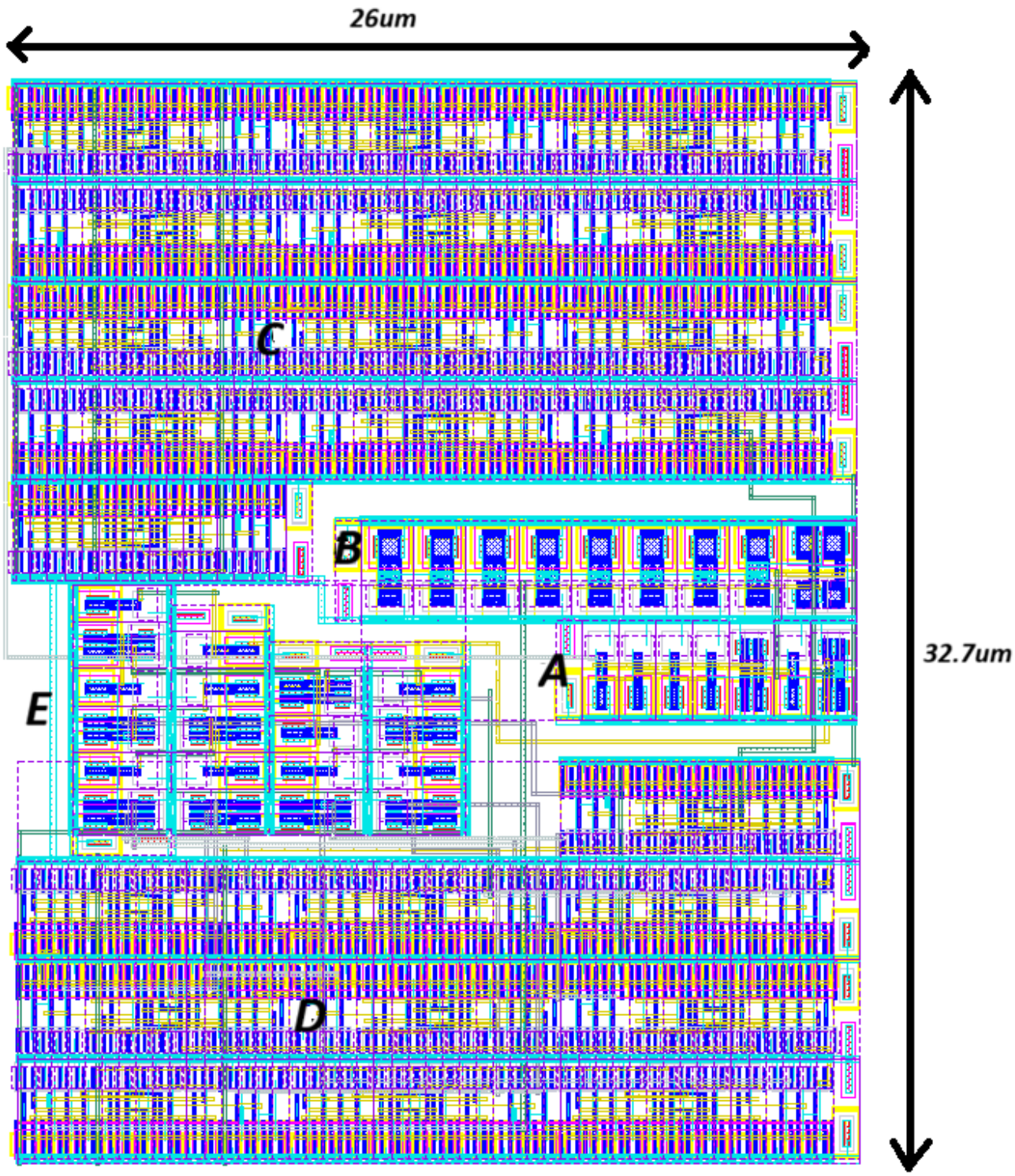


Figure 9. Layout of the temperature sensor. (A) VCO1, (B) VCO2, (C) Counter 1, (D) Counter 2, (E) Control Block.

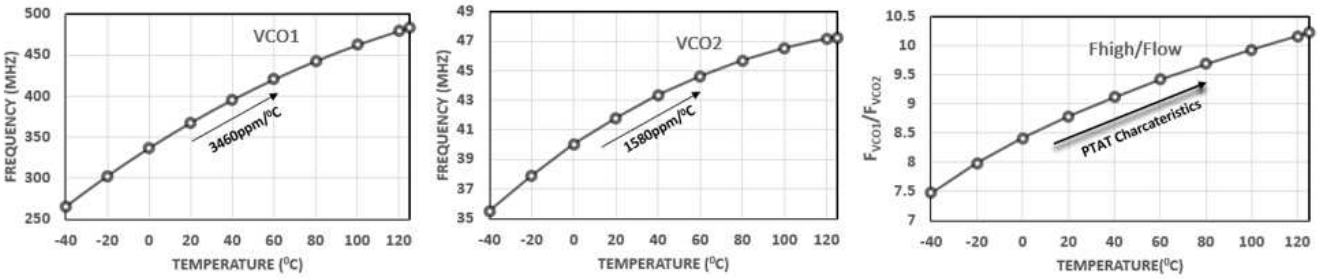


Figure 10. Temperature sensitivity of (A)VCO1, (B)VCO2, and (C)Ratio

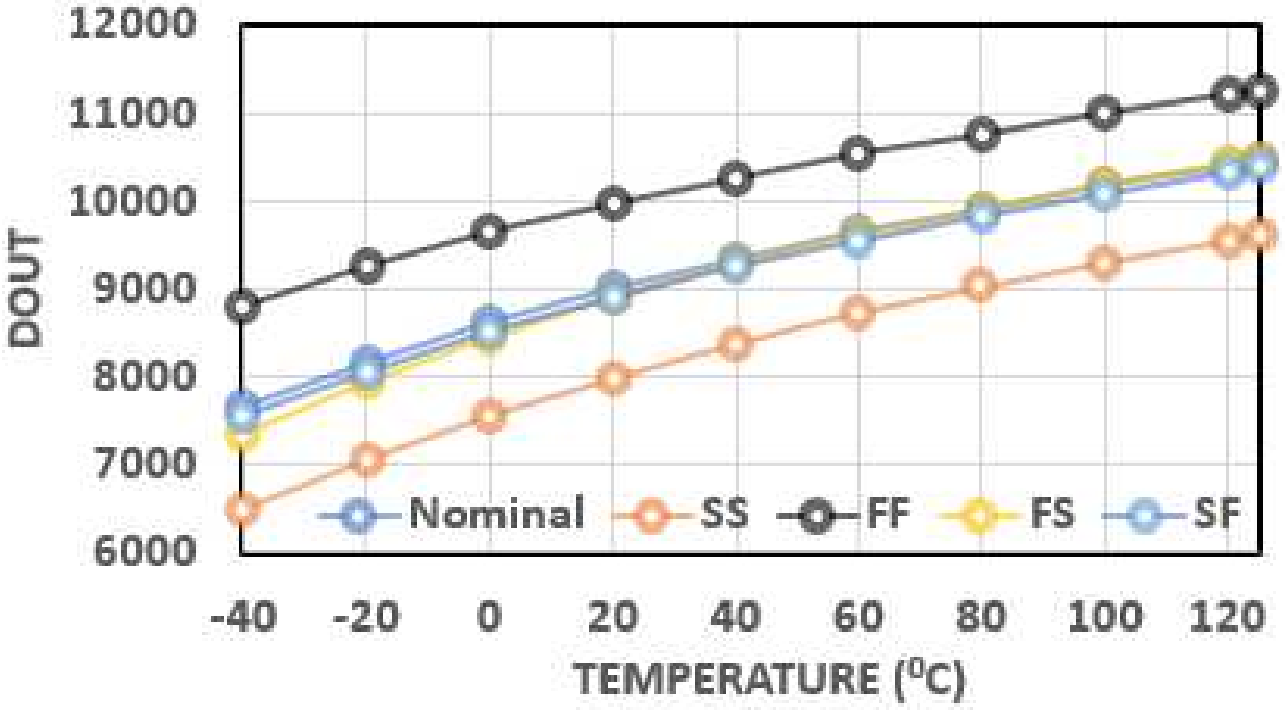


Figure 11. Measured count values with temperature across process corners.

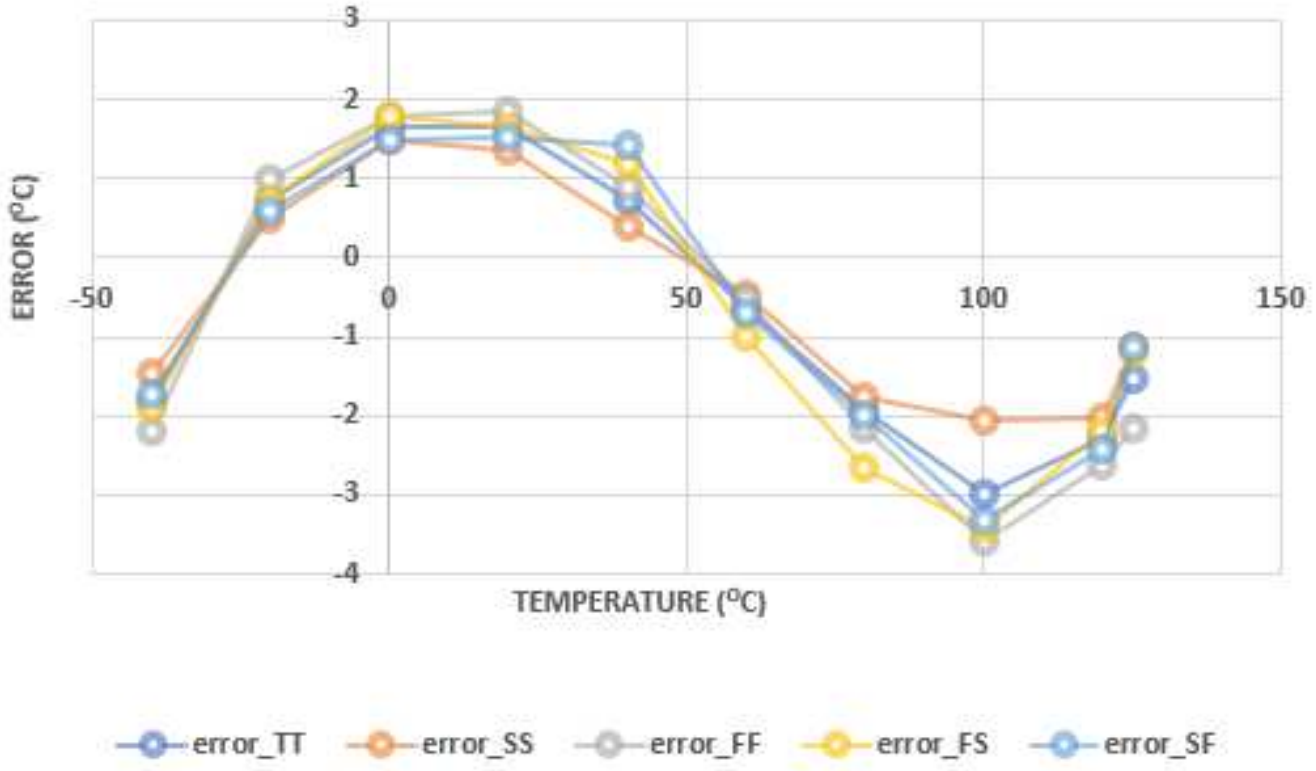


Figure 12. Measured error after one-point calibration at 60°C.

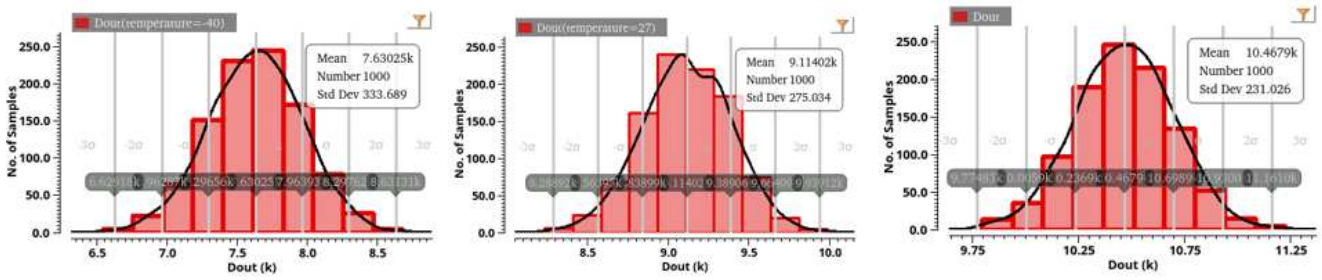


Figure 13. Monte Carlo runs for 1000 samples: (A) −40°C, (B) 27°C, and (C) 125°C.

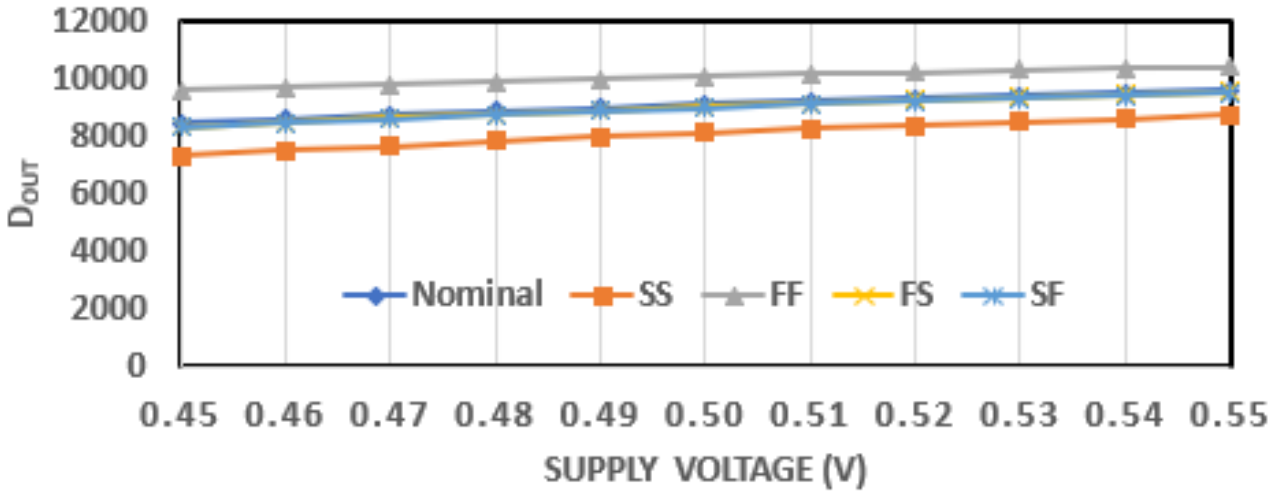


Figure 14. Dout variation with supply voltage across corners.

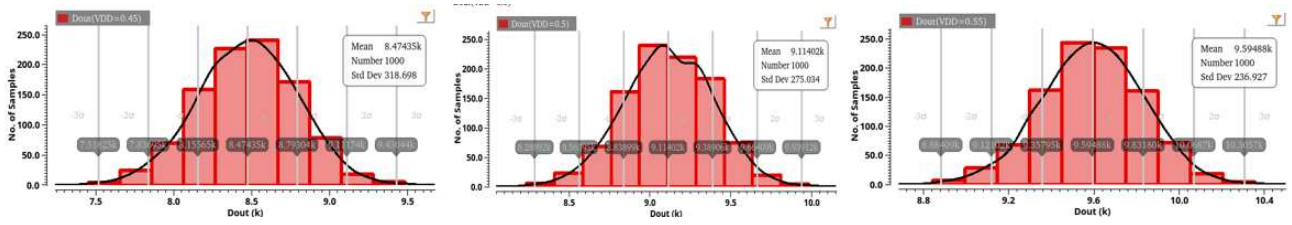


Figure 15. Variations in Dout at 3 different supply voltages using 1000 samples: (A) 0.45V, (B) 0.5V, and (C) 0.55V.

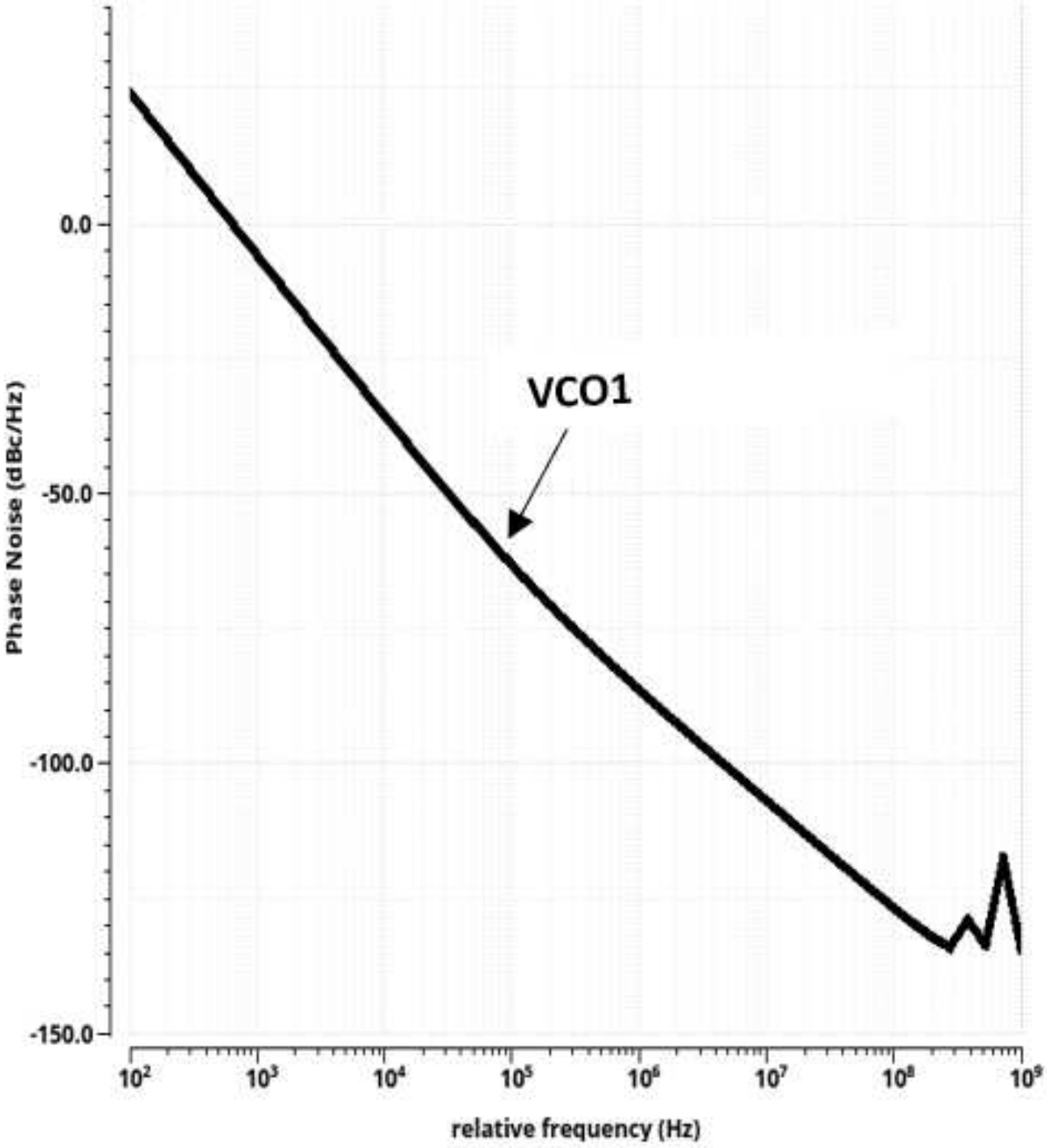


Figure 16. Post layout simulated phase noise of VCO.

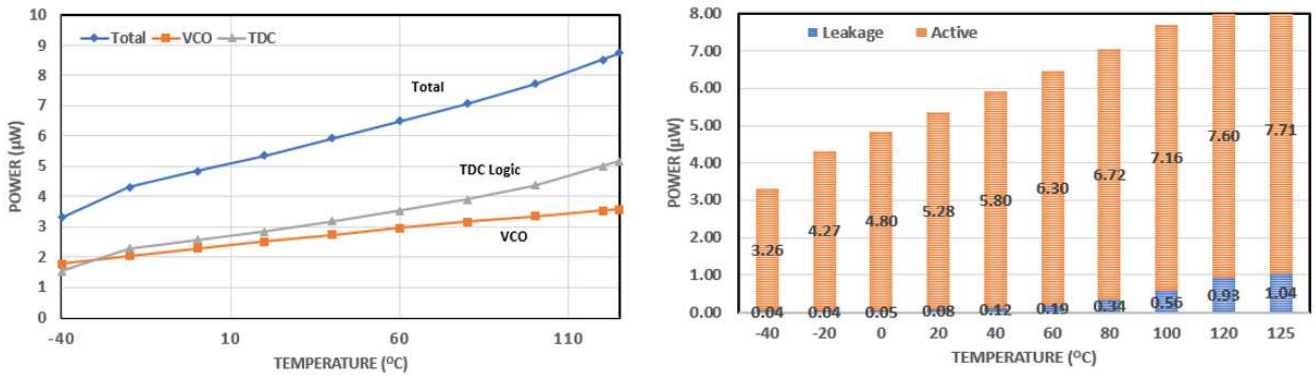


Figure 17. (a) Measured total power verses temperature. (b) Active and leakage components in total power.

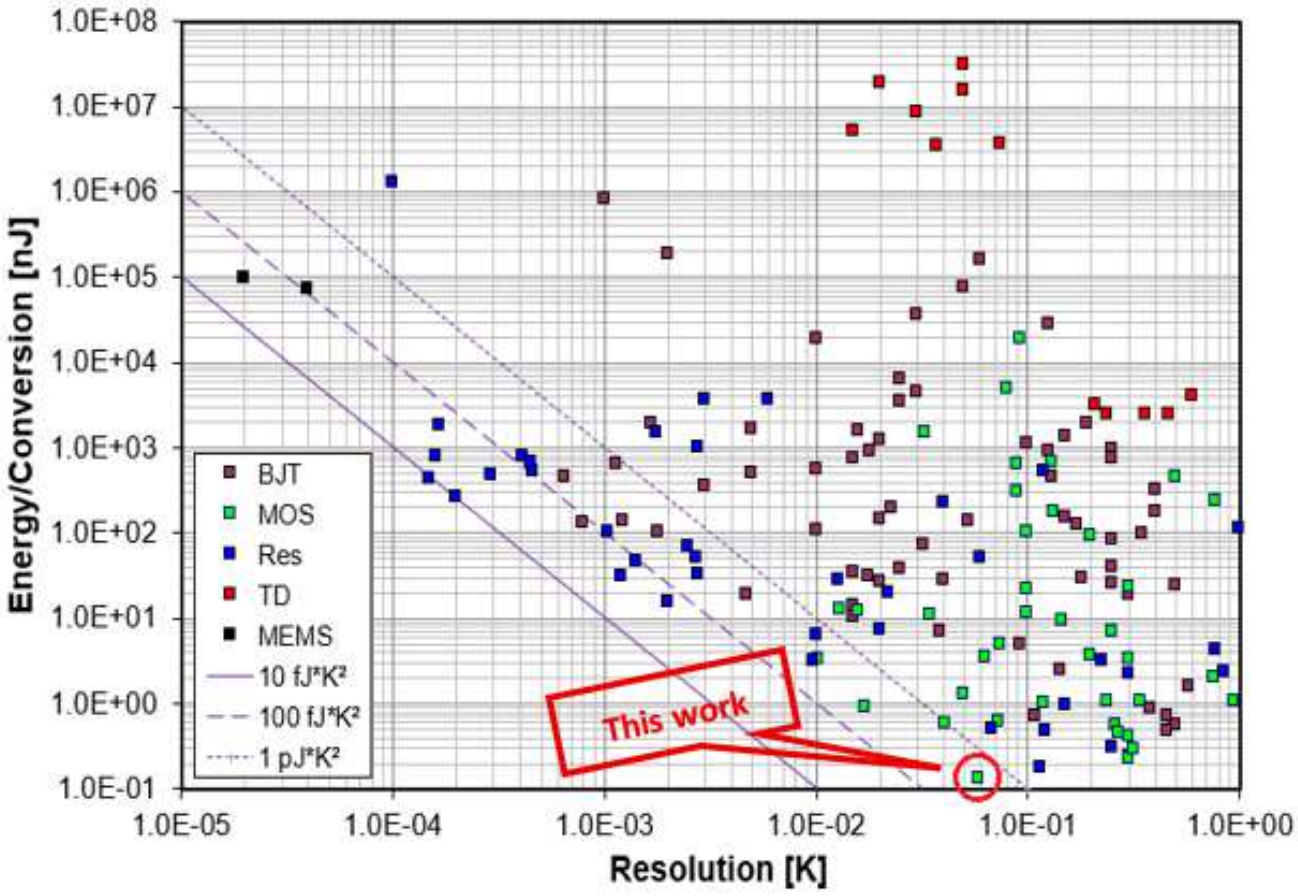


Figure 18. Graphical comparison of the proposed sensor in the energy-per-measurement versus resolution plot[34].

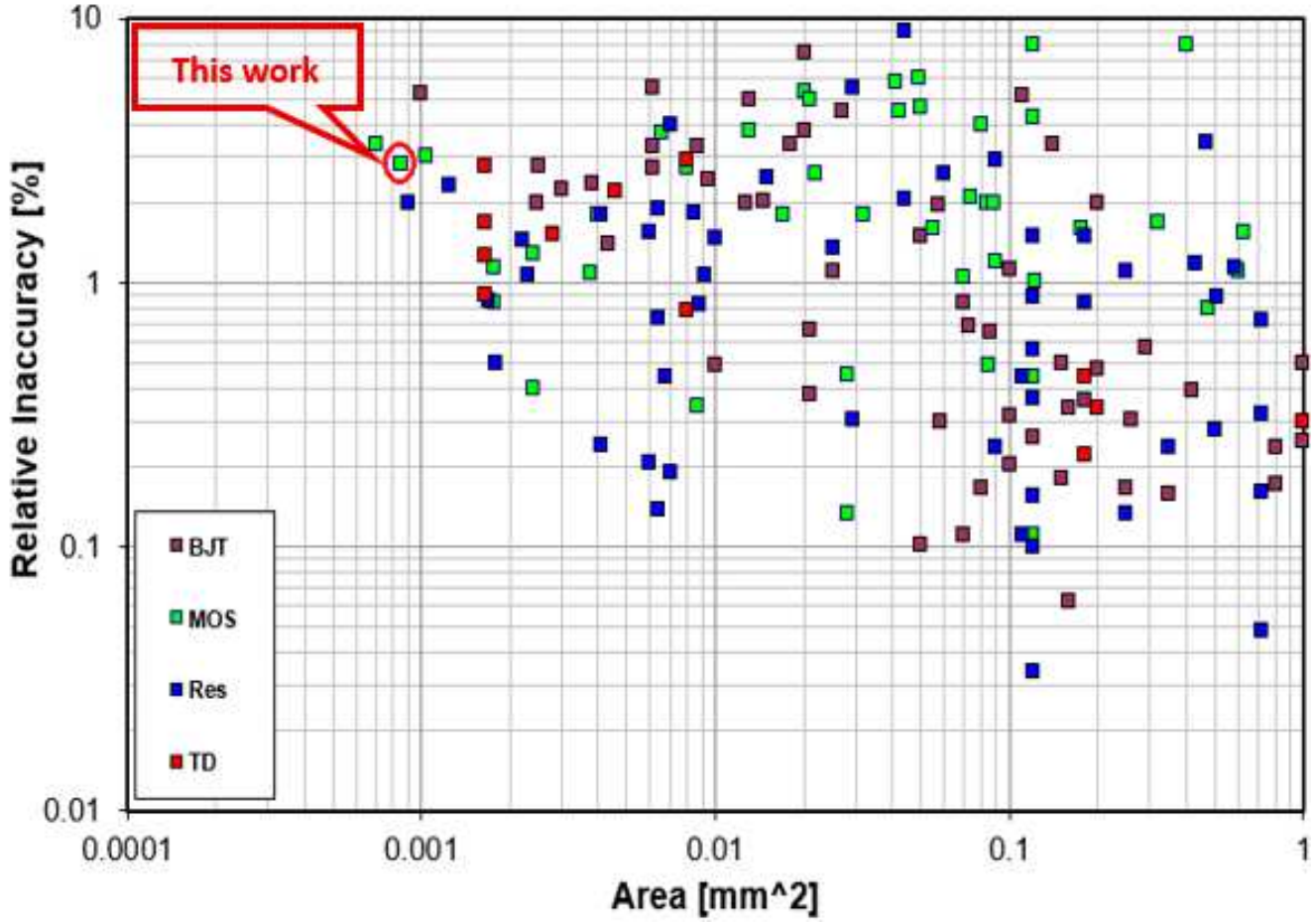


Figure 19. Graphical comparison of the proposed sensor in the relative inaccuracy versus area plot[34].

Table 1. PERFORMANCE COMPARISON OF THE PROPOSED TEMPERATURE SENSOR WITH STATE-OF-THE-ART DESIGNS

Parameter	This Work	Sensors J'24[28]	Sensors J'24[4]	TCAS2 '23[8]	JSSC'21 [15]	TransIM '20[27]	JSSC'19 [24]	JSSC'19 [16]	JSSC'16 [8]	TJEC'17 [26]	Sensors J'16[25]	Sensors J'14[12]
Technology (nm)	65	180	600	180	55	130	180	65	65	65	180	130
Type	MOS	MOS	BJT	Hybrid	TDS	MOS	MOS	TDS	MOS	MOS	Hybrid	TDS
Supply Voltage(V)	0.5	0.5	2.7-5.5	1.8	0.8-1.3	1.3	0.8	0.5	1.0	0.5-1.0	1.5	1.2
Temp. range (^oC)	-40-125	-40-125	-55-125	-40-70	-40-85	-20-85	-20-80	0-100	0-100	-55-125	-40-100	20-120
Resolution (^oC)	0.06	0.22	0.029	N/A	0.017	0.012	0.145	0.3	0.3	0.26	N/A	0.595
Conversion Time (ms)	0.0242	0.1	1.48	N/A	1.04	2	839	0.3	0.022	100	N/A	0.0023
Calibration	1-point	2-point	0-point	N/A	1-point	2-point	2-point	2-point	2-point	1-point	1-point	1-point
Sensing Error (^oC)	-2.9/+1.6 (p-p)	-0.9/+0.88 (p-p)	±1.45 (3σ)	-0.19/+0.34 (p-p)	±0.8 (3σ)	±0.6 (3σ)	-0.9/+1.2 (p-p)	-1.5/+1.6 (p-p)	-0.9/+0.9 (p-p)	-0.75/+0.8 (p-p)	-1.9/+1.5 (p-p)	-0.63/+1.04 (p-p)
Area (mm^2)	0.00085	0.0204	0.49	0.03	2.4	0.00916	0.074	0.63	0.0040	0.009	0.031	0.031
Power (μW)	5.5	0.97	747.62	2900	0.86	6	11	0.00076	3154	8.8	264	N/A
Energy/Cov (nJ)	0.133	0.097	1160	N/A	0.900	12.5	8.9	0.23	3.4	4.8	N/A	0.67
Res. FOM ($nJ.K^2$)	0.00046	0.0047	0.976	N/A	0.00026	0.0018	0.19	0.02	0.3	0.12	N/A	0.24

4 Conclusion

This work demonstrates a fully self-referenced temperature sensor realized exclusively with standard digital logic gates operating in the near-threshold regime, highlighting a highly energy- and area-efficient sensing paradigm. By converting temperature variations directly into frequency information, the proposed architecture eliminates the need for analog biasing or reference circuits, thereby improving robustness and scalability in deeply scaled CMOS technologies. A key idea of this work is the intentional creation of threshold-voltage mismatch between oscillator devices through exploitation of the reverse short-channel effect in planar CMOS, enabling temperature sensing without additional analog components or process modifications. Furthermore, the analysis of oscillator phase noise establishes fundamental limits on sensor resolution and provides valuable design insight for future frequency-based sensors. A major contribution of this work is the optimization of all digital blocks for near-threshold operation, enabling ultra-low-power operation and making the sensor a good fit for energy - limited IoT applications. In a 65-nm CMOS process, the sensor occupies only $850\mu m^2$ and achieves a competitive resolution figure-of-merit of 0.46pJ·K². Measurement results confirm accurate temperature sensing over a wide operating range from $-40°C$ to $125°C$, with a peak-to-peak inaccuracy of $+1.6°C/-2.9°C$ after one-point calibration with polynomial correction at nominal process corner. These results underscore the viability of purely digital, mismatch-aware sensor architectures for ultra-low-power systems-on-chip, making this approach particularly attractive for large-scale integration in IoT, embedded monitoring, and energy-constrained applications.

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References

1. H. Park and J. Kim, "A 0.8-V Resistor-Based Temperature Sensor in 65-nm CMOS With Supply Sensitivity of 0.28 °C/V," in *IEEE Journal of Solid-State Circuits*, vol. 53, no. 3, pp. 906-912, March 2018, doi: 10.1109/JSSC.2017.2788878.
2. J. Kim, S. Lee and M. Lee, "A 0.9V Self-Referenced Resistor-Based Temperature Sensor With -0.62/+0.81°C (3σ) Inaccuracy," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 12, pp. 4319-4323, Dec. 2023, doi: 10.1109/TCSII.2023.3291621.
3. Y. Lee, T. Kim and Y. Chae, "A 0.9-V $6400\mu m^2$ Resistor-Based Temperature Sensor With a One-Point Trimmed 3σ Inaccuracy of ±0.64 °C from -50°C to 125°C ," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 9, pp. 3313-3317, Sept. 2023, doi: 10.1109/TCSII.2023.3268166.
4. H. Fan et al., "A 13-bit Temperature Sensor with a ±1.45°C (3) Inaccuracy from -55°C to 125°C," in *IEEE Sensors Journal*, doi: 10.1109/JSEN.2024.3411649.
5. B. Wang and M. -K. Law, "Subranging BJT-Based CMOS Temperature Sensor With a ±0.45 °C Inaccuracy (3σ) From -50 °C to 180 °C and a Resolution-FoM of 7.2 pJ·K² at 150 °C," in *IEEE Journal of Solid-State Circuits*, vol. 57, no. 12, pp. 3693-3703, Dec. 2022, doi: 10.1109/JSSC.2022.3208770.
6. T. -J. Lee and K. -H. Tu, "High-Sensitivity PTAT Current Generator Using PTAT and CTAT Current Subtraction Method for Temperature Sensor With Frequency Output," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 70, no. 10, pp. 3922-3926, Oct. 2023, doi: 10.1109/TCSII.2023.3289137.
7. Z. Tang, S. Pan, M. Grubor and K. A. A. Makinwa, "A Sub-1 V Capacitively Biased BJT-Based Temperature Sensor With an Inaccuracy of ±0.15°C (3σ) From—55°C to 125°C," in *IEEE Journal of Solid-State Circuits*, vol. 58, no. 12, pp. 3433-3441, Dec. 2023, doi: 10.1109/JSSC.2023.3308554.
8. Z. Tang, X. -P. Yu, K. A. A. Makinwa and N. N. Tan, "A 0.8-V BJT-Based Temperature Sensor With an Inaccuracy of ± 0.4°C (3σ) From -40°C to 125°C in 22-nm CMOS," in *IEEE Journal of Solid-State Circuits*, doi: 10.1109/JSSC.2024.3523482.
9. R. G. Dreslinski, M. Wieckowski, D. Blaauw, D. Sylvester, and T. Mudge, "Near-threshold computing: Reclaiming moore's law through energy efficient integrated circuits," Proc. IEEE, 2010, doi: 10.1109/JPROC.2009.2034764.
10. J. Zhou, T. T.-H. Kim, and Y. Lian, "Near-threshold processor design techniques for power-constrained computing devices," in *2017 IEEE 12th International Conference on ASIC* (ASICON), Oct. 2017, pp. 920–923, doi: 10.1109/ASICON.2017.8252627.
11. J. Jun, J. Song, and C. Kim, "A Near-Threshold Voltage Oriented Digital Cell Library for High-Energy Efficiency and Optimized Performance in 65nm CMOS Process," *IEEE Trans. Circuits Syst. I Regul. Pap.*, vol. 65, no. 5, pp. 1567–1580, 2018, doi: 10.1109/TCSI.2017.2758793.

12. Souri, K., Makinwa, K.A.A. Energy-Efficient Smart Temperature Sensors in CMOS Technology (Analog Circuits and Signal Processing), *Springer International Publishing AG; 1st ed. 2018 Edition* (13 October 2017) ISBN-10 : 3319623060.

13. Zhong TANG, Xiao-Peng YU, Zheng SHI, et al., "CMOS Temperature Sensors: From Module Design to System Design," *Chinese Journal of Electronics*, vol. 34, no. 1, pp. 1–10, 2025 doi: 10.23919/cje.2023.00.425.

14. M. Pertijs, K. Makinwa and J. Huijsing, "A CMOS temperature sensor with a 3σ inaccuracy of $\pm 0.1 deg/C$ from -55°C to 125°C," ISSCC. 2005 *IEEE International Digest of Technical Papers. Solid-State Circuits Conference*, 2005., San Francisco, CA, USA, 2005, pp. 238-596 Vol. 1, doi: 10.1109/ISSCC.2005.1493957.

15. C. Deng, Y. Sheng, S. Wang, W. Hu, S. Diao and D. Qian, "A CMOS Smart Temperature Sensor With Single-Point Calibration Method for Clinical Use," in *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 63, no. 2, pp. 136-140, Feb. 2016, doi: 10.1109/TCSII.2015.2483419.

16. Y. -J. An, K. Ryu, D. -H. Jung, S. -H. Woo and S. -O. Jung, "An Energy Efficient Time-Domain Temperature Sensor for Low-Power On-Chip Thermal Management," in *IEEE Sensors Journal*, vol. 14, no. 1, pp. 104-110, Jan. 2014, doi: 10.1109/JSEN.2013.2280647.

17. Poki Chen, Chun-Chi Chen, Chin-Chung Tsai and Wen-Fu Lu, "A time-to-digital-converter-based CMOS smart temperature sensor," in *IEEE Journal of Solid-State Circuits*, vol. 40, no. 8, pp. 1642-1648, Aug. 2005, doi: 10.1109/JSSC.2005.852041.

18. S. Joo et al., "Highly Accurate, Fully Digital Temperature Sensor With Curvature Correction," in *IEEE Sensors Journal*, vol. 21, no. 19, pp. 21248-21258, 1 Oct.1, 2021, doi: 10.1109/JSEN.2021.3103982.

19. Z. Tang, Z. Huang, X. -P. Yu, Z. Shi and N. N. Tan, "A $0.26 pJK^2$ 2400-μm^2 Digital Temperature Sensor in 55-nm CMOS," in *IEEE Solid-State Circuits Letters*, vol. 4, pp. 96-99, 2021, doi: 10.1109/LSSC.2021.3072989.

20. H. Wang and P. P. Mercier, "A 763pW 230pJ/Conversion Fully Integrated CMOS Temperature-to-Digital Converter With +0.81 °C/-0.75 °C Inaccuracy," in *IEEE Journal of Solid-State Circuits*, vol. 54, no. 8, pp. 2281-2290, Aug. 2019, doi: 10.1109/JSSC.2019.2916418.

21. Yu-Lung Lo, Wei-Tsuen Chen, Yu-Ting Chiu, and Wei-Bin Yang, "A High-Resolution All-Digital Temperature Sensor with Process Variation Compensation," in *Sensors and Materials*, Vol. 28, No. 5 (2016) 395–402.

22. Y. -L. Lo and Y. -T. Chiu, "A High-Accuracy, High-Resolution, and Low-Cost All-Digital Temperature Sensor Using a Voltage Compensation Ring Oscillator," in *IEEE Sensors Journal*, vol. 16, no. 1, pp. 43-52, Jan.1, 2016, doi: 10.1109/JSEN.2015.2478792.

23. T. Anand, K. A. A. Makinwa and P. K. Hanumolu, "A VCO Based Highly Digital Temperature Sensor With 0.034 °C/mV Supply Sensitivity," in *IEEE Journal of Solid-State Circuits*, vol. 51, no. 11, pp. 2651-2663, Nov. 2016, doi: 10.1109/JSSC.2016.2598765.

24. A. Bakker, "CMOS smart temperature sensors - an overview," *SENSORS*, 2002 IEEE, Orlando, FL, USA, 2002, pp. 1423-1427 vol.2, doi: 10.1109/ICSENS.2002.1037330.

25. M. A. P. Pertijs, A. L. Aita, K. A. A. Makinwa and J. H. Huijsing, "Low-Cost Calibration Techniques for Smart Temperature Sensors," in *IEEE Sensors Journal*, vol. 10, no. 6, pp. 1098-1105, June 2010, doi: 10.1109/JSEN.2010.2040730.

26. R. Sun and H. Huang, "A Fully Digital Time-Domain Temperature Sensor for Battery-Powered Wireless Sensor Network," 2024 4th International Conference on Electronics, Circuits and Information Engineering (ECIE), Hangzhou, China, 2024, pp. 49-52, doi: 10.1109/ECIE61885.2024.10626551.

27. T. Someya, A. K. M. M. Islam, T. Sakurai and M. Takamiya, "An 11-nW CMOS Temperature-to-Digital Converter Utilizing Sub-Threshold Current at Sub-Thermal Drain Voltage," in *IEEE Journal of Solid-State Circuits*, vol. 54, no. 3, pp. 613-622, March 2019, doi: 10.1109/JSSC.2019.2891718.

28. M. Jalalifar and G. -S. Byun, "A Wide Range CMOS Temperature Sensor With Process Variation Compensation for On-Chip Monitoring," in *IEEE Sensors Journal*, vol. 16, no. 14, pp. 5536-5542, July15, 2016, doi: 10.1109/JSEN.2016.2568242.

29. M. Bashir, S. R. Patri, and K. Prasad, "Low-power voltage to a frequency-based smart temperature sensor with +0.8°C/-0.75°C accuracy for -55°C to 125°C," *Turkish J. Electr. Eng. Comput. Sci.*, vol. 25, no. 6, pp. 4880–4892, 2017.

30. A. Ballo, G. Bruno, A. D. Grasso and M. G. G. Vaiana, "A Compact Temperature Sensor With a Resolution FoM of 1.82 pJK^2," in *IEEE Transactions on Instrumentation and Measurement*, vol. 69, no. 10, pp. 8571-8579, Oct. 2020, doi: 10.1109/TIM.2020.2992839.

31. C. Jayaram and P. S. Rao, "A 0.5-V Energy-Efficient CMOS Temperature Sensor With 97.64 pJ/Conversion for Portable Applications," in *IEEE Sensors Journal*, vol. 24, no. 3, pp. 2436-2444, 1 Feb.1, 2024, doi: 10.1109/JSEN.2023.3338957.

32. Nayak, R., Kianpoor, I. Bahubalindruni, P.G. Low power ring oscillator for IoT applications. *Analog Integr Circ Sig Process* 93, 257–263 (2017). https://doi.org/10.1007/s10470-017-1015-2.

33. P. Srikram, P. Ambalathankandy, M. Motomura and M. Ikebe, "A 0.5 V Modified Pseudo-Differential Current-Starved Ring-VCO with Linearity Improvement for IoT Devices," 2023 *International Electrical Engineering* (iEECON), Krabi, Thailand, 2023, pp. 219-223, doi: 10.1109/iEECON56657.2023.10126919.

34. K.A.A. Makinwa, "Smart Temperature Sensor Survey," [Online]. Available:http://ei.ewi.tudelft.nl/docs/TSensor_survey.xls.

Data availability

All data generated or analysed during this study are included in this published article.

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Author contributions statement

Authors 1 and 2 conceived the design idea, Author 1 conducted the experiments and analyzed the results. Both authors have reviewed the results and final manuscript.

Additional information

The authors declare that they have no competing interests.