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A Power-Efficient and Noise-Resilient Domino Logic Architecture with Adaptive Keeper Control for Wide Fan-In Applications.

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Abstract

In this paper, a power efficient and noise resilient domino logic architecture is proposed for wide fan-in dynamic circuits. Conventional domino logic suffers from high power dissipation, leakage current and reduced robustness due to keeper contention and charge sharing in large PDN. To mitigate these limitations an adaptive keeper regulation scheme is introduced to suppress unnecessary contention during evaluation while preserving dynamic node stability. In addition, the PDN is restructured using a stacked footer transistor with parallel discharge path to mitigate subthreshold leakage and alleviate charge sharing without degrading evaluation speed. The proposed DLG is designed and simulated using 90 nm CMOS technology in Cadence Virtuoso. Simulation results demonstrate 54% improvements in noise margin, 34% reductions in power consumption and 33% reductions in PDP and EDP, along with improved tolerance to process variations compared to 32-in conventional domino logic gate. Furthermore, a 128-bit wide fan-in multiplexer is implemented to validate the effectiveness of proposed approach.

Keywords:

CMOS technology, Domino logic, Noise efficient, Wide fan in

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1. Introduction

The continuous growth of portable and wireless devices has pushed VLSI circuit to deliver higher performance with lower power. CMOS technology scaling, achieved through reduced device dimensions and lower supply voltages has been a key driver of these improvements. However, sustaining adequate drive current under reduces supply levels requires lowering the threshold voltage (V_{th}), which significantly increases leakage current [1,2]. Among different circuit families domino logic gained wide acceptance in high-speed processor, especially for implementing wide fan-in gates [3]. Compare to static logic, domino logic is preferred due to their compact layout and lower parasitic capacitance [4]. Despite these advantages domino logic faces significant challenges, including high power dissipation, leakage and limited noise immunity especially in scaled technologies [5]. At sun-90 nm nodes, leakage current becomes a dominant factor contributing more than half of the total power consumption [2,3]. This

leakage discharges the dynamic node, thereby degrading noise margin and causing logic errors. Furthermore, process variation, crosstalk, and high clock frequencies aggravate the reliability concern of domino circuit [6].

To improve robustness, a PMOS keeper in conjunction with a static inverter is commonly employed forming a domino structure with enhance noise tolerance [3,4]. In small fan-in circuits a weak keeper is sufficient however, wide fan-in gates require a stronger keeper to counteract excessive leakage. This is typically achieved by increasing the aspect ratio of the keeper transistor defined as keeper ratio (KPR). While a large keeper improves noise immunity it also introduces contention with the NMOS pull-down network (PDN) leading to higher delay, greater power dissipation and increased sensitivity to process variations [7-9]. As illustrated in Fig. 1(c) the keeper size has a direct impact on the average power consumption. Therefore, careful optimization the KR is essential as it governs the trade-off between speed, power and noise robustness in wide fan-in domino circuit [10-12].

$$KPR = \frac{\mu_p(\frac{W}{L})_{keeper\ transistor}}{\mu_n(\frac{W}{L})_{Evaluation\ transistor}} \quad (1)$$

Here W and L define the transistors channel dimensions (width and length) while μ_n and μ_p indicate the mobility values for electrons and holes.

The keeper ratio not only impacts leakage suppression and contention but also governs the charge held at the dynamic node thereby influencing the output state. A DLG comprising a precharge device, skewed inverter and keeper transistor stabilizes the node while the PDN resolves the logic. Since power is a key metric, the average power consumption is estimated similarly to static CMOS logic as expressed in Eq. (2) [7,8].

$$P_{avg} = P_{sw} + P_{sc} + P_{leak} \quad (2)$$

Where, P_{sw} corresponds to dynamic switching power, P_{sc} is short-circuit power and P_{leak} denotes leakage power arising from subthreshold and gate leakage effects. Among the different components of Pavg, the switching power is the most dominant as it arises from the repeated charging and discharging of capacitances [5,13]. It can therefore be expressed as

$$P_{sw} = \alpha_{0\to1} f_{Clk} V_{Swing} V_{DD} C_L \quad (3)$$

Here $\alpha_{0\to1}$ denotes the switching activity, f_{CLK} is the input clock frequency, C_L is the load capacitance and V_{swing} is the peak voltage swing. As expressed in Eqs.3 lowering the voltage swing in the proposed domino circuit effectively reduces the switching power.

In nano scale domino gates leakage power is dominated by subthreshold current, which increases with the number of inputs and technology scaling affecting robustness and performance [14,15]. A leakage-tolerant approach is therefore essential with subthreshold current being the primary component, as given in following equations.

$$I_{sub-th} = I_0\left(1 - e^{\left(\frac{-V_{DS}}{V_T}\right)}\right)\left(e^{\left(\frac{V_{GS} - V_{TH} + \eta V_{DS}}{nV_T}\right)}\right) \quad (4)$$

Where,

$$I_0 = \mu_0 C_{OX} \frac{W}{L} (n-1) V_T^2 \quad (5)$$

Here V_{GS} and V_{DS} correspond to the gate-source and drain source voltages, while V_{TH} and V_T are the threshold and thermal of the MOS devices. I0 indicates the reverse saturation current, n, μ_0, C_{OX}, η and W/L represent the subthreshold swing coefficient, zero-bias mobility, gate oxide capacitance, DIBIL effect, transistor width to length ratio respectively.

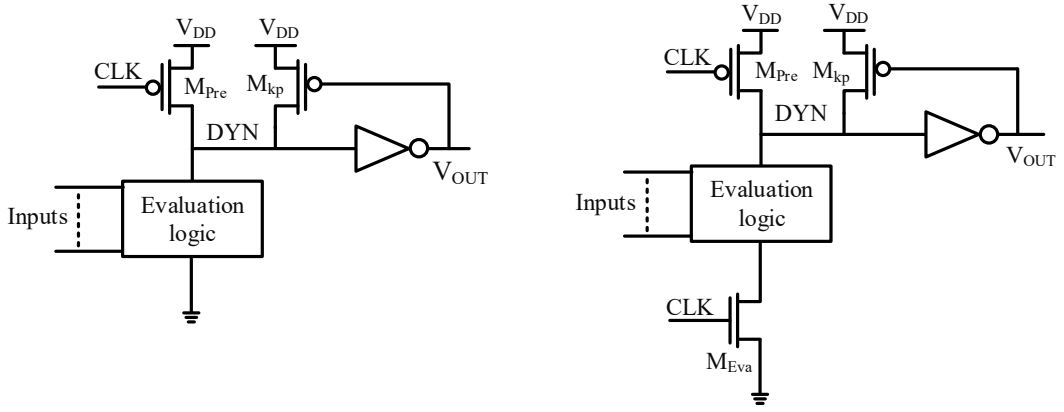
The paper is organized as follow. Section 2 review existing domino logic circuits, while section 3 introduces the proposed dynamic circuit design. Section 4 presents simulation results along with a comparative analysis. Section 5 details the implementation of the proposed wide fan-in multiplexer. Finally, section 6 summarizes the key findings and conclusions of the study.

2. Review of existing domino logic circuit

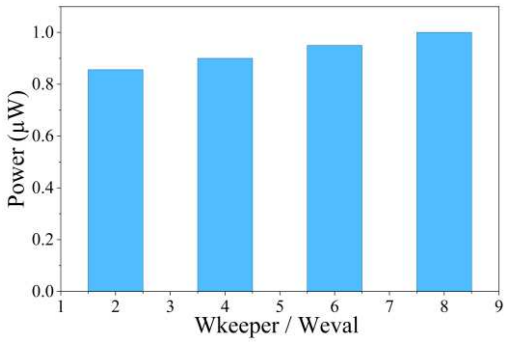
Domino logic circuits are widely used in high-performance VLSI due to their fast switching and suitability for wide fan-in applications. Various architectures have been proposed to improve noise immunity, power efficiency and robustness. Due to its potential use in low-power VLSI circuits, a study of previous research has been done to learn more about the design, operation and simulation findings of DLG.

2.1 Conventional domino logic gate

Conventional domino logic [7] is widely implemented using standard footed domino logic gate (SFLDLG) and standard footless domino logic gate (SFDLG) topologies (Fig. 1(a), (b)), but both face significant challenges. Leakage currents in the pull-down network (PDN), including band-to-band tunneling, gate tunneling and subthreshold leakage, increases sharply at nanoscale dimensions. Additionally, these circuits are highly sensitive to noise sources such as crosstalk, charge sharing, substrate noise, input fluctuations and supply/ground variations. Such effects can discharge the dynamic node (DYN) and reduce noise immunity. The degradation is more pronounced in wide fan-in gates, where numerous transistors are connected to the DYN node. To improve robustness the conventional DLG integrates a dynamic gate with a static inverter and a keeper. During evaluation phase (EV phase), the keeper maintains the DYN voltage to ensure correct logic. Upsizing the keeper enhances noise tolerance but increases delay and power dissipation due to contention with PDN transistors as shown in Fig. 1(c), highlighting the trade-off between robustness and efficiency.



(a) (b)



(c)

Fig. 1. Conventional domino logic circuits (a) SFLDLG, (b) SFDLG, (c) effect of keeper strength scaling on the power consumption in domino logic design [7].

2.2 High speed domino logic gate (HSDLG)

HSDLG approaches have been developed to enhance the performance of dynamic gate by reducing PDN-keeper contention. The HSDLG proposed by Anis et al. [12] (Fig. 2) Employs a redesigned keeper network controlled by NMOS and PMOS transistors to reduce switching power, while Mult-threshold transistors mitigate delay and leakage. However, leakage remains significant in wide fan-in designs. Additionally, HSDLG uses a delayed clock typically implemented with a two-inverter chain to conditionally activate the keeper after a brief delay lowering PDN contention during evaluation. Although this improves speed, robustness is reduced because the dynamic node initially floats. Collectively these techniques highlight the trade-off between performance and noise immunity in high-speed domino circuits.

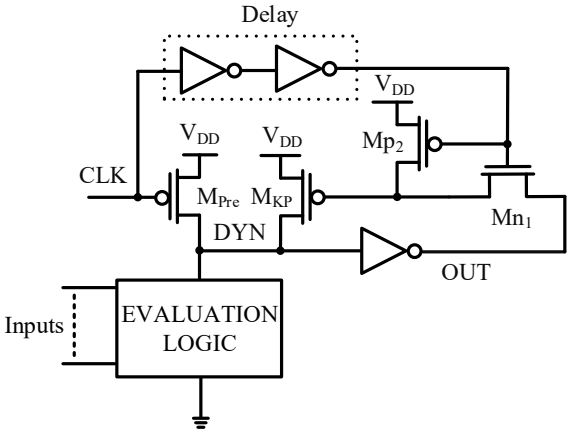


Fig. 2 High speed domino logic gate [12].

2.3 Leakage current replica domino logic gate (LCRDLG)

Lih et al. [13] presented the LCRDLG structure, as shown in Fig. 3 which combines a cascaded PMOS transistor with a keeper controlled by an analog current mirror to increase scalability and noise tolerance in dynamic logic gates. This method lowers subthreshold leakage during standby, improve keeper switching properties and allows adaptation to process, voltage and temperature (PVT) fluctuations. The design calls for an extra transistor for each gate as well as

a shared current mirror. For scalability, the keeper strength dynamically monitors PDN leakage, nevertheless wide fan-in setups have higher power consumption and lower noise tolerance.

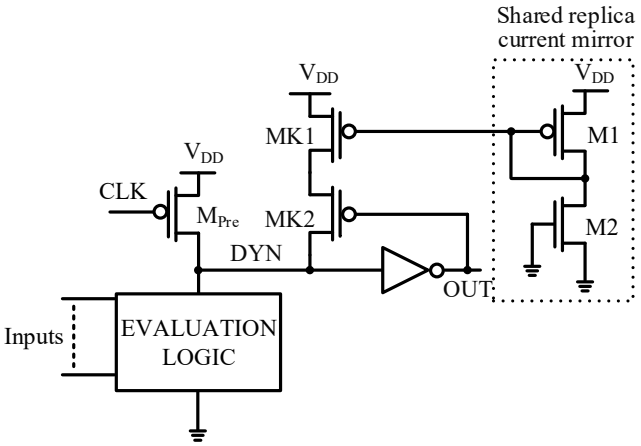


Fig. 3 Leakage current replica domino logic gate

2.4 Conditional keeper domino logic gate (CKDLG)

To address noise sensitivity in dynamic logic designs, Alvandpour et al. [14] presented the CKDLG scheme, depicted in Fig. 4. The design utilizes two keepers with different drive strengths. The weak keeper engages at the start of evaluation, whereas the strong keeper activates only if the dynamic node fails to discharge within a predefined delay. A NAND gate supervises this conditional operation. Although the approach improves immunity to leakage and noise the supplementary devices and logic contribute to greater silicon area and power dissipation.

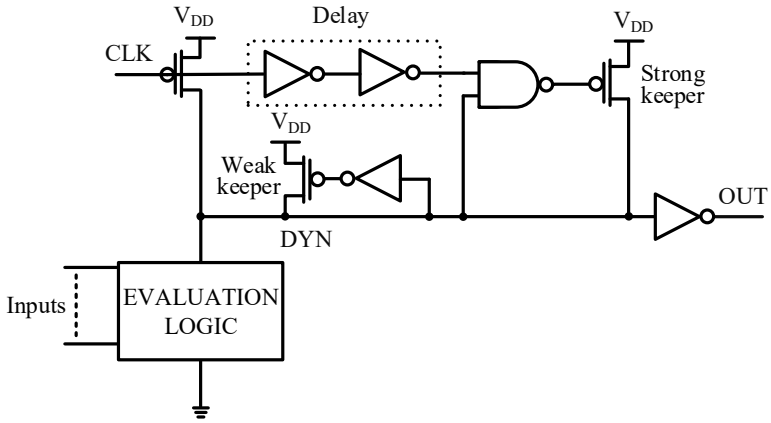


Fig. 4 Conditional keeper domino logic gate

2.5 Current comparison domino logic gate (CCDLG)

In order to suppress leakage effect in dynamic circuits, Peiravi et al. [15] proposed CCDLG, as shown in Fig. 5. The scheme evaluates the pull up network (PUN) current against a worst- case leakage reference enabling effective leakage control. Replacing PDN-based sensing with PUN comparison to prevent undesired discharge of the dynamic node and enhances noise immunity. Despite these advantages, the architecture necessitates a complex reference generation block

resulting in greater silicon area, increased delay and heightened sensitivity to process variations.

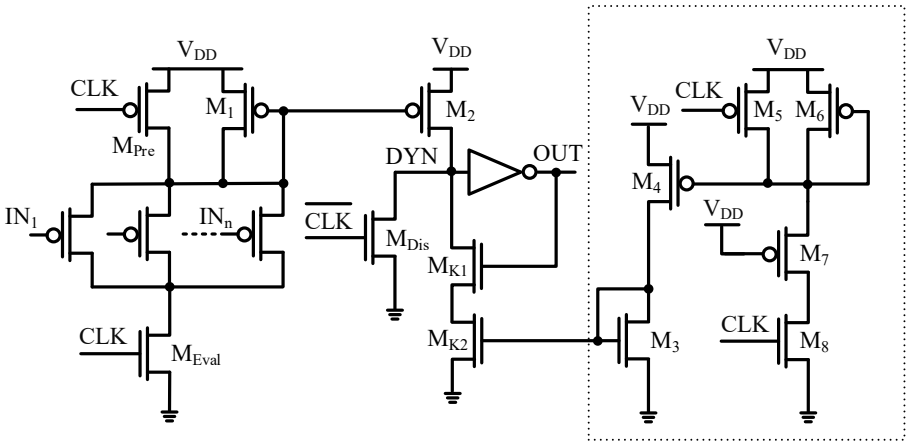


Fig. 5 Current comparison domino logic gate

2.6 Diode footed domino logic gate (DFDLG)

To address leakage in dynamic domino circuits Mahmoodi et al. proposed the DFDLG, as shown in Fig. 6. The architecture employs diode connected footer transistors that generate a negative source bias for PDN during evaluation when the dynamic node remains high. This negative bias introduces an effective negative $V_{GS,}$ elevating the threshold voltage and suppressing subthreshold leakage, thereby enhancing noise immunity. Although a mirror configuration improves operational stability, the additional footer resistance and enlarged device dimensions increase delay and area limiting scalability in-speed wide fan-in designs.

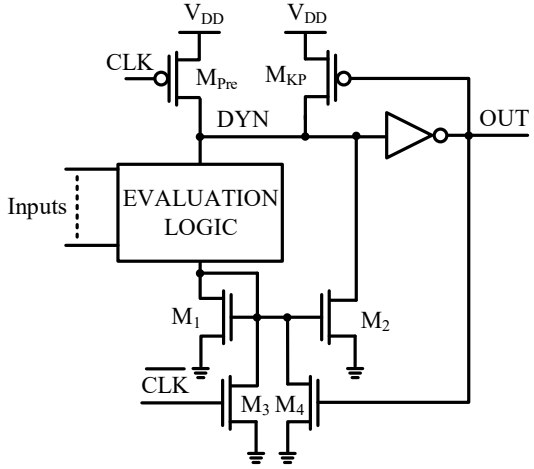


Fig. 6 Diode-Footed Domino logic Gate

2.7 Dual-Operation Input-Dependent Domino Logic Gate (DOINDLG)

Shah et al. DOINDLG [16], shown in Fig. 7, to reduce leakage power in domino logic circuits. The design combines high-threshold-voltage transistors with an NMOS sleep switch to suppress subthreshold leakage effectively. Clock- and input-dependent control signals in the DOIND block regulate the dynamic node during both precharge and evaluation phases, improving leakage robustness. During standby mode, the sleep transistor discharges the

dynamic node, resulting in significant leakage reduction. Simulation results indicate improved tolerance to supply voltage and temperature variations compared to conventional domino logic. However, the inclusion of additional control circuitry and stacked transistors increases design complexity, leading to higher propagation delay, degraded output swing, and increased area overhead. Furthermore, precise generation of control voltages for the DOIND block adds implementation challenges, which may limit scalability in high-speed and wide fan-in designs.

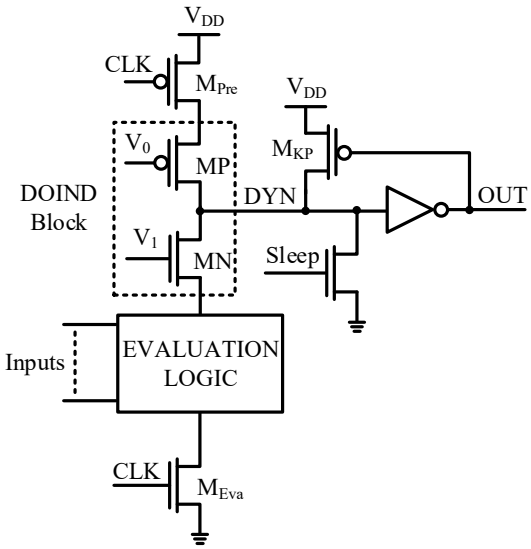


Fig. 7 Dual-Operation Input-Dependent Domino Logic Gate

2.8 Variation resilient keeper-based domino logic gate (VRKDLG)

Kandpal et al. proposed VRKDLG [17], as shown in Fig. 8 to improve the robustness of high-performance dynamic circuit under PVT variations. The technique modifies the conventional keeper structure by adaptively controlling the keeper strength during the evaluation phase thereby reducing unnecessary contention with the pull-down network while maintaining adequate noise immunity. Although the approach enhances stability of the dynamic node particularly at low supply voltages, it introduces additional control circuitry that increases design complexity and area overhead. Further the adaptive keeper operation relies on precise timing and careful transistor sizing making the design sensitive to clock skew and parameter variations. The added keeper path also contributes to increased power consumption and limit scalability for wide fan-in and ultra-high frequency domino logic applications.

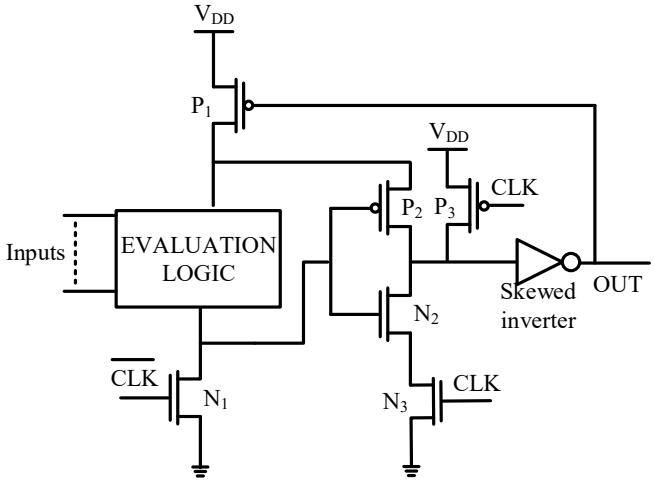


Fig. 8 Variation resilient keeper-based domino logic gate

2.9 Voltage comparison domino Logic gate (VCDLG)

Asyaei *et al.* proposed the VCDLG [18] to improve leakage tolerance in wide fan-in domino circuits as shown in Fig. 9. The key concept of VCDLG is the electrical isolation of the dynamic node from the pull-down network, which prevents leakage current from directly affecting the dynamic node voltage. In place of direct discharge operation, a sense amplifier is used to compare the voltage potential at the upper and lower nodes of the PDN, thereby producing the correct output logic level. This voltage-comparison mechanism ensures reliable evaluation even in the presence of significant leakage currents. Furthermore, limiting the voltage swing at the dynamic node reduces switching power consumption and alleviates charge-sharing effects. However, the inclusion of the sense amplifier increases circuit complexity and area overhead, and also introduces sensitivity to process and supply voltage variations, which can impact overall performance.

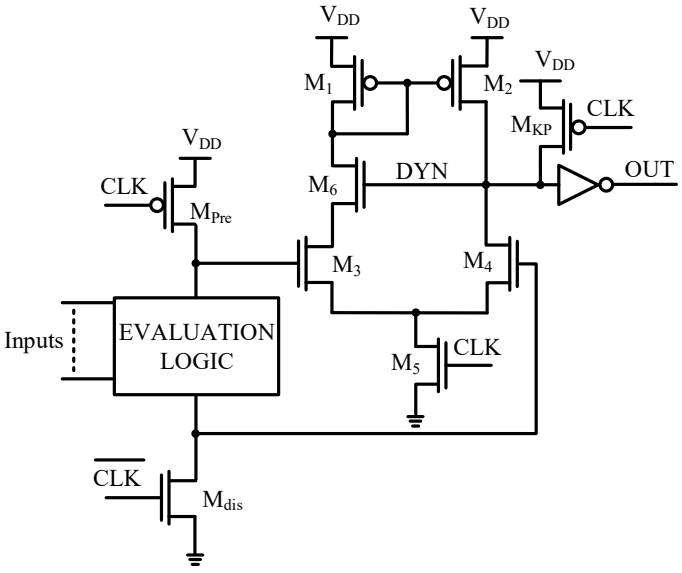


Fig. 9 Voltage comparison domino Logic gate

2.10 Low power domino logic gate (LPDLG)

Asyaei et al. [19] presented a power-efficient scheme for reducing energy consumption in memory bit lines, shown in Fig. 10. The design lowers dynamic power by limiting the voltage swing of the pull-down network, while leakage is suppressed through footer control via an output-driven inverter. Simulation results show significant power reduction and improved noise immunity. However, the approach has limitations, as gate performance may degrade for high fan-in scenarios, and additional control circuitry increases design complexity.

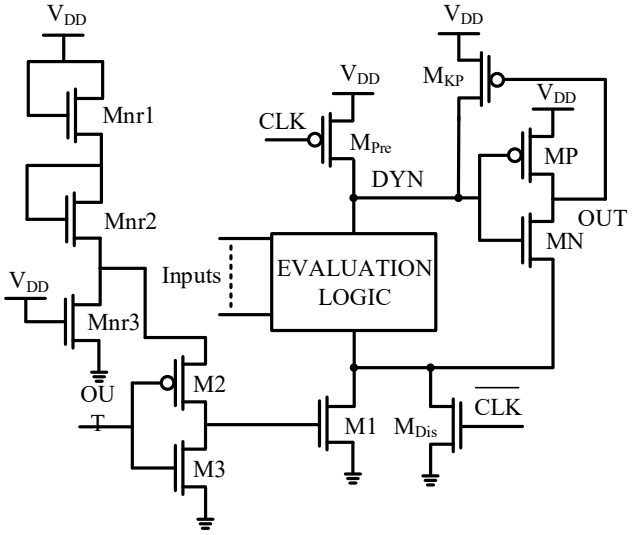


Fig. 10 Low power domino logic gate

2.11 Foot driven stack transistor domino logic gate (FDSTDLG)

Garg et al. [20] presented the FDSTDLG architecture to restrict leakage-induced discharging of the dynamic node in wide fan-in domino logic circuits realized in deep-submicron CMOS technology, as shown in Fig. 11. Although stacked NMOS transistors controlled by the output nodes help supress leakage but the design suffers from several drawbacks i.e. the wider footer transistor introduces area overhead reducing suitability for area constrained design. Moreover, the circuit performance is strongly dependent on precise transistor sizing and biasing making the technique sensitive to PVT variations and also the additional stacked devices increase design complexity and may hinder optimization for very high frequency operation.

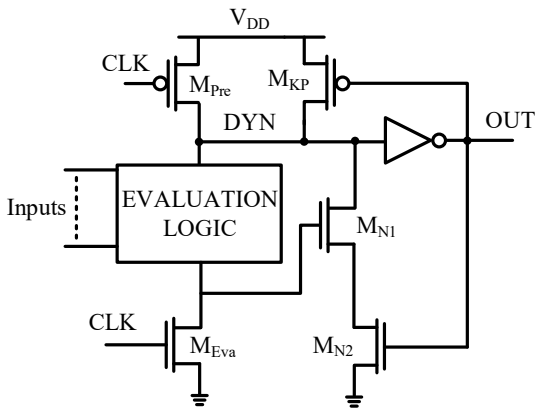


Fig. 11 Foot driven stack transistor domino logic gate

From the above literature survey, it is observed that existing domino logic circuits suffer from increased leakage current, reduced noise immunity and excessive contention current especially in wide fan-in configurations. Therefore, a modified domino logic design is proposed in this work to address these limitations.

3. proposed domino logic circuit

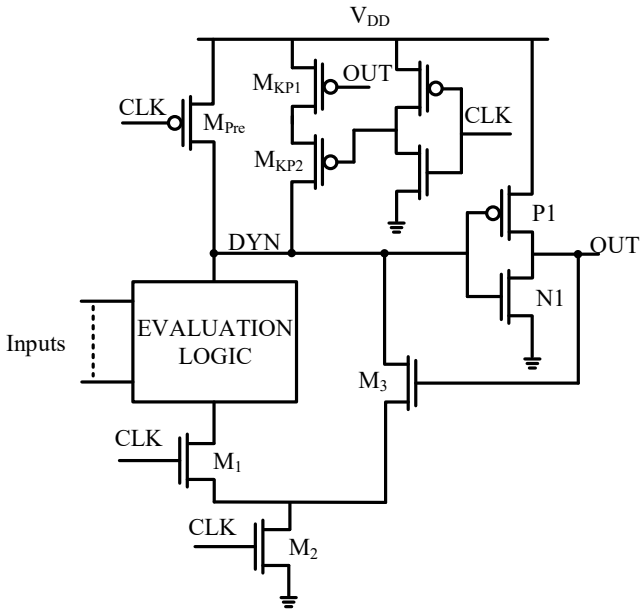


Fig. 12 Circuit-level schematic of the proposed DLG

This paper presents an improved domino logic architecture aimed at minimizing leakage current, reducing contention between the keeper and PDN and enhancing noise immunity while achieving optimized PDP and EDP for wide fan in OR logic as shown in Fig. 12. The proposed circuit operate in two coordinated phases. In the first phase a conditionally controlled keeper network stabilizes the dynamic node and suppresses contention induced power dissipation. In the second phase a modified PDN structure is employed to reduce subthreshold leakage and improve evaluation robustness without incurring excessive delay.

A. Conditional keeper network analysis

In conventional domino logic circuits, a static keeper transistor remains weakly conducting during the evaluation phase irrespective of the conduction state of the PDN. When a valid discharge path is activated, the static behaviour introduces a direct contention current between the keeper and the PDN, leading to unnecessary dynamic power dissipation and degradation in evaluation speed. Further enabling the keeper during the precharge phase is electrically redundant, since the dynamic node is already strongly charged through the precharge transistor.

To mitigate redundant keeper conduction and evaluation phase contention, the proposed domino logic employs a clock and data controlled conditional keeper network. From a device perspective the keeper transistor is enabled only when the dynamic node is susceptible to charge loss due to leakage or noise i.e. during evaluation phase in the absence of an active pull-

down path. When the PDN conducts the keeper is completely disabled thereby eliminating simultaneous current flow between the pull-up and pull-down devices. This selective activation ensures that the keeper provides a restoring current solely to compensate subthreshold leakage and capacitive coupling effects, while avoiding unnecessary current contention during valid evaluation events.

Accordingly, the keeper enable condition is governed by both the clock signal and the conduction state of the PDN and can be expressed as

$$\text{Keeper Enable} = \text{CLK} * \overline{PDN_{ON}} \qquad (6)$$

Where $PDN_{ON} = 1$ denotes the presence of an active discharge path during the evaluation phase

An equivalent voltage domain interpretation of this condition is given by

$$\text{Keeper Enable} = \begin{cases} 1, & \text{if CLK} = 1 \text{ and } V_{DYN} \geq V_{DD} - |V_{TP}| \\ 0 & \text{Otherwise} \end{cases}$$

Which ensures that the keeper supplies a restoring current only when the dynamic node remains charged and is vulnerable to leakage or noise induced disturbances.

The proposed keeper structure is realized using two series connected PMOS transistors, one driven by clock signal and the other controlled by the inverter output of the dynamic node. During the evaluation phase if no valid PDN discharge path exists the dynamic node remains near V_{DD}, enabling the keeper to supply a restoring current that compensates for leakage and noise induced charge loss. Conversely when the PDN conducts the dynamic node voltage falls below V_{DD} - V_{TP}, forcing the data-controlled keeper transistor into cutoff and completely disabling the keeper during legitimate discharge events.

Accordingly, the effective keeper current in the proposed design is given by

$$I_{keeper,prop} = \begin{cases} I_{keeper}, & PDN_{ON} = 0 \\ 0, & PDN_{ON} = 1 \end{cases}$$

This conditional operation eliminates keeper-PDN contention during valid evaluation, such that the average contention current satisfies

$$I_{cont,prop} < I_{cont,conv} \qquad (8)$$

As a result, the contention related dynamic power dissipation is significantly reduced without compromising functional correctness. In addition, by supplying restoring current only in the absence of PDN conduction the proposed keeper enhances dynamic node stability against leakage and noise disturbances, thereby improving noise immunity while preserving evaluation speed. These characteristics make the conditional keeper network particularly suitable for wide fan-in domino logic applications.

B. Modified Pull-Down Network Architecture

The proposed domino logic circuit incorporates a modified PDN to suppress subthreshold leakage current and enhance evaluation phase robustness while maintaining high speed operation. In conventional footed domino logic, the evaluation network is connected to ground

through a single NMOS footer transistor, which provides a low resistance discharge path during evaluation but exhibits significant leakage and reduced noise tolerance due to the absence of stacking effects.

To address these limitations the proposed design adopts a stacked footer PDN topology, in which two NMOS transistors M_1 and M_3 form parallel evaluation path connected in series with a footer transistor M_2. During the evaluation phase the precharge transistor is turned OFF and the dynamic node is conditionally discharge through

$$\text{DYN} \rightarrow \text{Evaluation Logic} \rightarrow (\text{M1} \parallel \text{M3}) \rightarrow \text{M2} \rightarrow \text{GND}.$$

The series connected footer transistor M2 plays a key role in leakage suppression. When the PDN is idle or weakly conducting, leakage induced voltage division along the stacked pull-down path raises the source potential of the upper pull-down transistors, introducing a nonzero source-body voltage (V_{SB})[16,23]. This source bias activates the body effect thereby increasing the effective threshold voltage of the pull-down devices, which can be expressed as

$$V_{TH,eff} = v_{TH0} + \gamma\left(\sqrt{\phi + v_{sB}} - \sqrt{\phi}\right). \qquad (9)$$

As a result, the subthreshold leakage current is exponentially suppressed since it follows [7]

$$I_{sub}\alpha\ exp\left(\frac{V_{GS}-V_{TH,eff}}{\eta V_T}\right) \qquad (10)$$

As a result, the increased effective threshold voltage significantly lower subthreshold leakage current which improves dynamic node charge retention and strengths resistance to leakage induced discharge.

Although the insertion of M2 increases the pull-down resistance, the parallel transistor M3 is intentionally introduced to mitigates the associated delay penalty. By providing an additional discharge path during valid evaluation events, M3 reduces the effective resistance of the PDN without negating the leakage suppression achieved by stacking. The equivalent pull-down resistance can be approximated as

$$R_{eq} \approx (R_{M1}||R_{M3}) + R_{M2}. \qquad (11)$$

Since ($R_{M1} \parallel R_{M3}$) < R_{M1}, the inclusion of M_3 significantly improves evaluation speed particularly for wide fan-in logic where discharge paths are inherently slow. Importantly leakage suppression remains governed by the stacked transistor M_2, ensuring that the addition of M_3 does not compromise leakage reduction or noise immunity.

Accordingly, the evaluation delay of the proposed DLG can be approximated using a first-order RC model:

$$t_{eval} \approx R_{eq}.C_{DYN} \qquad (12)$$

By combining a conditionally activated keeper network with a leakage suppressing yet delay compensated PDN the proposed domino logic architecture achieves a favorable trade-off

among leakage current reduction, noise immunity enhancement and evaluation speed making it well suited for wide fan-in high performance dynamic logic applications.

The key novelty of the proposed domino logic circuit is summarized as follows:

- ❖ A clock and data dependent conditional keeper network that completely suppresses keeper-PDN contention during valid discharge events, thereby significantly reducing contention power while preserving dynamic node stability
- ❖ A leakage aware pull-down network architecture employing a stacked footer transistor with parallel evaluation path, which supresses subthreshold leakage through body-effect induced threshold voltage modulation without incurring a substantial evaluation delay penalty.
- ❖ An optimized trade-off among power efficiency, noise immunity and speed resulting in improved PDP and EDP, making the proposed architecture well suited for wide fan-in OR domino logic applications.

3.1 Operation of the proposed domino logic gate (DLG)

The proposed DLG operates in two distinct phases namely the precharge phase and the evaluation phase, similar to conventional domino logic. Throughout this discussion logic high (‘1’) and logic low (‘0’) correspond to supply voltage V_{DD} and ground respectively. The proposed circuit implements a wide fan-in OR logic function for which the input controlled NMOS transistor in PDN are connected in parallel followed by the modified footer structure describe earlier.

- Precharge Phase

During the precharge phase the clock signal CLK is at logic ‘0’ and its complements is at logic ‘1’. Under this condition the precharge PMOS transistor is turned ON, charging the dynamic node (DYN) to V_{DD}, while all NMOS transistors in the PDN remain OFF, thereby isolating the DYN from the ground path. As a result, the output of the inverter is driven to logic ‘0’. In the proposed architecture the conditional keeper network remains completely disabled during this phase, which prevent any redundant current flow or contention with the precharge device. Consequently, the dynamic node and output node settle at logic ‘1’ and logic ‘0’ respectively at the end of the precharge phase.

- Evaluation Phase

During the evaluation phase, CLK transition to logic ‘1’ and $\overline{CLK}$ to logic ‘0’, turning OFF the precharge transistor and enabling conditional evaluation of the DYN based on the applied inputs. Two operating conditions arise during this phase.

Condition-I (No discharge path):

When all input signals applied to the PDN are at logic ‘0’, no valid path exists between the DYN and ground. The DYN therefore retains its precharge voltage level. Under this condition, the conditional keeper network is enabled and supplies a weak restoring current to compensate for leakage or noise induced charge loss, thereby maintaining the DYN at logic ‘1’. As aresult the inverter output remain at logic ‘0’.

Condition-II (Valid discharge path):

When at least one input to the PDN is at logic ‘1’, a valid discharge path is established. The DYN begins to discharge through the parallel evaluation transistors and the stacked footer network. As the DYN voltage decreases, the inverter output transitions to logic ‘1’, which disable the conditional keeper. This prevents contention between the keeper and the PDN during legitimate discharge events. The parallel evaluation path ensures sufficient discharge current, while the stacked footer suppresses leakage during weak conduction. Consequently, the DYN and output node settle at logic ‘0’ and logic ‘1’, respectively.

The output response of the suggested domino gate is investigated using transient simulation in order to confirm the 32-bit OR capability shown in Fig. 14. The assessment is carried out in the worst-case scenario i.e. only one PDN transistor is triggered by a logic high input during the evaluation phase, while all PDN transistor input are maintained at logic low during the precharge phase to reflect the most crucial operating situation.

Overall, the proposed operation ensures correct OR logic functionality while effectively suppressing keeper-PDN contention, improving noise immunity and maintaining controlled evaluation speed even for wide fan-in configurations.

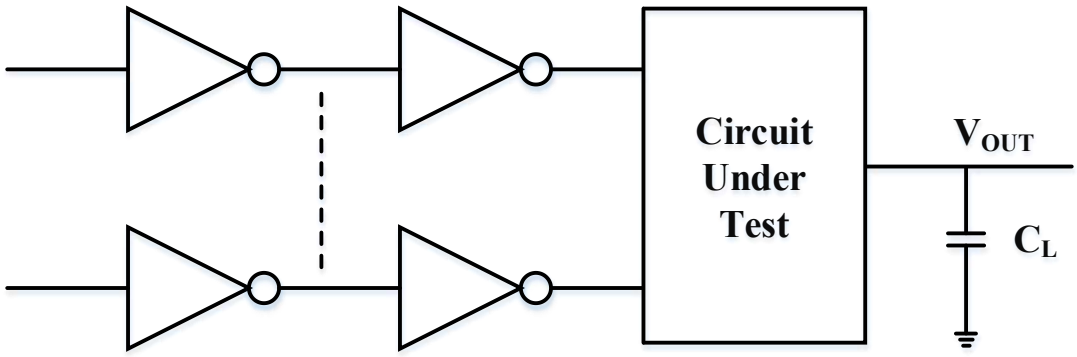


Fig.13 Simulation Framework [24]

4. simulation results and comparison

The proposed domino logic circuits were designed and evaluated using the Cadence Virtuoso simulation environment based on a 90-nm CMOS process technology. All simulations were performed with a supply voltage of 1 V under nominal conditions. To model practical loading scenarios a load capacitance of 5 fF was used and the clock frequency was fixed at 1 GHz. The corresponding simulation testbench is shown in Fig. 13. An OR gate configuration was chosen for performance analysis as it is widely adopted for evaluating dynamic logic circuits. Performance metrics were extracted under identical simulation conditions to ensure a fair and consistent comparison with previously reported domino logic design.

The simulation methodology adopted in this work follows the configuration reported in [24]. In this setup all input signal are applied through buffer stages to emulate realistic operating conditions. The propagation delay is measured from the input to the output under worst case

timing conditions. This simulation framework is widely accepted for evaluating the performance of domino logic circuits. In addition to delay multiple metrics are considered to assess the functional correctness, robustness and noise immunity of the proposed design. The definition of these evaluation metrics is presented in the following subsection.

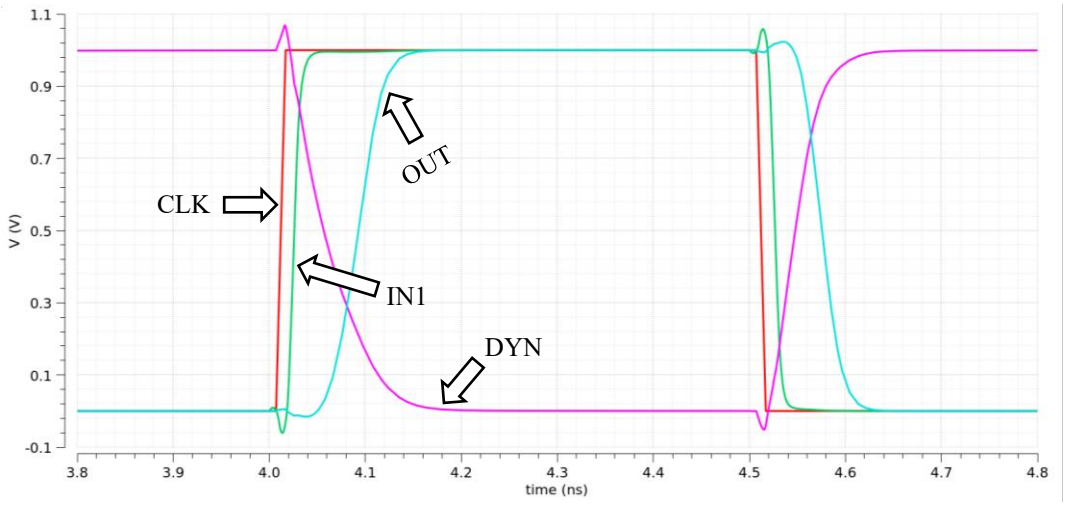


Fig. 14 Transient output characteristics of the 32-input OR gate implemented with the proposed design.

4.1 transistor sizing

Optimizing an individual design parameter in dynamic domino logic circuits typically involves trade-off among multiple performance metrics. For example, enlarging the keeper transistor improve noise immunity but simultaneously increases contention with the PDN during evaluation, which adversely affects propagation delay and power dissipation. Therefore, uniform transistor upsizing is not an efficient optimization approach when overall performance is assessed using a comprehensive FOM. In this study all transistors are initially sized to their minimum allowable dimensions to establish a consistent baseline, after which only a limited set of transistors critical to circuit performance is selectively resized to achieve a balanced compromise among speed, power consumption and robustness. In the proposed design noise immunity is enhanced through controlled sizing of the keeper transistor while delay reduction is achieved by appropriately sizing the PMOS device of the output inverter to improve output signal restoration. This selective sizing strategy ensures that improvements in one performance metric do not excessively degrade others, thereby enabling a fair comparison with existing domino logic architectures. The channel length of all transistors is fixed at L_{min} = 90 nm, the initial width is set to $W_{min} = 3L_{min}$ and selectively adjusted to meet the desired performance objectives and the PMOS to NMOS width ratio of all output inverters is maintained at 2. The transistor sizing parameters used in the proposed architecture are presented in Table 1.

Table 1. Transistor dimensions used in the proposed circuit for 8, 16, 32 and 64-input OR gates

Fan-in (delay)	W_{pre}	W_{Evl}	W_{M1}	W_{M2}	W_{M3}	W_{KP1}	W_{KP2}	W_{P1}	W_{N1}
8-in (90ps)	6Lmin	3Lmin	3Lmin	3Lmin	5Lmin	3Lmin	8Lmin	8Lmin	4Lmin

16-in (100ps)	6Lmin	3Lmin	3Lmin	3Lmin	5Lmin	3Lmin	8Lmin	8Lmin	4Lmin
32-in (110ps)	6Lmin	3Lmin	3Lmin	3Lmin	7Lmin	3Lmin	8Lmin	10Lmin	5Lmin
64-in (120ps)	6Lmin	3Lmin	5Lmin	3Lmin	8Lmin	3Lmin	8Lmin	10Lmin	5Lmin

4.2 propagation delay (t_p)

The parameter t_p quantifies gate speed by specifying the time elapsed from an input transition to the resulting output transition [4]. In this work delay is evaluated during the evaluation phase under the worst-case condition where a single pull-down network (PDN) transistor is active. The delay is calculated as the average of the rising and falling transition time measured at the 50% voltage level, expressed as

$$t_p = \frac{t_{pHL} + t_{pLH}}{2} \qquad (13)$$

where t_{pHL} and t_{pLH} denotes the propagation delays measured between the input and output signals at the 50% voltage level during high-to-low and low-to-high output transitions respectively.

4.3 Average power consumption (P_{Avg})

The P_{Avg} of the gate is determined using transient simulation. The circuit is driven by a 1 GHz clock and analyzed over ten successive clock periods. To ensure robust validation of the proposed design the power measurement is performed under worst case switching conditions. The formulation used to calculate P_{avg} is presented in Eq. (2).

Table.2 P_{Avg} and its normalized counterpart are evaluated for the proposed and existing DLG under identical delay conditions.

Fan-in (delay)		SFDLG [7]	DFDLG [3]	HSDLG [12]	VCDLG [18]	VRKDLG [17]	DOINDLG [16]	FDSTDLG [20]	LPDLG [19]	LVNIDLG [22]	PROPOSED
8-in (90ps)	P_{Avg}(µW)	17.016	18.931	26.460	27.489	17.071	25.965	12.809	14.503	16.779	11.071
	Normalized PAvg	1	1.112	1.555	1.615	1.003	1.525	0.752	0.852	0.986	0.650
16-in (100ps)	P_{Avg}(µW)	21.127	23.189	27.548	29.378	18.103	33.353	15.720	15.872	17.880	12.808
	Normalized PAvg	1	1.097	1.303	1.390	0.856	1.578	0.744	0.751	0.846	0.606
32-in (110ps)	P_{Avg}(µW)	29.216	31.960	31.729	33.976	22.130	38.304	20.592	18.664	23.106	15.611
	Normalized PAvg	1	1.093	1.086	1.162	0.757	1.311	0.704	0.638	0.790	0.534
64-in (120ps)	P_{Avg}(µW)	51.731	52.010	36.454	36.832	30.959	42.002	31.838	23.837	35.981	21.316
	Normalized PAvg	1	1.005	0.704	0.711	0.598	8.11	0.615	0.460	0.695	0.412

4.4 Noise immunity

Various metrics have been proposed to assess the noise tolerance of dynamic logic circuits [16,18,19]. Among them Unity Noise Gain (UNG) is commonly used to compare the robustness of dynamic gates [3,10,13,20-23]. UNG represents the input noise amplitude that results in an output noise pulse with an equal peak value [18]. Although the input disturbance

can be controlled by modifying the pulse amplitude or width, UNG does not capture the effect of the output pulse duration.

To address this limitation this work employs the Unity Noise Gain Average (UNA) metrics [16]. UNA represents the input noise amplitude at which the average output noise voltage equals the corresponding average input noise voltage and can be expressed as

$$UNA = \{Vin : V_{noise,avg} = V_{out,avg}\} \quad (14)$$

For fair comparison the input noise amplitude is increased under worst-case conditions until this equality is achieved. The worst-case operating condition of an OR gate is observed when identical noise disturbances are simultaneously imposed on all inputs in the evaluation phase.

Table.3 UNA and its normalized counterpart are evaluated for the proposed and existing DLG under identical delay conditions.

Fan-in (delay)		SFDLG [7]	DFDLG [3]	HSDLG [12]	VCDLG [18]	VRKDLG [17]	DOINDLG [16]	FDSTDLG [20]	LPDLG [19]	LVNIDLG [22]	PROPOSED
8-in (90ps)	UNA(V)	0.468	0.685	0.368	0.703	0.686	0.564	0.601	0.506	0.637	0.723
	Normalized UNA	1	1.463	0.786	1.502	1.465	1.205	1.284	1.081	1.361	1.544
16-in (100ps)	UNA(V)	0.460	0.674	0.352	0.682	0.659	0.532	0.564	0.468	0.613	0.702
	Normalized UNA	1	1.465	0.765	1.482	1.432	1.156	1.226	1.017	1.332	1.526
32-in (110ps)	UNA(V)	0.426	0.628	0.339	0.673	0.649	0.502	0.534	0.439	0.576	0.696
	Normalized UNA	1	1.474	0.795	1.579	1.523	1.178	1.253	1.030	1.352	1.633
64-in (120ps)	UNA(V)	0.382	0.580	0.327	0.666	0.636	0.489	0.467	0.407	0.518	0.680
	Normalized UNA	1	1.518	0.856	1.743	1.664	1.280	1.222	1.065	1.356	1.780

4.5 Figure of merit

To comprehensively compare the proposed circuit with existing designs a Figure of Merit (FOM) is employed that simultaneously accounts for noise immunity, power consumption, delay and layout area. Since noise pulse width plays a critical role in dynamic logic the UNA is adopted as the noise robustness metric. The FOM is defined as

$$FOM = \frac{UNA_{norm}}{P_{avg,norm}\ X\ t_{p,norm}^{2}\ X\ A_{norm}} \quad (15)$$

Where UNA_{norm}, P_{avg},$t_{p,norm}$ and A_{norm} represent the normalized unity noise gain , average power consumption, propagation delay and layout estimated area respectively. All parameters are normalized with respect to the corresponding SFDL implementation to enable fair comparison.

Layout extracted area is used to reflect practical design constraints and process corner simulations are performed to evaluate robustness under variations. Since the circuit area remains unchanged across process corners the variation in FOM is primarily influenced by changes in UNA and the power delay product. The maximum FOM is observed at the favorable process corner confirming the effectiveness of the proposed design under worst case operating condition.

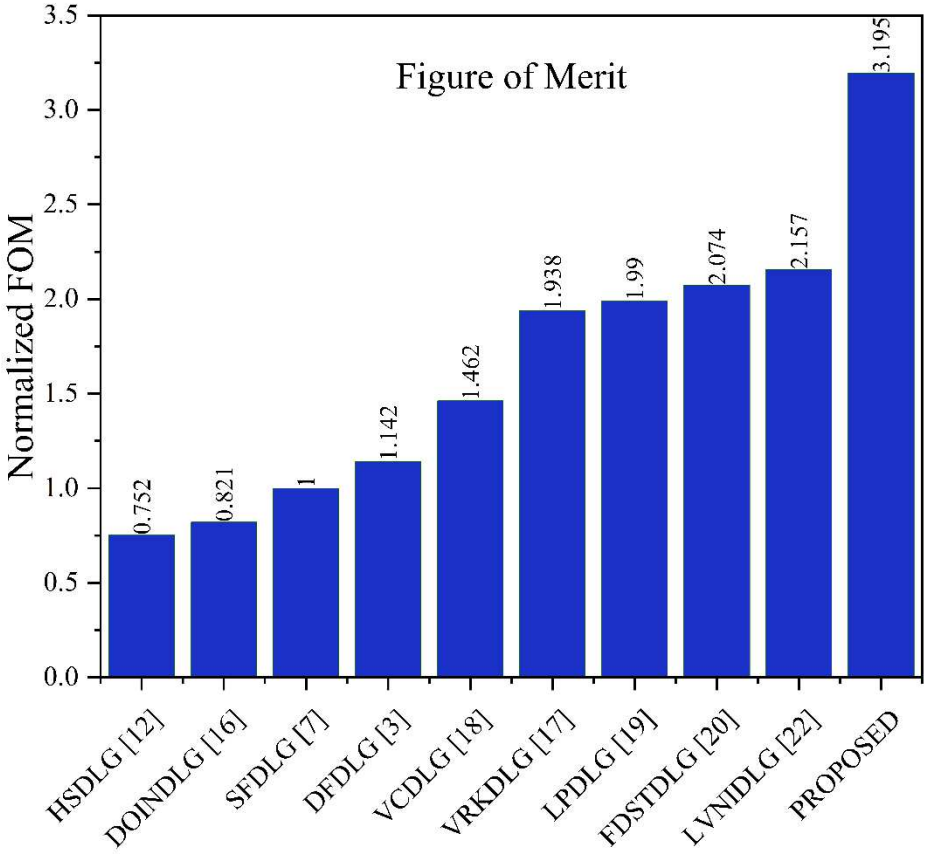


Fig. 15. Normalized FOM of various reported DLG compared with the proposed 32- input design

Table.4 The normalized standard deviation of P_{Avg} and delay for the proposed and reference DLG assessed under identical delay conditions.

Fan-in (delay)		SFDLG [7]	DFDLG [3]	HSDLG [12]	VCDLG [18]	VRKDLG [17]	DOINDLG [16]	FDSTDLG [20]	LPDLG [19]	LVNIDLG [22]	PROPOSED
8-in (90ps)	σ_{PAvg}	1.00	0.91	0.93	0.92	0.94	1.11	0.97	0.98	0.92	0.91
	σ_{Delay}	1.00	0.98	0.95	0.93	0.96	1.02	0.96	0.95	0.95	0.90
16-in (100ps)	σ_{PAvg}	1.00	0.96	0.92	0.95	0.95	0.99	0.99	0.97	0.90	0.89
	σ_{Delay}	1.00	0.99	0.95	0.93	0.97	0.97	0.93	0.94	0.93	0.87
32-in (110ps)	σ_{PAvg}	1.00	0.90	0.90	0.91	0.92	0.95	0.92	0.91	0.87	0.82
	σ_{Delay}	1.00	0.88	0.93	0.96	0.90	0.98	0.90	0.93	0.89	0.83
64-in (120ps)	σ_{PAvg}	1.00	0.83	0.87	0.84	0.87	0.92	0.87	0.90	0.85	0.79
	σ_{Delay}	1.00	0.80	0.89	0.89	0.90	0.95	0.89	0.88	0.88	0.82

4.6 Power Delay Product (PDP)

PDP is a commonly used metrics for jointly evaluating power consumption and speed in logic circuits []. In dynamic and domino logic PDP represents the energy dissipated during a single evaluation event and is defined as

$$PDP = P_{Avg} * t_p \qquad (16)$$

PDP provides an effective means to assess the energy efficiency of DLG while accounting for their timing behavior.

4.7 Energy Delay Product (EDP)

The EDP further incorporates the impact of delay by weighting timing performance more strongly and is defined as

$$EDP = P_{Avg} * t_p^2 \qquad (17)$$

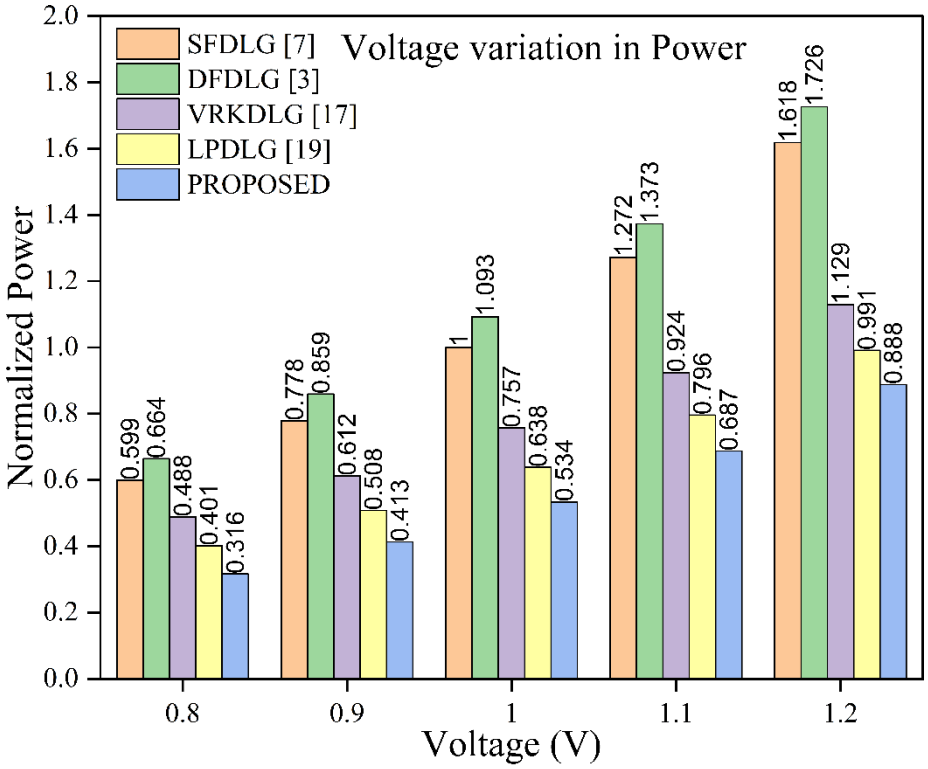
EDP is particularly useful for evaluating wide fan-in domino logic, where increased evaluation path resistance and parasitic capacitances result in pronounced delay variations across different circuit topologies.

Table 5. Evaluation of normalized PDP and EDP for the proposed and reference DLG.

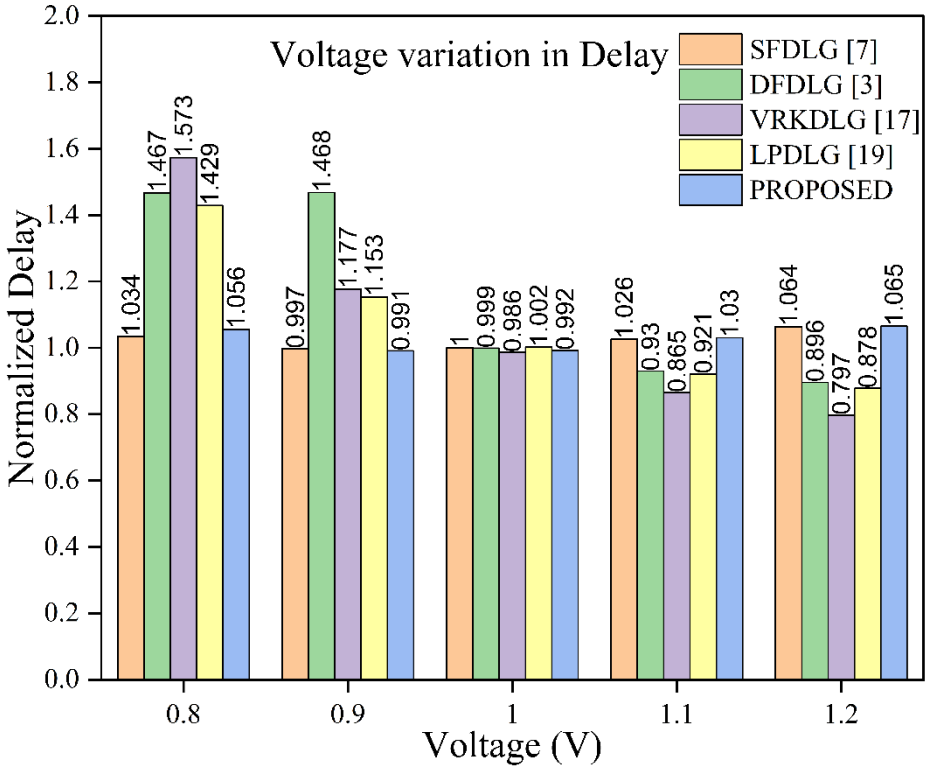
Fan-in (delay)		SFDLG [7]	DFDLG [3]	HSDLG [12]	VCDLG [18]	VRKDLG [17]	DOINDLG [16]	FDSTDLG [20]	LPDLG [19]	LVNIDLG [22]	PROPOSED
8-in (90ps)	PDP	1	1.162	1.593	1.655	1.024	1.508	0.779	0.870	1.005	0.662
	EDP	1	1.214	1.633	1.695	1.046	1.530	0.804	0.887	1.026	0.675
16-in (100ps)	PDP	1	1.141	1.384	1.528	0.938	1.913	0.803	0.836	0.918	0.686
	EDP	1	1.188	1.470	1.680	1.027	2.070	0.867	0.931	0.997	0.776
32-in (110ps)	PDP	1	1.093	0.977	1.155	0.740	1.442	0.706	0.640	0.789	0.530
	EDP	1	1.093	0.879	1.148	0.724	1.436	0.707	0.642	0.790	0.525
64-in (120ps)	PDP	1	0.992	0.701	0.709	0.593	0.865	0.605	0.418	0.697	0.409
	EDP	1	0.982	0.700	0.710	0.590	0.843	0.597	0.416	0.701	0.408

Table 6. Performance evaluation of the proposed gate in comparison with SFDL [7], DFDLG [3] LPDG [19] and VRKDG [17] for 32-bit inputs

Parameter	SFDLG [7]	DFDLG [3]	LPDLG [19]	VRKDLG [17]	Proposed
P_{Avg} (µW)	29.216	31.960	18.664	22.130	15.611
P_{leak} (µW)	2.452	3.356	1.634	4.299	1.970
Delay (ps)	110.807	110.795	111.101	108.342	109.055
Normalized delay	1	0.999	1.002	0.977	0.984
UNA (V)	0.426	0.628	0.439	0.649	0.696
Normalized UNA	1	1.474	1.030	1.523	1.633
σ (ps) in delay	11.190	9.847	10.182	10.071	9.287
σ (nW) in P_{avg}	621.971	559.774	565.994	572.214	510.017
Area (μm^2)	271.150	320.212	219.995	281.538	259.489
Normalized area	1	1.180	0.811	1.038	0.841
PDP (fJ)	3.237	3.541	2.073	2.397	1.689
Normalized PDP	1	1.093	0.640	0.740	0.521
EDP ($x10^{-25}$ J.S)	3.587	3.923	2.303	2.597	1.842
Normalized EDP	1	1.093	0.642	0.724	0.513
Normalized FOM	1	1.142	1.990	1.038	3.195

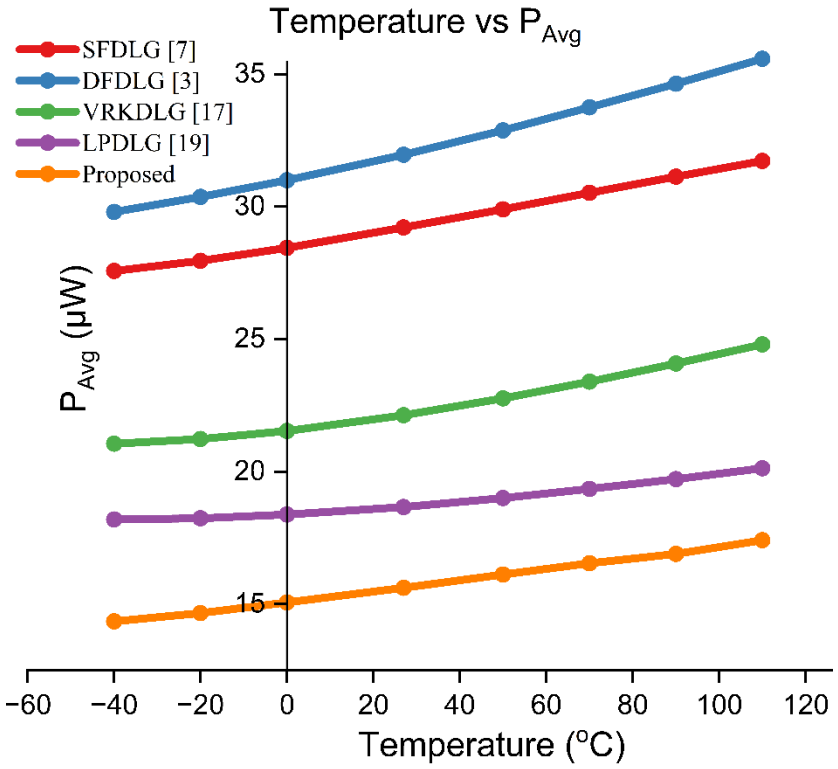

Voltage variation in Power
SFDLG [7]
DFDLG [3]
VRKDLG [17]
LPDLG [19]
PROPOSED
Normalized Power
Voltage (V)
0.8
0.9
1
1.1
1.2
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
0.599
0.664
0.488
0.401
0.316
0.778
0.859
0.612
0.508
0.413
1
1.093
0.757
0.638
0.534
1.272
1.373
0.924
0.796
0.687
1.618
1.726
1.129
0.991
0.888

(a)

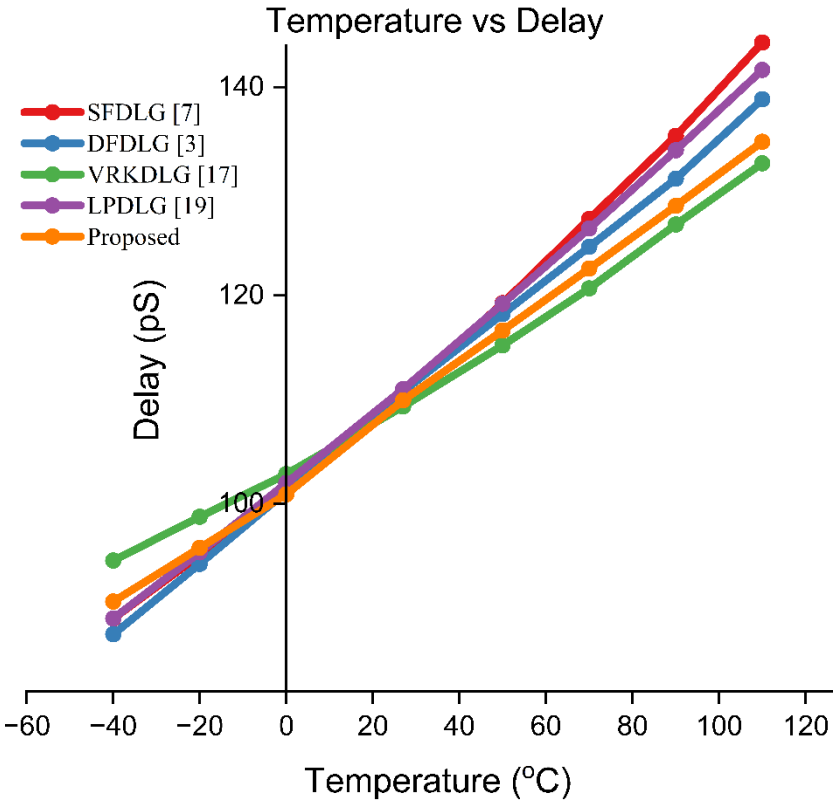

Voltage variation in Delay
SFDLG [7]
DFDLG [3]
VRKDLG [17]
LPDLG [19]
PROPOSED
Normalized Delay
Voltage (V)
0.8
0.9
1
1.1
1.2
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
1.034
1.467
1.573
1.429
1.056
0.997
1.468
1.177
1.153
0.991
1
0.999
0.986
1.002
0.992
1.026
0.93
0.865
0.921
1.03
1.064
0.896
0.797
0.878
1.065

(b)

Fig. 16. Comparative analysis of (a) normalized power and (b) normalized delay at various supply voltages for the proposed 32- bit DLG and existing designs (SFDL [7], DFDLG [3], LPDG [19], VRKDG [17]).

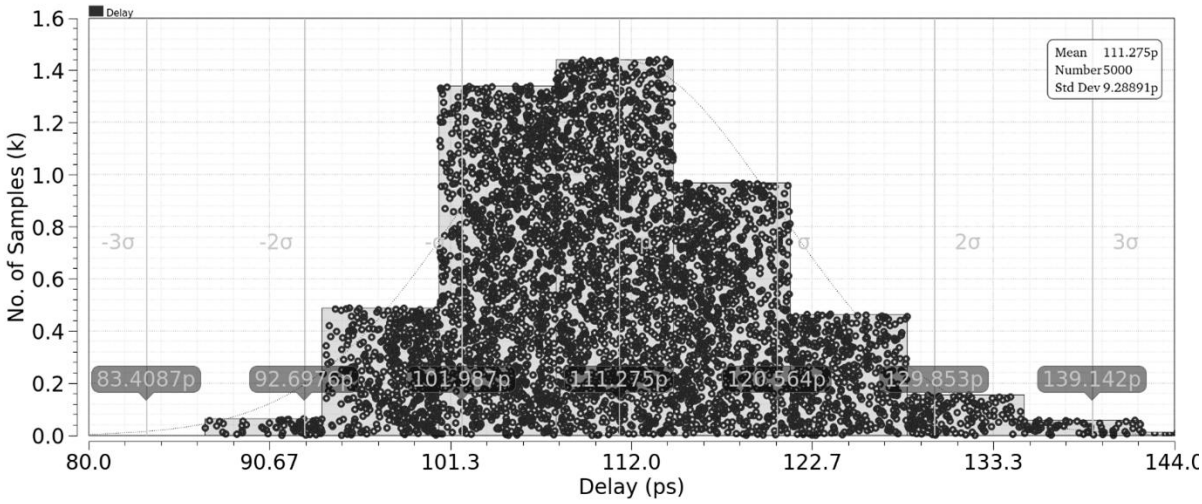


(a)

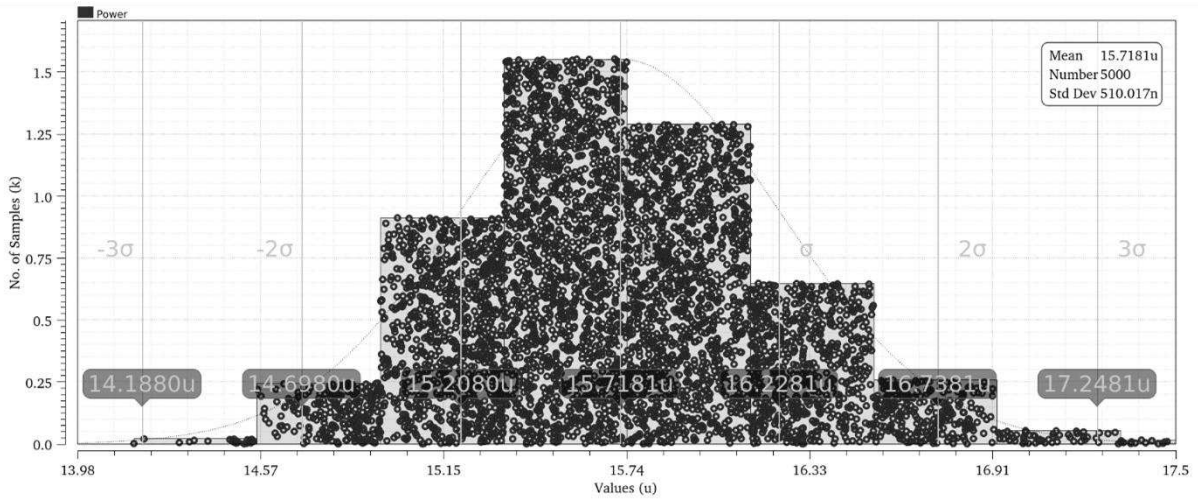


(b)

Fig. 17. Temperature dependent variation of (a) P_{Avg} and (b) delay for the proposed 32-bit DLG and existing designs (SFDL [7], DFDLG [3], LPDG [19], VRKDG [17]) at 32-bit input against temperature.



(a)



(b)

Fig. 18. Monte Carlo simulation results for the proposed gate at 32-bit input: (a) Delay distribution and (b) power distribution.

The measured P_{Avg} of the proposed DLG and the reference designs for different fan-in configuration is reported in Table 2. For a fair comparison all values are normalized with respect to the SFDLG [7]. The normalized results indicate a consistent reduction in P_{Avg} for the proposed design across all fan-in cases. In particular the proposed DLG achieves an average power reduction of approximately 46% compare to SFDLG [7], about 31% relative to VRKDLG [17] and about 19% relative to LPDLG [19].

The observed reduction in power consumption can be directly attributed to the combined effect of the conditional keeper network and modified PDN architecture. The clock and data-controlled keeper eliminate unnecessary keeper-PDN contention during valid evaluation events, thereby suppressing contention induced dynamic power dissipation. In addition, the stacked footer transistor in pull-down path effectively reduces subthreshold leakage through body effect induced threshold voltage modulation. The parallel evaluation path further limits excessive discharge resistance while preserving leakage suppression. Together these mechanisms reduce charge sharing and unnecessary switching activity at the dynamic node, which collectively contribute to the reduction in P_{Avg}.

The UNA values obtained for the proposed DLG and the reference designs under different fan-in conditions are summarized in Table 3. For consistency all UNA values are normalized with respect to the SFDG []. The normalized results indicate a clear improvement in noise immunity for the proposed design across all fan-in configurations. Specifically, the proposed DLG exhibits UNA values that are approximately 1.554 to 1.780 higher than SFDLG [7], 1.05 to 1.07 times higher than VRKDLG [17] and 1.38 to 1.67 times higher than LPDLG [9].

The observed enhancement in UNA can be attributed to the combined influence of the conditional keeper network and the modified PDN. The selectively activated keeper supplies a restoring current only when the PDN is inactive, thereby improving dynamic node charge retention in the presence of noise disturbances without introducing contention during valid evaluation. In addition, the stacked footer structure suppresses leakage induced voltage

degradation at the dynamic node, while the parallel evaluation path ensures controlled discharge behavior. These mechanisms collectively stabilize the dynamic node voltage during evaluation resulting in improved noise immunity and higher UNA values for the proposed DLG.

The FOM values for the proposed DLG and the reference designs under a 32-input configuration are presented in Fig. 15. For comparative clarity all FOM values are normalized with respect to the SFDLG [7]. The silicon area of each DLG is obtained from post-layout implementation, ensuring accurate estimation of the physical footprint. The extracted layout area is incorporated into the FOM calculation to enable a realistic and fair performance comparison among the considered designs.

As shown Fig.15, the proposed DLG demonstrates a significant improvement in FOM compare to the existing designs. specifically, the proposed architecture achieves an improvement of approximately 3.2x compared to SFDLG [7], 1.648x compared to VRKDLG [17] and also 1.605x compared to LPDG [19]. These results indicate the superior efficiency of the proposed design when both performance and are area jointly considered. The improvement in FOM is primarily attributed to the redesigned conditional keeper and modified footer based PDN, which together reduce power dissipation and improve robustness without incurring a significant area overhead.

To quantify sensitivity to process variations, the standard deviation of propagation delay and P_{avg} was extracted for both the proposed and existing DLG. These values were normalized with respect to the SFDLG [7] and are reported in Table 4. A Monte Carlo analysis with 5000 iterations was performed to statistically capture the effects of random process fluctuations on circuit performance. The results in Table 4 indicates a noticeable reduction in process-induced variations for the proposed design. Specifically, the proposed DLG exhibits approximately 17% and 8% lower delay variation and about 18% and 10% lower PAvg variation compared to SFDLG [7] and LPDLG [19], respectively.

The improved robustness against process variations arises from the combined effect of the conditional keeper network and the modified pull-down architecture. Selective keeper activation stabilizes the dynamic node during evaluation in the absence of a valid discharge path, while the stacked footer structure suppresses leakage induced fluctuations through body effect-enhanced threshold modulation. Together these mechanisms reduce sensitivity to device parameter variations, thereby improving the reliability and robustness of the proposed DLGunder PVT variations.

The PDP and EDP obtained for the proposed DLG and the reference designs under different fan-in configurations are summarized in Table 5. For a fair comparison, all the PDP and EDP values are normalized with respect to the SFDLG [7]. The normalized results demonstrate a consistent improvement in both PDP and EDP for the proposed design across all fan-in conditions, indicating enhanced energy efficiency without sacrificing evaluation speed.

The reduced PDP is mainly due to lower average power under identical delay conditions. The clock and data controlled conditional keeper minimizes keeper-PDN contention, while the stacked footer PDN suppresses subthreshold leakage. The parallel evaluation path offsets the

increased pull-down resistance resulting in negligible delay degradation and a lower PDP than existing designs.

The improved EDP reflects reduced energy consumption with controlled evaluation delay. Leakage induced dynamic node degradation and unnecessary switching are minimized while the optimized PDN maintains sufficient discharge strength for wide fan-in operation. Consequently, the proposed DLG outperforms SFDLG [7] and VRKDLG [17] in EDP, demonstrating its effectiveness for energy efficient high-performance wide fan-in domino logic.

The evaluation of stability, reliability and robustness in domino logic circuits requires careful consideration of PVT variations. To assess the impact of these variations, the proposed DLG and selected reference designs were simulated for different fan-in configurations under identical delay conditions, with Monte Carlo analysis used to extract the statistical variations (standard deviation) of delay and average power.

To evaluate sensitivity to supply voltage variations, the P_{Avg} and delay of the proposed and selected reference DLG were analyzed for a 32-input configuration across a range of supply voltages. The corresponding delay and power characteristics normalized with respect to SFDG [7], are illustrated in Fig. 16. The proposed DLG consistently exhibits lower P_{Avg} and reduced delay than conventional design over entire voltage range. This improved voltage robustness is primarily attributed to the conditional operation of the keeper network, which avoid partial conduction and contention during evaluation.

Furthermore, the impact of temperature variation was evaluated by analyzing the P_{Avg} and delay of the proposed and selected reference DLG over a wide temperature range, as shown in Figs. 17. The proposed design exhibits minimal sensitivity to temperature changes. This enhanced thermal stability is attributed to controlled keeper switching activity and improved dynamic node stability which together limit leakage-induced fluctuations and excessive contention across the operating temperature range.

A comprehensive comparison of key performance metrics for the proposed and selected reference DLG is presented in Table 6. The results indicate that the proposed design exhibits improved stability, reliability and robustness under the combined effects of PVT variations when compared with SFDLG [7], DFDLG [3], LPDLG [19] and VRKDLG [17].

The enhanced PVT tolerance of the proposed DLG can be attributed to the redesigned conditional keeper network and the modified footer based pull-down structure, which together stabilize the dynamic node and suppress variation induced leakage and contention. To further quantify robustness, the standard deviation of propagation delay and P_{Avg} was extracted using a Monte Carlo simulation with 5000 iterations. The resulting distributions for delay and P_{Avg} are illustrated in Figs. 18(a) and 18(b), confirming the reduced sensitivity of the proposed design to process-induced variations.

5. Wide Fan-In Multiplexer design

Wide fan-in multiplexers are critical components in memory read path and are commonly employed in bit-line selection circuitry [19,25]. However, such circuits typically suffer from high power consumption due to the large switching capacitance associated with wide fan-in structures, where dynamic power dominates because of frequent read and write operations. These challenges are further exacerbated in large capacity memories requiring multiple read ports and low access latency to support modern superscalar microprocessors [19].

Consequently, the design of energy efficient wide fan in DLG is essential for bit-line and multiplexer applications. Owing to its reduced switching power consumption and enhanced noise immunity the proposed DLG is well suited for implementing wide fan-in multiplexer, register files and high-performance superscalar processor datapaths.

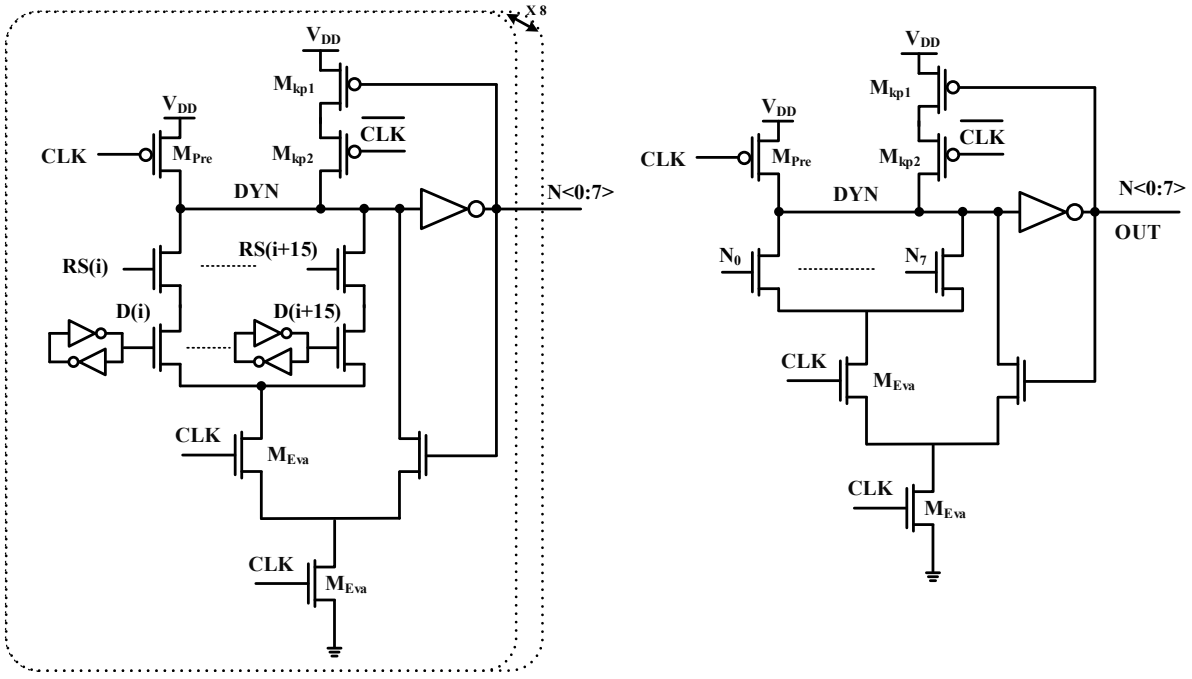


Fig. 19. 128-input multiplexer implemented using the proposed circuit

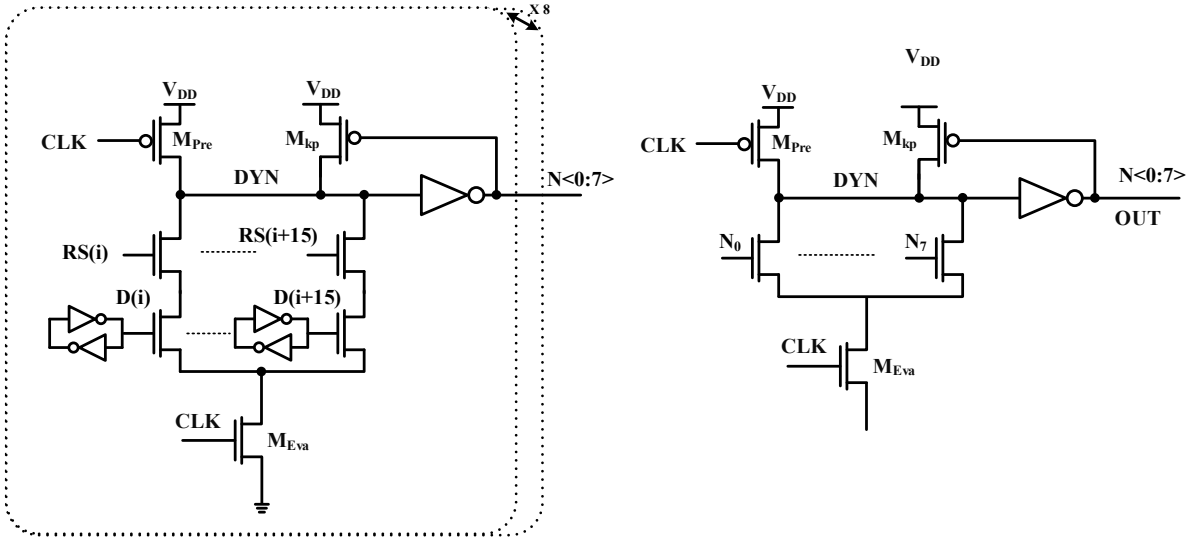


Fig. 20. 128-input multiplexer implemented using the SFDLG circuit

To demonstrate the effectiveness of the proposed DLG relative to the SFDLG [7], a 128-bit wide fan-in multiplexer was implemented using both logic styles, as shown in Figs. 19 and 20, respectively. To achieve improved speed and better management of parasitic capacitances compare to a single large evaluation stage, a multistage architecture was adopted. Specifically, eight 32 X 1 multiplexers were operated in parallel and their outputs were subsequently applied to an 8-input OR gate in the second stage to generate the final output.

The key performance parameters, including P_{Avg}, propagation delay, UNA and FOM were extracted through post-layout simulations of the proposed domino-based multiplexer. All metrics were normalized with respect to the conventional domino-based multiplexer are summarized in Table 7. For FOM calculation, the multiplexers area was obtained from the layout as shown in Fig. 24. The results indicate that the proposed design achieves improved performance across most evaluated metrics primarily due to reduced charge sharing at the dynamic node and effective suppression of subthreshold leakage enabled by the conditional keeper and modified PDN.

Furthermore, both the proposed and conventional domino-based multiplexer designs were evaluated under PVT variations to assess robustness and reliability. The P_{Avg} and delay characteristics were measure across different process corners, supply voltages and operating temperatures with results shown in Figs. 21-23. It is evident that the proposed domino-based multiplexer exhibits superior tolerance to PVT variations compared to the conventional design [7], confirming its enhanced stability and robustness for large fan-in applications.

Table 7. Normalized value of various performance metrics for the 128 X 1 multiplexer.

	Conventional	This work
Power(µW)	39.295	26.505
Normalized power	1	0.674
Delay(ps)	145.021	145.468
Normalized delay	1	1.003
PDP (fJ)	5.698	3.855
Normalized PDP	1	0.676
EDP	826.419	560.889
Normalized EDP	1	0.678
UNA (V)	0.439	0.532
Normalized UNA	1	1.211
Area (µm * µm)	36.78 * 50.48	38.90*52.60
Normalized area	1	1.102
Normalized FOM	1	1.63

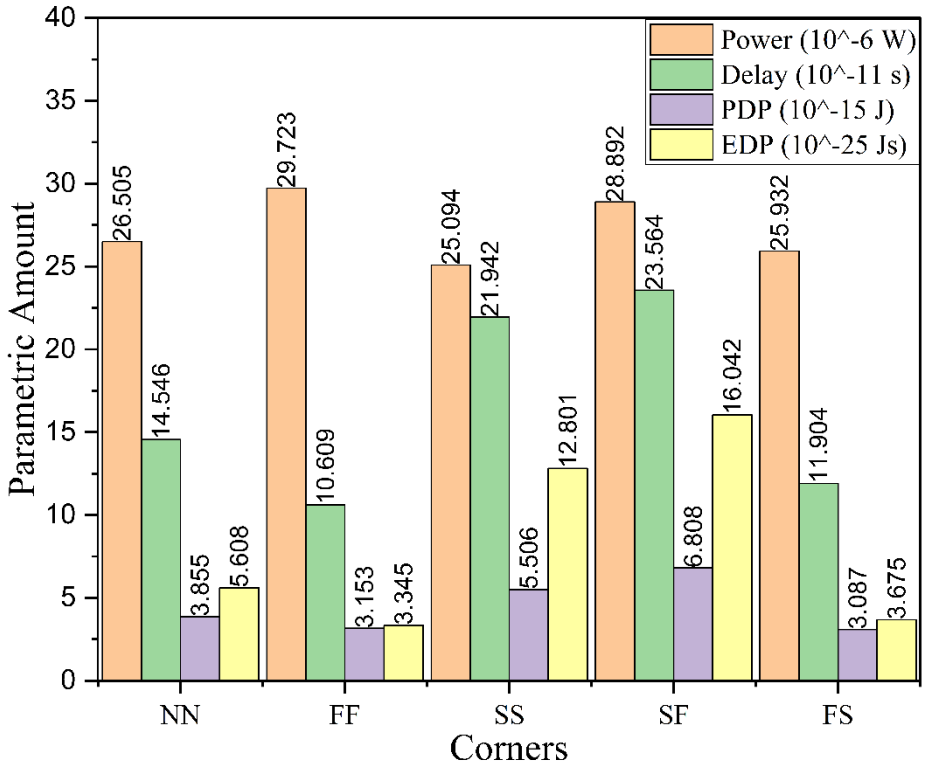


Fig. 21. Performance metrics of the proposed 128-bit MUX across different process corners.

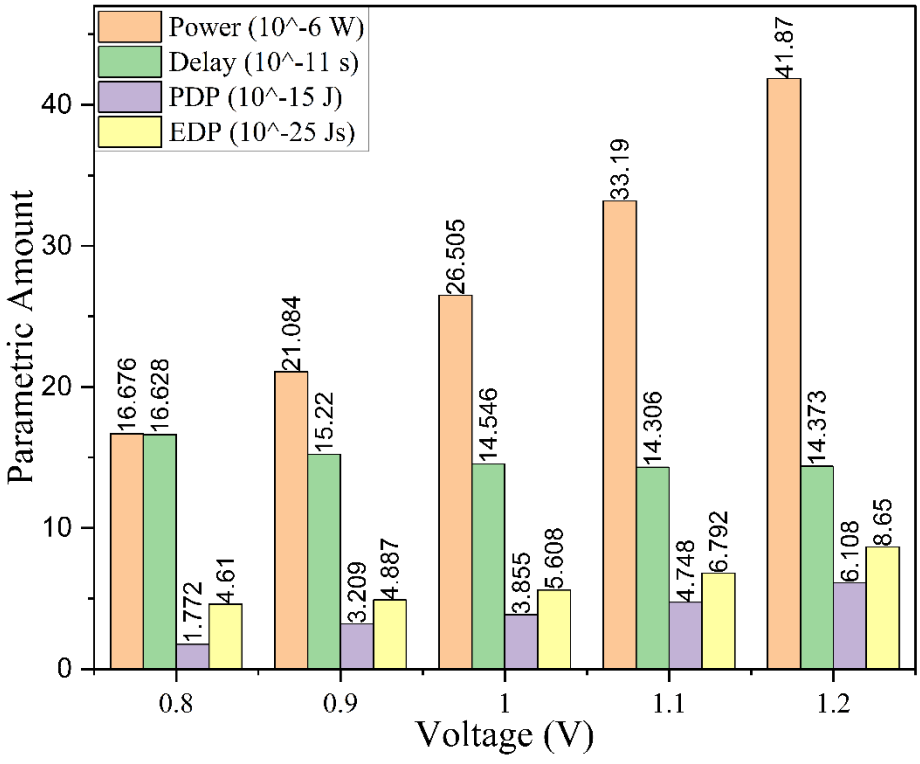


Fig. 22. Performance metrics of the proposed 128-bit MUX across different supply voltage

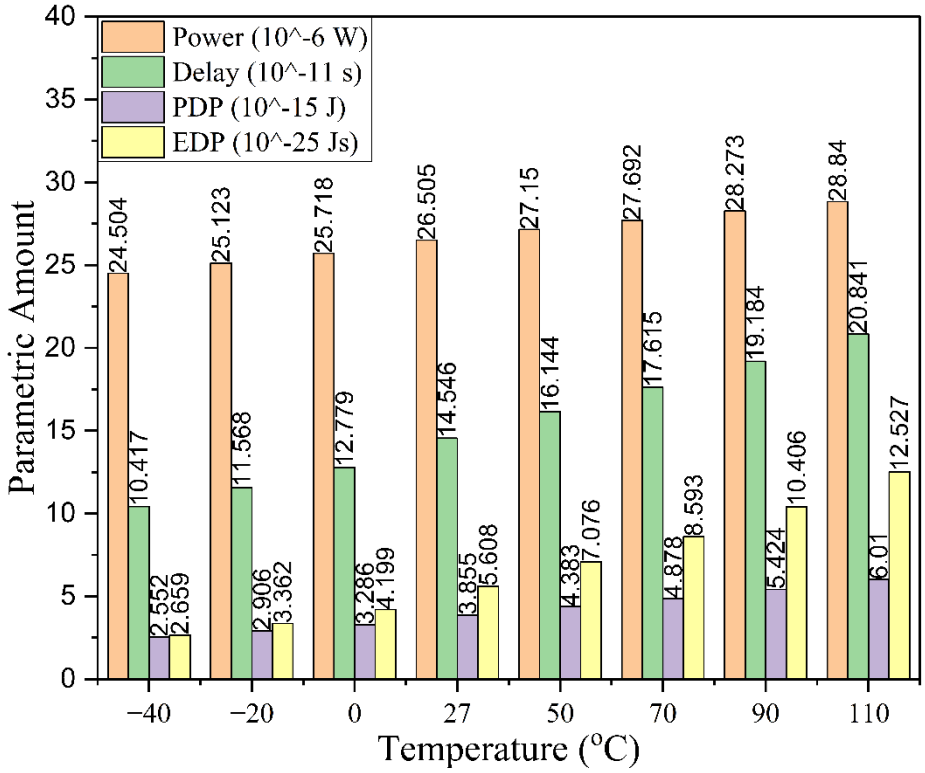


Fig. 23. Performance metrics of the proposed 128-bit MUX across different temperatures.

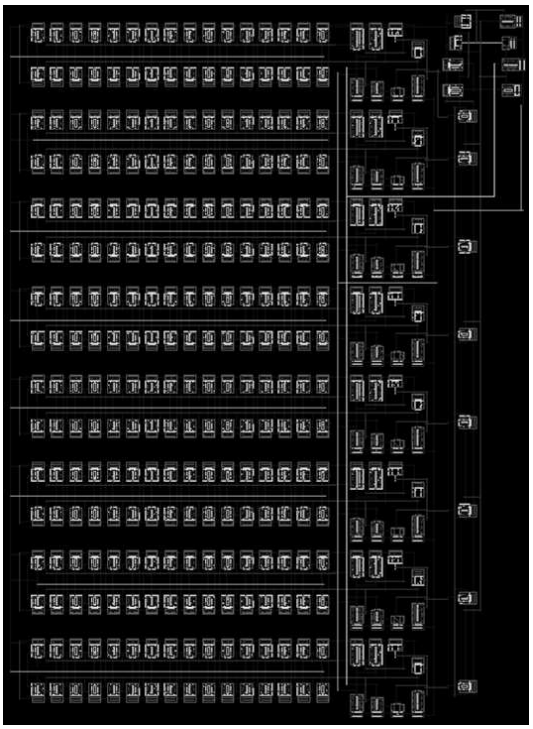


Fig. 24. Layout of 128-input multiplexers implemented using the proposed circuit.

6.Conclusion

The robust and power-efficient domino logic architecture presented in this paper is designed for wide fan-in dynamic circuits. The suggested approach significantly lowers dynamic power

consumption while maintaining dynamic node stability by utilizing adaptive keeper control to prevent unnecessary keeper PDN contention during valid evaluation. A revised PDN that has a stacked footer transistor and parallel discharge channels also helps to alleviate the leakage and variability issues that are frequently associated with wide fan-in domino logic. Without appreciably slowing down evaluation speed, this arrangement raises the effective threshold voltage, suppressing subthreshold leakage and charge sharing. Analytical formulations and through simulation results show better power-delay and energy-delay characteristics, increased noise immunity and enhanced tolerance to process changes as compared to traditional domino logic gate.

The suggested method is further validated by implementing and comparing a 128-bit wide fan-in multiplexer to a traditional architecture. The simulation findings indicate a 32% decrease in power usage, a 21% improvement in noise margin and a 32% decrease in PDP and EDP respectively. These findings support the suggested architectures applicability for contemporary energy-efficient wide fan-in dynamic logic applications.

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