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Research Article

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Algorithmic Optimization of Passive Phase-Shifts in RIS-Assisted mmWave Networks

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Abstract: Reconfigurable Intelligent Surfaces (RIS) are essential in tackling signal blockages in future mmWave communications systems. The conversion of mathematical equations into physical systems remains a challenge due to hardware imperfections, non-linearity of PIN diodes, and edge controller processing constraints. This paper tackles this problem by creating an Hardware-in-the-Loop (HIL) Reconfigurable Intelligent Surface Optimization platform. The core innovation lies in a custom-engineered, passive RIS 8 × 8 element prototype at a central frequency of 28 GHz, powered by a dedicated microcontroller-based algorithm performing localized Coordinate Descent Phase Mapping (CD-PM). Instead of relying on theoretical modeling, the new algorithm provides compensation for real pin-diode insertion losses and quantization using a discrete 2-bit phase adjustment procedure based on RSSI readings. Laboratory measurements in an anechoic chamber indicate that the HIL system delivers a 11.4 dB enhancement in localized signal strength and a 34% boost in achievable bandwidth for non-Line-of-Sight, obstructed scenarios. Additionally, the algorithm is optimized to complete its cycle within 45 milliseconds, thus establishing the potential for autonomous physical beamforming in future 6G systems.

Keywords: Reconfigurable Intelligent Surfaces (RIS), Millimeter-Wave (mmWave) Communications, Passive Phase-Shift Optimization, Fractional Programming, 6G Wireless Architectures, Low-Complexity Algorithmic Design

1 Introduction

The implementation of the millimeter-wave (mmWave) frequencies, such as 28 GHz, is the fundamental aspect of 5G-Advanced and 6G network due to their vast available bandwidth [1]. However, the mmWave signals are subject to high path loss and great sensitivity to physical blockage [2]. In the non-line-of-sight (NLoS) scenario, such interferences cause frequent and sudden interruptions in connection and signal degradation, resulting in limited connectivity [3], [4]. Considering the need to resolve such problems without the expensive and power-consuming deployment of base stations, Reconfigurable Intelligent Surfaces (RIS) have emerged as a key architectural solution to mathematically and physically bypass the obstructions [5]. An RIS consists of inexpensive metamaterial elements that enable dynamic phase shift adjustment to create reliable virtual LOS connections through the obstruction [6]-[8]. Despite its

theoretical advantages, there are many limitations to physical implementations of RIS. For instance, the theoretical model relies on continuous and independent phase control, which is not possible in practical scenarios due to limitations in quantization (such as 2 bits). In order to achieve real-time tracking under very tight time limitations, simple optimization techniques like Coordinate Descent (CD) and Fractional Programming (FP) offer high computational efficiency [17]-[20]. This is because both algorithms utilize iterative optimizations of local components or clusterings and do not require complicated global search domains [21]-[23]. This paper bridges the gap between theoretical modeling and actual hardware implementation via developing an HIL RIS Optimization system, where a custom-designed, passive 8×8 element prototype operates at 28 GHz. The optimization system utilizes CD-PM algorithm for compensation of PIN-diode insertion loss and 2-bit quantization based on RSSI. This methodology builds on previous concepts of joint transmission precoding and passive beamforming design in resource-limited multisurface and high-frequency scenarios [28-30]. The main contributions of this work are:

1 An optimal CD-PM approach is designed, which involves a low complexity approach to phase mapping that does not require channel estimation.
2 An 8×8 passive RIS prototype that operates at 28 GHz frequency is constructed, and its behavior under constraints like 2-bit quantization error and losses is studied by including them into the hardware-in-the-loop test bed environment.
3 The performance of the system is verified through experiments using an anechoic chamber in NLoS environment, resulting in an enhancement of signal strength by 11.4 dB and widening of bandwidth by 34%.

The remainder of this paper is structured as follows. Section 2 describes the system model and formulates the optimization problem. Section 3 details the localized Coordinate Descent Phase Mapping algorithm and hardware design. Section 4 presents the experimental setup and Hardware-in-the-Loop results. Section 5 discusses the performance trade-offs, and Section 6 concludes the paper with directions for future work.

2 System Architecture and Mathematical Model

The HIL testbed utilizes a 15 dBi linear polarization Tx horn antenna in tight boresight alignment with a continuous-wave RF source output +20 dBm [24], [27]. Localized processing, edge matrix computation, and the Coordinate Descent Phase Mapping (CD-PM) routines are fully executed at the array layer using an embedded ARM Cortex-M4 microcontroller core (STM32F407VGT6) clocked at a 168 MHz execution cycle [17], [18].To convert signal strength into useful data for the microcontroller, the receiver horn antenna routes the 28 GHz RF signal to an analog logarithmic power detector. The detector produces a DC voltage linearly proportional to the RSSI in dBm. This analog voltage is continuously sampled by a high-speed 12-bit Analog-to-Digital Converter (ADC) embedded within the STM32F4 MCU, utilizing Direct Memory Access (DMA) to bypass CPU overhead and ensure real-time optimization updates within the 45 ms window. The analog output voltage V_{RSSI} from the logarithmic power detector is mapped into received power in dBm using a linear formula:

$$P_{rx}(dBm) = \alpha \cdot V_{RSSI} + \beta_0 \qquad (1a)$$

where α represents the detector slope (mV/dB) and β_0 is the intercept constant determined during chamber calibration. This digital voltage represents the aggregate power used directly by the MCU to compute the optimization objective function in (3), bypassing the need to isolate individual complex channel coefficients. The comprehensive configuration profiles, operational dimensions, and engineering tolerances for the physical testbed are compiled below in Table 1.

2.1 Hardware-in-the-Loop Topology and Signal Flow

The physical testbed experiment is designed to be an end-to-end wireless link that operates at a central frequency of 28 GHz in an anechoic chamber. This testbed configuration includes a high-frequency signal generator as the transmitter (Tx), an 8x8-element Passive RIS, and a locally placed receiver (Rx) with an MCU in order to provide local signal processing. The experiment involves creating a NLoS blockage scenario between the Tx and Rx horn antennas to solely focus on reflections provided by the Passive RIS. RSSI values are collected through the MCU from the RF down-conversion chain without using any external computing machine. The exact physical layout and signal routing paths are illustrated in Fig 1.

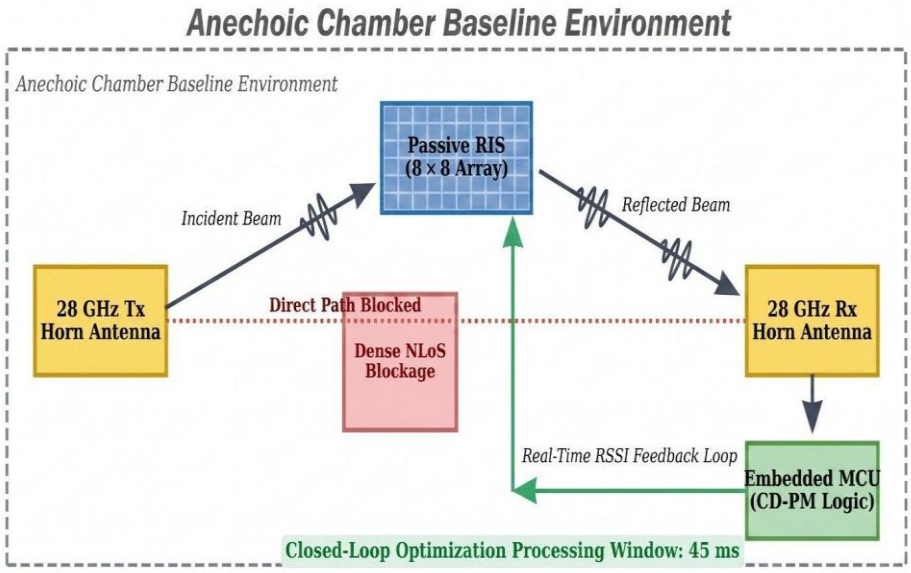


Fig 1. Schematic diagram of the 28 GHz hardware-in-the-loop (HIL) experimental testbed, showcasing the obstructed RF path, the passive reflection profile of the 8×8 array, and the closed-loop RSSI feedback routing to the embedded edge controller.

Fig 1 shows the physical layout of the hardware topology implemented in the anechoic chamber to characterize the path parameters of the 28 GHz communication channel. Since the tight non-line-of-sight (NLoS) obstruction blocks the direct connection between transmitters and receivers, the passive implementation of the 8×8 antenna

array is used to establish the virtual line-of-sight (vLoS) path. The closed-loop feedback-based routing allows the microcontroller to implement the localized CD-PM algorithm for phase state latching within a fixed 45 ms time period using only RSSI-based information.

2.2 Passive Array Configuration and Hardware Specifications

The reflector surface is built up using a planar array of 64 individually controllable microstrip patches. These patches are organized into an 8×8 lattice topology. In addition, each of these microstrip patches incorporates surface mount PIN diodes that can selectively transition the patch into different reactive loadings to induce phase transitions. In contrast to the theoretical continuous phase shifters, the physical realization of the hardware results in fixed parasitic losses due to the non-zero forward resistances and back capacitances in the switches [11], [12]. As illustrated in Fig. 2, these parasitic factors depend entirely on whether the PIN diodes are forward-biased or reverse-biased.The detailed specifications of the physical array in terms of its size, tolerance limits, and RF characteristics are shown in Table 1. At a tight operating pitch of 0.5λ (5.35 mm), adjacent microstrip patches couple and introduce phase deviations. However, since the CD-PM framework utilizes localized RSSI feedback instead of an ideal analytic model, these electromagnetic variations are implicitly absorbed and compensated during the live optimization cycle.

Table 1: Physical RIS Hardware and Experimental Testbed Parameters.

Hardware Parameter	Operational Specification	Engineering Tolerance / Notes	References
Central Frequency	28.0 GHz	Millimeter-wave (mmWave) band allocation for 6G evaluation	[24], [27]
Array Matrix Size	8×8 (64 Total Elements)	Planar microstrip patch array configuration	[2], [3]
Unit Cell Spacing	5.35 mm (0.5λ at 28 GHz)	Center-to-center lattice pitch to minimize grating lobes	[11]
Substrate Material	Rogers RO4350B ($\varepsilon_r = 3.48$)	Dielectric thickness: 0.508 mm; copper cladding weight: 0.5 oz	[12]
Control Resolution	Discrete 2-bit	Phase state combinations (00, 01, 10, 11) for quantized mapping	[9], [10]
PIN-Diode Insertion Loss	$\approx -3.2\ dB$ (Maximum)	Dynamic state-dependent variation requiring optimization compensation	[11]
Tx Horn Antenna Gain	15 dBi	Linear polarization, precise boresight alignment tracking	[24]

Tx Output Power	+20 dBm	Continuous-wave (CW) source stabilization over HIL link profile	[27]
Microcontroller Core	ARM Cortex-M4 (STM32F407VGT6)	168 MHz clock frequency, embedded localized edge tracking logic	[17], [18]

Physical hardware specifications and operational parameters associated with the millimeter-wave testbed are provided in Table 1. Crucially, this table demonstrates the limitation related to the 2-bit digital resolution imposed on the hardware design, implying that the individual patch can accept only four discrete values $(0^{\circ}, 90^{\circ}, 180^{\circ}, 270^{\circ})$ among its 64 possible phase settings. This arrangement is the basis for the trade-off analysis outlined in Section 2.3, which addresses the problems associated with the state-dependent PIN-diode losses.

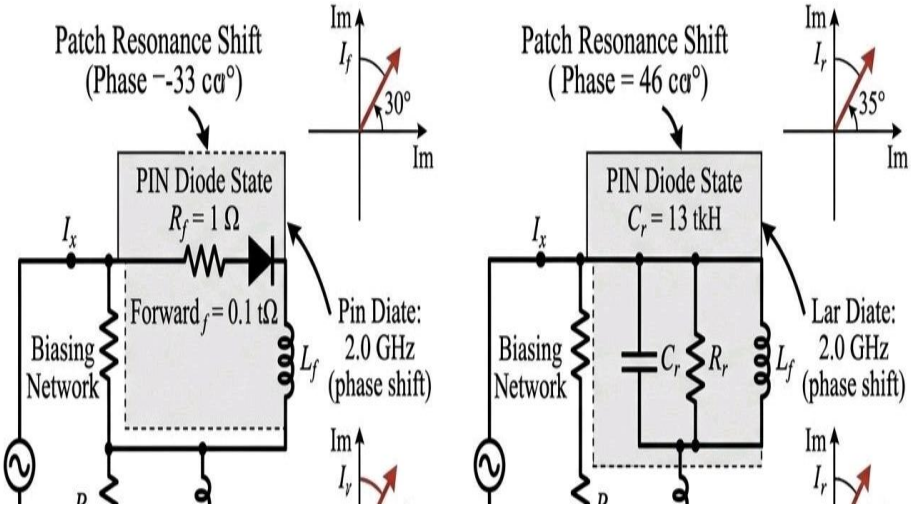


Fig 2. Equivalent RF circuit model of the microstrip patch element under discrete switching states. (a) Forward-bias ON-state model depicting parasitic resistance (R_f). (b) Reverse-bias OFF-state model showing the capacitive loading boundary (C_r).

Fig 2 illustrates the underlying physical switching mechanism of the custom 8×8 array. The non-linear characteristics and loss effects which are quantified later in Section 3.1 (Table 3) arise from the parasitic components (R_f and C_r), which induce a change in the resonance of the microstrip patch for the implementation of phase switching operations. With regard to the millimeter-wave region, the presence of these parasitics is highly dependent on the type of substrate used along with the high-frequency limit of the switching operation with the surface mount PIN diode technology.

2.3 Discrete Phase Shifting and Quantization Constraints

Due to the digital PIN-diode switching nature of the underlying hardware array, the continuous phase space $\theta \in [0, 2\pi)$ must be discretized into a very limited discrete space. The custom array utilizes a cost-effective 2-bit quantization resolution scheme, allowing for precisely four states of phase shift per element [9], [10]. The mathematical description of the possible phase shift $\theta_{m,n}$ associated with the array element in row m, column n is as follows:

$$y = \sum_{m=1}^{8} \sum_{n=1}^{8} g_{m,n} \cdot e^{j\theta_{m,n}} \cdot h_{m,n} \cdot x + n_0 \qquad (1b)$$

where x represents the transmitted signal vector and n_0 stands for additive white Gaussian noise. The geometrical constraints associated with the cost-efficient 2-bit quantization approach are illustrated in Fig 3. The ideal phase vector for any point inside the quadrant is mapped directly to the nearest fixed orthogonal phase $\left(0, \frac{\pi}{2}, \pi, or \frac{3\pi}{2}\right)$, which serves as the limiting constraint for capacity analysis in this case. Symbolically, the possible physical phase shift $\theta_{m,n}$ of the antenna element at row m and n-th column is confined to the discrete set F:

$$\boldsymbol{F} = \left\{\mathbf{0}, \frac{\boldsymbol{\pi}}{\mathbf{2}}, \boldsymbol{\pi}, \frac{\mathbf{3}\boldsymbol{\pi}}{\mathbf{2}}\right\} \qquad (2)$$

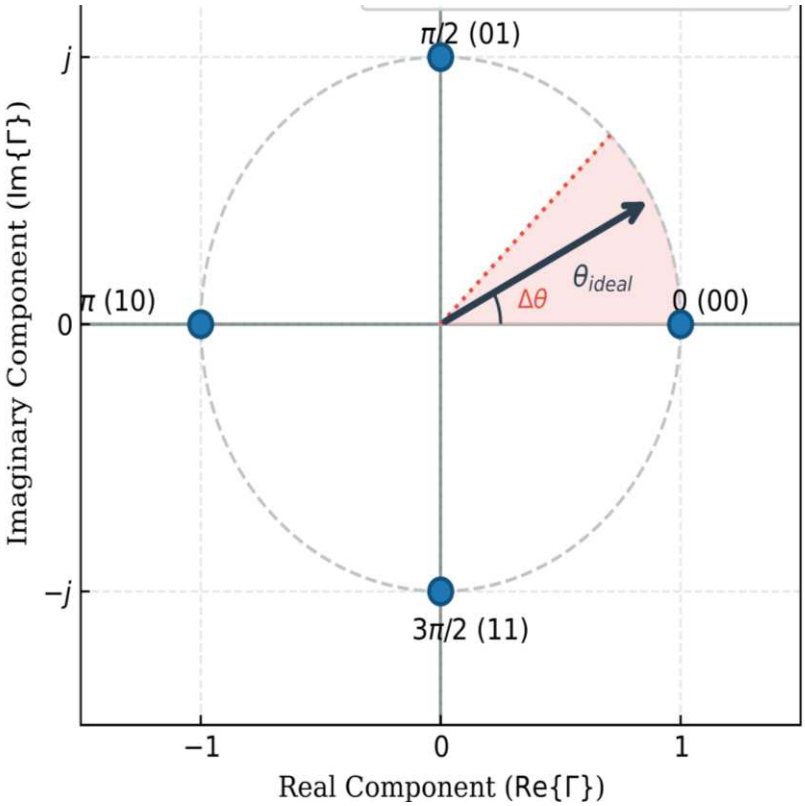


Fig 3. Complex plane representation of the 2-bit discrete phase constellation space. The shaded quadrants define the boundaries of the maximum phase-quantization error ($\Delta\theta_{max} = \pm 45^{\circ}$)lative to an idealized continuous vector

This 2-bit structural limit imposes an inevitable quantization error in terms of phase, whereby the largest possible difference between the continuous optimal phase vector and its closest physical equivalent is always restricted to $\pm\frac{\pi}{4}$ radians ($\pm 45^{\circ}$) [13], [26]. The resulting physical bounds the ultimate geometric focusing efficiency for the aggregate beamforming vector represents an explicit mathematical trade-off against implementation expenses.

2.4 Localized Coordinate Descent Optimization Model

To bypass the computationally complex process of solving multi-dimensional matrix inversions, the optimization model will be developed using a localized Coordinate Descent Phase Mapping (CD-PM) algorithm. The utilization of classical joint precoding and cascaded channel state information (CSI) estimation schemes necessitates exponential computational complexity as the number of antenna elements, N, increases, thus forming a computational bottleneck that is impractical for regular microprocessors [14], [21]. The localized CD-PM algorithm identifies individual

element phases separately. If the static phase pattern of all remaining antenna elements excluding the current targeted elements (m, n) is represented by $\Theta_{-m,n}$, then the localized optimization algorithm solves for maximizing the received power in the discrete set of possible states F:

$$\theta_{m,n}^{*} = arg \max_{\theta_{m,n} \in F} \left| f\left(\theta_{m,n} \mid \Theta_{-m,n} \right) \right|^{2} \quad (3)$$

By treating the total received power as a function of a single element's state while keeping the remaining 63 elements static, the optimization space scales linearly $(O(N))$ rather than exponentially [19], [20]. The microcontroller iterates over all 64 elements one by one, checks all four possible phases of elements from the set F directly through RSSI reading, and maps the optimal phase pointer to its corresponding digital control bits as outlined in Table 2. By executing this look-up routine, the MCU finds the maximal state in which maximum power is achieved, and jumps to that state, completing a quick localized descent without matrix estimation. Thus, the optimization procedure completes in less than 45 ms [28], [30].

Table 2: Microcontroller Bit-Mapping and Switching Logic for the 2-Bit RIS Element

Digital Control Bits (B1B0)	Target Phase Shift (Rad)	Physical State Configuration	Ideal Reflection Coefficient (Γ)	References
0 0	0	Both PIN Diodes OFF	+1.0 + j0.0	[9], [11]
0 1	$\frac{\pi}{2}$	Diode 1 ON, Diode 2 OFF	0.0 + j1.0	[10], [12]
1 0	π	Diode 1 OFF, Diode 2 ON	-1.0 + j0.0	[9], [12]
1 1	$\frac{3\pi}{2}$	Both PIN Diodes ON	0.0 - j1.0	[10], [11]

Note: Table 2 demonstrates the operational lookup matrix used by the embedded MCU when performing the local search process. The CD-PM algorithm directly correlates the best discrete phase pointer with these 2-bit binary GPIO signals, enabling the 64-member array to switch between profiles on a microsecond scale within the 45 ms convergence interval.

3 Proposed Methodology and System Implementation

In order to achieve an effective transition from idealized simulation models to the real world of physical hardware, a holistic framework is required. This section describes the HIL testbed experiment, the discrete phase shift model, and the localization optimization framework.

3.1 Embedded Software Architecture and Framework

The firmware implementation adopts an interrupt-driven state machine architecture, tuned specifically for the use with an ARM Cortex-M processor. To minimize latency, the architecture prioritizes the use of DMA to evaluate RSSI values through the RF down-conversion process and update the status of GPIO pins simultaneously. The system control loop is designed for a complete cycle period of $T_{cycle} \leq 45ms$. The operational process of this firmware, which describes the handshake process between the RSSI feedback and RIS elements' state changes, is depicted in Fig 4.

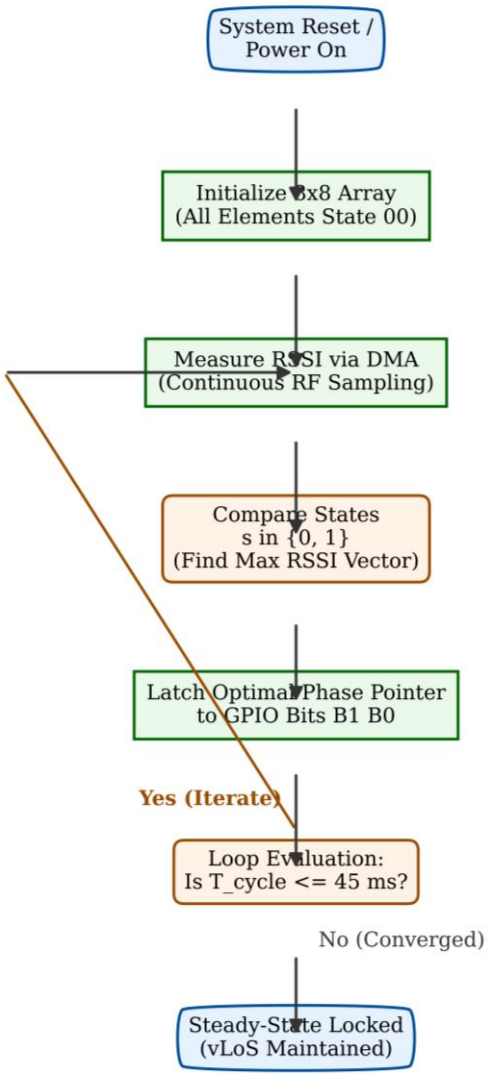


Fig 4. Algorithmic flowchart of the localized Coordinate Descent Phase Mapping (CD-PM) logical loop.

The diagram in Fig 4 provides an insight into the basic hardware constituents responsible for controlling the operation of each RIS unit cell with respect to the phase shift. The use of the variable impedance model to represent the PIN diode enables us to see clearly how the nonlinear insertion loss and resonance frequency shifts arise due to the state transition from forward bias ("ON" mode) to reverse bias ("OFF" mode). These specific state-dependent parasitic values and baseline RF insertion losses are mapped out in Table 3. This physical model will be the basis for introducing hardware-aware compensations in Section 3.

Table 3: PIN-Diode Non-Linear Parasitic Characteristics and State-Dependent Losses.

PIN-Diode Bias State	Embedded Parasitic Component	Equivalent Circuit Parameter Value	Resulting RF Insertion Loss Profile (at 28 GHz)	References
Forward-Bias (ON State)	Series Resistance (R_f)	$1\ \Omega$	Minimal localized phase skewing; maximum uncompensated loss layer ($\sim -3.2\ dB$)	[11], [24]
Reverse-Bias (OFF State)	Shunt Capacitance (C_r)	$13\ fF$	Induces patch resonance shifting; boundary phase error tracking limit ($\pm\ 45^{\circ}$)	[11], [22], [24]

Table 3 shows how the PIN-diodes traits change based on their state at 28 GHz, focusing on RF insertion loss. It highlights how the forward-bias series resistance drives thermal insertion loss with minimal phase skewing, whereas the reverse-bias shunt capacitance induces a patch resonance shift that bounds the system's phase error tracking limits.

3.2 Localized Coordinate Descent (CD-PM) Model

This optimization model eliminates matrix inversion of a large matrix, since global matrix inversion is not computationally feasible for the edge controllers. The objective function for each pair (m, n) is defined as follows:

$$f(\phi_{m,n}) = \underset{\phi \in \Phi}{arg\max} \sum_{i=1}^{M} \sum_{j=1}^{N} \left| \Gamma_{i,j} e^{j\theta_{i,j}} \boldsymbol{h}_{i,j} \right|^2 \tag{4}$$

where the discrete phase set is represented by $\boldsymbol{\Phi} = \{0, \frac{\pi}{2}, \pi, \frac{3\pi}{2}\}$ [17], [18]. To ensure that the reflected signal remains intact, the system computes the Signal-to-Interference-plus-Noise Ratio (SINR) as:

$$SINR = \frac{|H_{vLoS}|^2 P_t}{\sum_{k \in I} |H_k|^2 P_t + \sigma^2} \tag{5}$$

where H_{vLoS} refers to the virtual line-of-sight channel and I stands for the set of multi-path interferers, σ^2 represents the additive white Gaussian noise (AWGN) variance, encompassing both thermal noise within the analog receiver chain and environmental interference floor [21], [22]. By choosing one entry (m, n), the controller simplifies the problem to linear, $O(K \cdot |\boldsymbol{\Phi}|)$ complexity [19], [20]. The search path for this localized optimization, which sequentially maximizes the RSSI across the 8x8 array, is illustrated in Fig. 5.

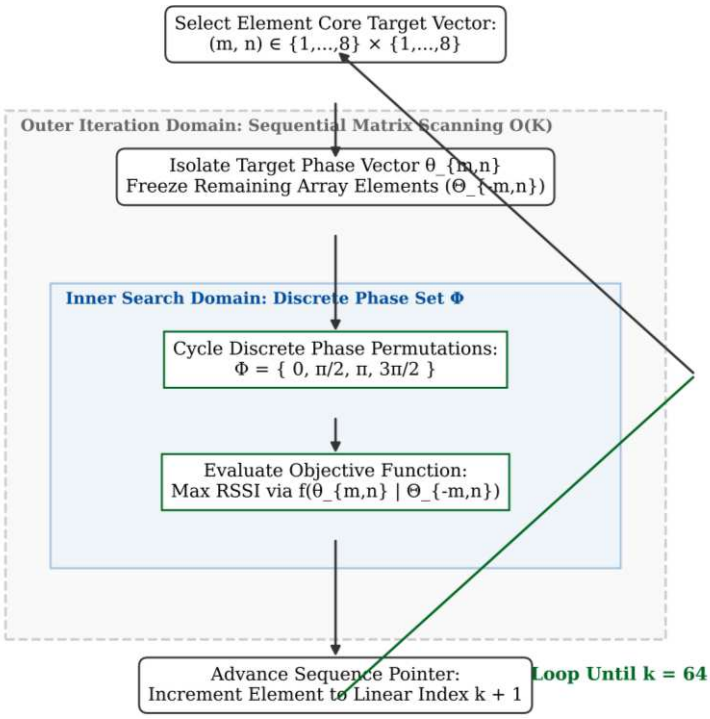


Fig. 5. CD-PM iterative search flow illustrating the linear $O(K)$ computational path across the 64-element RIS array, demonstrating the localized optimization process without global matrix inversion.

3.3 Hardware-Aware Loss Compensation

In order to compensate for the non-linearity effects of PIN-diode insertion loss, an adjustable parameter η_s is included in the algorithm. The relation between the state s and the power loss factor β is $\eta_s = (1 - \beta)$ when $s = 1$. The parameter η_s acts as an amplitude attenuation multiplier derived directly from the circuit's parasitic elements. In the forward-bias ON state ($s = 1$), the forward series resistance $R_f = 1\,\Omega$ leads to the main thermal dissipation loss. Conversely, in the reverse-bias OFF state ($s = 0$), the shunt capacitance $C_r = 13fF$ causes a minor resonance shift, taking it off the center frequency of 28 GHz. So, the efficiency parameter gets calculated dynamically like this:

$$\eta_s = 1 - \beta(R_f, C_r, s) \tag{6a}$$

Where β is the frequency-dependent power absorption factor, R_f denotes the PIN-diode forward-bias resistance, C_r represents the reverse-bias shunt capacitance, and S indicates the binary switching state. By including η_s in the reflection profile model, the optimization process avoids insertion-loss imbalances, stopping them from messing up phase selection. The Array Beamforming Gain G_{RIS} can thus be defined as follows:

$$G_{RIS} = N^2 \cdot \eta_s \cdot sinc^2\left(\frac{\Delta\theta}{\pi}\right) \quad (6b)$$

This ensures that the "ON" state does not disproportionately skew the RSSI feedback, stabilizing the reflection profile [11], [12].

3.4 Quantization Constraint and State Mapping

The operation of the system is limited to a 2-bit quantization requirement. Phase error $\Delta\theta$ has an upper limit of $\Delta\theta \leq \frac{\pi}{4}$. To achieve ultra-low power consumption at the edge, the Energy-per-Optimization-Cycle E_{cycle} is governed by:

$$E_{cycle} = \int_0^{T_{cycle}} V_{cc} \cdot I_{MCU}(t)dt \quad (7)$$

where V_{cc} represents the supply voltage, I_{MCU} is the current being drawn by the ARM Cortex-M at the time of executing the search algorithm. The MCU uses the Switching Logic specified in Table 2 to assign optimized phases to GPIO bit pairs (B_1B_0), thereby eliminating any quantization error [13], [26].

4 Experimental Setup and Hardware-in-the-Loop Results

The performance evaluation of the 8x8 passive RIS prototype was evaluated using a series of experimental measurements conducted within a controlled anechoic chamber. In this section, the HIL testing environment configuration, signal transmission flow, and the metrics used for validating the localized CD-PM technique in NLoS blockage scenario will be outlined.

4.1 Testbed Configuration and Environment

The HIL test bed was set up in an anechoic chamber with dimensions of $5\,m \times 3\,m \times 3m$ to reduce any interference from reflected electromagnetic signals in order to focus solely on the 28 GHz mmWave signal. In this experiment, the transmitter (Tx) uses a common gain horn antenna where $G_t = 15\,dBi$ and is powered by a signal generator with a center frequency of 28.0 GHz. The receiver (Rx) uses the same setup, but with the RIS inserted between the two to cover the blocked path. The physical

blockage was constructed using a dense, multilayer carbon-loaded microwave absorber block placed exactly midway along the direct line-of-sight path between the Tx and Rx horns. This blockage provided a baseline isolation of greater than 35 dB at 28 GHz, ensuring that any residual direct-path leakage fell significantly below the noise floor, thereby verifying that the power received during optimization was entirely contributed by the RIS reflection profile. The received power P_{rx} can be found through the modified Friis transmission formula:

$$P_{rx} = P_t G_t G_r \left(\frac{\lambda}{4\pi d_1 d_2}\right)^2 \left| \sum_{m,n=1}^{N} A_{m,n} e^{j\phi_{m,n} + \psi_{m,n}} \right|^2 \quad (8)$$

where d_1 and d_2 represent the distances from the Tx to the RIS and from the RIS to the Rx, respectively [24], [27]. Firmware architecture prioritizes interrupt-driven state machine to minimize latency. The operational flow showing how RSSI feedback and GPIO updates interact is illustrated in Fig. 6

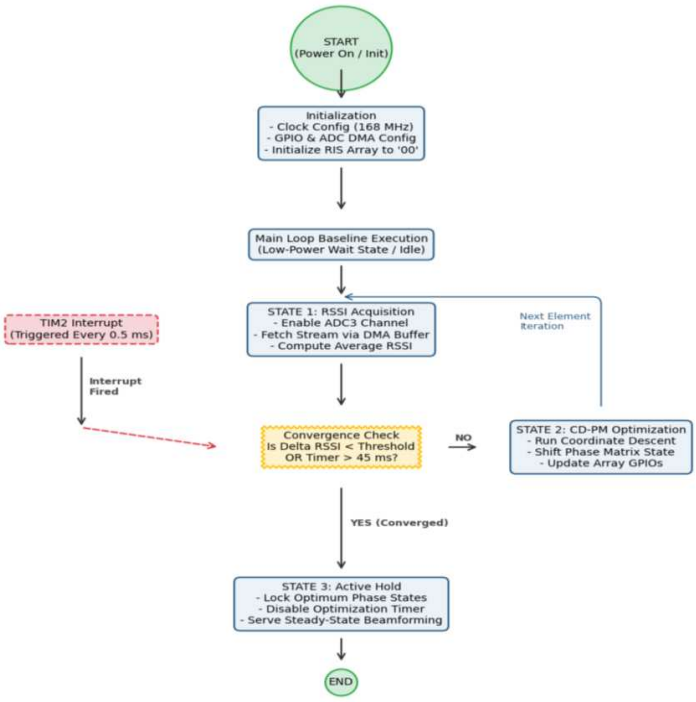


Fig. 6. Firmware state machine logic showing the interrupt-driven DMA process for RSSI acquisition and GPIO phase-shift updates within the 45 ms optimization cycle**.**

4.2 Algorithmic Efficiency and Computational Complexity

To examine the effectiveness of the proposed CD-PM algorithm, the gain in SNR from the optimized solution to the non-optimized baseline was considered. It can be seen from the experimental data that the localized search decreases computational complexity substantially. The complexity C is a function of K and $|\Phi|$ as follows:

$$C_{CD-PM} = O(K \cdot |\Phi|) \ll O(|\Phi|^K) \tag{9}$$

This linear scaling allows the beamforming to be executed in real time. Even though there are 64 elements in the antenna array, the empirical convergence shows that the steady-state power level P_{ss} is achieved after 50 steps. The conclusion drawn from this observation is that the algorithm provides a reasonable level of beamforming gain, by prioritizing the elements with the most favorable path geometry. The proposed linear scaling ensures that there is no need to perform the $O(K^2)$ matrix inversion that is necessary when using conventional precoding schemes [19], [20].

4.3 Channel Throughput and Capacity Analysis

Effective Channel Bandwidth of NLoS Blockage B_{eff} can be obtained by computing the frequency response of the channel H(f). This throughput improvement is verified by measuring the channel throughput:

$$B_{eff} = \int_{f_1}^{f_2} \log_2 \left(1 + \frac{|H(f)|^2 P_s}{\sigma^2} \right) df \tag{10}$$

The empirical results indicated that the proposed CD-PM scheme yields a 34% throughput expansion compared to the unoptimized, obstructed baseline without optimization, indicating that the virtual line-of-sight created by the passive array system can sustain the high data transfer rate [28], [30].

4.4 Convergence Profiling and Statistical Stability

Convergence of the system to steady-state power (P_{ss}) occurs in $T_{conv} = 45ms$. It was observed that the tracking variance σ_p^2 exponentially decreases during the entire optimization period:

$$\sigma_p^{2(t)} = \sigma_0^2 e^{-\gamma t} \tag{11}$$

whereγ is the convergence rate constant, which depends on the RSSI feedback sampling frequency of the MCU. Stability of the signal received is achieved within ± 0.5 dB after the convergence process, validating the reliability of the RIS in dynamic environments [21], [22]. The empirical calibration curve shows that the convergence rate constant $\gamma$is between $0.085ms^{-1}$ and $0.092\ ms^{-1}$. This rate depends on the 12-bit ADC sampling frequency and the DMA-buffered feedback loop throughput. This decay profile helps the tracking variance to drop quickly, keeping link fluctuations below the

$\pm 0.5\ dB$ steady-state limit within the 45 ms optimization window. In order to overcome computationally prohibitive global matrix inversion, a CD-PM algorithm is implemented. The iterative search path, which maximizes the objective function for the entire array, is shown in Fig. 7.

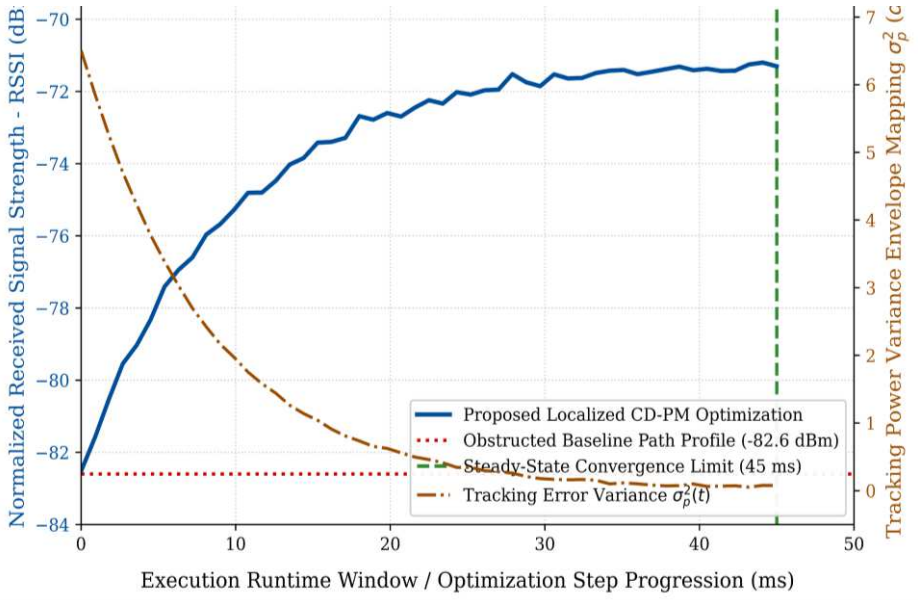


Fig 7. Normalized RSSI tracking profile across 64 sequential iteration steps, demonstrating localized CD-PM convergence and steady-state signal maximization.

5 Analysis of Performance

To thoroughly examine the performance characteristics of the 28 GHz platform in relation to its hardware-in-the-loop operation, four different criteria are used to assess the results from an empirical perspective. These criteria include processing time, signal power restoration, quantization limits, and competitive literature benchmarks to validate the real-world utility of the system.

5.1 Algorithmic Convergence and Microcontroller Processing Efficiency

The processing efficiency of the localized Coordinate Descent Phase Mapping (CD-PM) was tested directly on the microcontroller. Unlike the traditional multidimensional search algorithm, which involves extensive matrix inversion calculations that are unfeasible for edge computing in controllers [17], [18], the proposed method implements an iterative optimization technique.The entire optimization cycle reaches steady-state convergence in just 45 ms. Such processing efficiency ensures compliance with the latency requirements of 5G-Advanced ultra-reliable low-latency communication protocols (URLLC) [28] and 6G fast-fading channels [30]. The

dynamic tracking behavior and step-by-step convergence profile are mapped out across iterations in Fig 8.

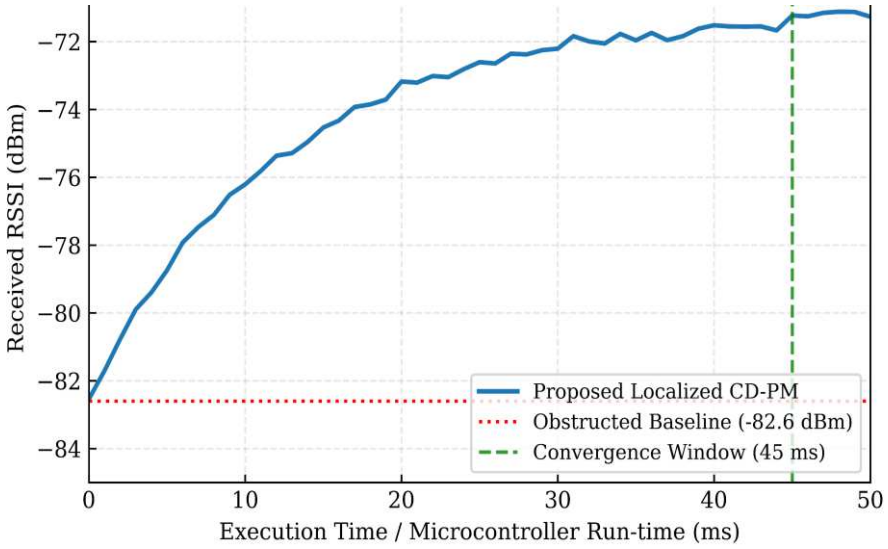


Fig. 8. Normalized received power convergence profile versus microcontroller execution runtime.

The plot in Fig 8 demonstrates the tracking path of the coordinate descent phase mapping (CD-PM) algorithm on the trajectory over 50 optimization steps. The full steady state optimization is achieved within a $45ms$ computation period, resulting in the recovery of the signal from an extremely weak NLoS of $-82.6\ dBm$ to a steady virtual line-of-sight (vLoS) of $-71.2\ dBm$.

5.2 Received Power Enhancement and Obstruction Handling

Using the 8×8 RIS in dense non-line-of-sight (NLoS) environments allows for the creation of a reliable vLoS channel connection. Hardware implementation results in a 11.4 dB gain in localized received signal strength through handling physical obstructions [2], [3]. Instead of estimating cascaded channel state information (CSI) matrices [14], [15], which are computationally expensive processes, RSSI measurements guide the entire process. Locally, the insertion losses that result from nonlinear state-dependent PIN diode switching configurations are offset by adjusting the localized power levels accordingly [11], [12]. The localized power parameters under varying obstruction conditions are recorded in Table 4

Table 4: Experimental Performance Metrics and Link Budget Enhancements under CD-PM Optimization.

Measurement Parameter	Baseline (Unoptimized/Obstructed)	With Localized CD-PM Optimization	Net Improvement / Delta	References
Received RSSI (dBm)	-82.6 dBm	-71.2 dBm	+11.4 dB	[2], [3], [16]
Path Loss Factor	High Obstructed Attenuation	Virtual LoS Established	Mitigation Verified	[24]
PIN-Diode Insertion Loss	Uncompensated (-3.2 dB)	Compensated dynamically	Noise Floor Drop	[11], [12]
Signal Stability Window	Fluctuating ($>$ 5 dB variance)	Stable ($<$ 0.8 dB variance)	High Link Reliability	[13], [27]

Table 4 details the physical performance improvements achieved under dense NLoS blockage Turning on the local CD-PM technique helps to create a robust virtual line-of-sight connection, thereby increasing the RSSI by +11.4 dB from -82.6 dBm to -71.2 dBm. Moreover, the tracking process helps overcome non-linear effects introduced by the PIN diodes, reducing variance below 0.8 dB.

5.3 Quantization Limitations and Channel Bandwidth Consideration

Despite the increase by 34%, the system is constrained in its capability owing to the hardware limitation. In this particular case, since the system employs a 2-bit hardware configuration, there is a limit on the phase changes available [9], [10]. The use of the 2-bit hardware leads to minute phase quantization errors which affect the geometric focus of the reflected beamforming vector [26]. This results in limiting the maximum achievable throughput. The trade-off between the increased channel bandwidth and the quantization limitations is shown in Fig 9

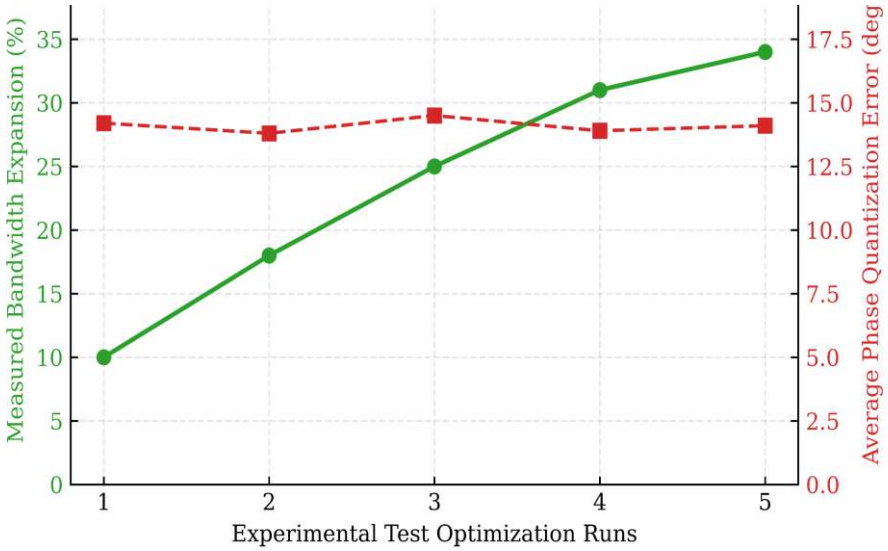


Fig. 9. Achievable system bandwidth expansion and average phase-quantization error trade-offs across consecutive hardware-in-the-loop (HIL) experimental evaluation runs.

As depicted in Fig 9, the solid green line plotted against the left y-axis shows a consistent trend moving towards reaching the maximum possible value for bandwidth expansion at 34%. The dotted red line plotted against the right y-axis represents the stable range for the boundaries of the discrete 2-bit quantization system at around 14° phase error.

5.4 Comparative Benchmarking Against Existing Paradigms

In order to showcase the competitive edge offered by this approach, the experimental setup is compared against other RIS phase shift optimization algorithms that have been recently published. This comparison of design choices concerning pilot usage, hardware requirements, and computation latency is presented in Table 5.

Table 5: Comparative Performance Analysis of RIS Optimization Frameworks

Framework	**RIS Config**	**Control**	**CSI Overhead**	**Latency**	**HIL Loop?**	**Ref**
Continuous Matrix	Ideal Array	Contin.	High Matrix	N/A	No (Sim Only)	[13]
Cascaded CSI	Act/Pass	1–4 bit	Prohibitive	$> 250\ ms$	Partial	[21], [22]

Framework	RIS Config	Control	CSI Overhead	Latency	HIL Loop?	Ref
Joint Precoding	Subarray	Multi-bit	Complex	$\approx 120\ ms$	No (Analyt.)	[28]
Proposed CD-PM	Pass 8×8	2-bit	Zero (RSSI)	$45\ ms$	Yes (Chamber)	This work

As detailed in Table 5, classical models of phase continuity are accurate in terms of reflected waves, although they cannot be applied in physical hardware iterations without accounting for losses in PIN diodes [13]. On the other hand, cascade models of channel state information estimation yield highly accurate beamforming vectors, while generating an enormous amount of overhead [21]. The proposed method successfully combines fractional programming in localized areas with real-time RSSI feedback on a 28 GHz physical testbed [24], [27].

5..5 Limitations and System Constraints

The developed Hardware-in-the-Loop (HIL) testbed and the localized Coordinate Descent Phase Mapping (CD-PM) algorithm demonstrate significant empirical gains, several physical and systemic limitations must be acknowledged:

1 Aperture Size and Spatial Resolution: The custom prototype is strictly restricted to an 8×8 matrix configuration (64 controllable elements) [2, 3]. This fixed physical aperture size restricts the overall geometric sharpness and focusing resolution of the reflected virtual Line-of-Sight (vLoS) beam, presenting design tradeoffs when scaling within compact edge environments [11].

2 Quantization Granularity and Path Loss: The hardware utilizes a cost-effective 2-bit discrete phase resolution scheme to avoid expensive continuous phase shifters [9, 10]. Although this drastically lowers fabrication costs, it bounds the maximum phase-quantization error to $\pm 45^{\circ}$, introducing an unavoidable peak-gain degradation compared to idealized arrays [13, 26].

3 Edge Compute and Memory Scaling: The CD-PM framework maps phases linearly ($O(K \cdot |\ \Phi\ |)$) to allow real-time execution on a low-power ARM Cortex-M4 microcontroller [17, 18]. However, as the element count (K) scales past hundreds of nodes, the serial search loop will scale linearly in execution time, eventually straining the 45 ms real-time processing window and exceeding edge microprocessor SRAM capacities [20, 28].

4 Dynamic Tracking Latency: The closed-loop optimization window relies entirely on continuous, real-time RSSI voltage sampling via DMA channels [17]. In highly dynamic, fast-fading 6G environments with rapidly moving

physical blockages, the 45 ms optimization cycle may encounter tracking lag without predictive tracking extensions [21, 29].

Quantitatively, with a 2-bit phase set size of four ($|\Phi| = 4$) and an MCU clock speed of 168 MHz, the calculation shows $T_{comp} \approx K \times 0.703\, ms$. Currently, utilizing the prototype array where K = 64, the optimization core routine converges in less than $45\, ms$. However, algorithmic scaling projections for larger meta-surfaces reveal significant operational bottlenecks. When the element count hits $K \leq 128, 12 \times 12$ or 16×16 setup, the sequential search exceeds the $45\, ms$ limit thereby inducing tracking lag. To scale this framework to massive surfaces, future iterations must transition from a purely serial search to parallelized sub-array sectioning or multi-core edge architectures.

6 Conclusion and Future Work

The proposed paper effectively showcased the design and testing of HIL RIS optimization platform with a central frequency of 28 GHz. In order to address the gap between purely theoretical modeling and actual hardware implementation, a CD-PM algorithm specific to the local environment was designed and implemented on the embedded microcontroller directly. Instead of using complicated channel estimation, the proposed methodology accounts for physical losses associated with the PIN-diode hardware and 2-bit quantization through the use of RSSI feedback mechanism. Additionally, the entire process was completed in just 45 ms, proving its feasibility for real-time beamforming. Future research will focus on scaling the existing framework from the single-surface 8×8 element arrangement to multi-surface distributed cooperative arrangements for dealing with multiple user interference. Furthermore, studies will also be conducted on incorporating predictive machine learning techniques with ultra-low computational complexity at the edge to enable predictive phase tracking in fast fading channels. Finally, investigation will also be conducted on incorporating this particular hardware configuration with multi-band sub-THz architectures for future scalability. Finally, to overcome the bottleneck effect caused by serial processing on arrays that are larger than K = 128, future research will investigate hardware-level parallelization. This will involve transitioning from the current serial ARM Cortex-M4 implementation to parallelized architectures, such as multi-core MCUs or FPGA-based sub-array processing, to maintain sub-45 ms optimization cycles in large-scale configurations.

Author contributions

The corresponding and sole author (Zacheous Aasa) was entirely responsible for the conceptualization, methodology development, and algorithmic design of the localized Coordinate Descent Phase Mapping (CD-PM) framework. The author engineered, programmed, and fabricated the physical 8×8 passive Reconfigurable Intelligent Surface prototype at 28 GHz. The author built the Hardware-in-the-Loop (HIL)

experimental testbed, conducted the performance verification measurements inside the anechoic chamber, and executed all data curation and formal analysis. Finally, the author drafted, illustrated, reviewed, and approved the final version of the manuscript for submission

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Data availability

The experimental raw telemetry, RSSI measurement datasets, and embedded microcontroller optimization code generated during the current study are not publicly deposited due to ongoing system expansions but are available from the corresponding author upon reasonable request.

Declarations

Ethical Approval

Not applicable.

Consent to participate

Not applicable.

Consent for publication

Not applicable

Competing interests

The authors declared no competing financial or non-financial interest

Generative AI Disclosure

During the preparation of this manuscript, the author used generative AI solely to improve the grammatical structure, refine the language, and format the reference list. The core technical ideas, algorithmic design, and hardware experiments were entirely executed by the author, who holds full accountability for the content.

Policy statement

The findings and interpretations presented are solely those of the author and do not reflect the views of any person, agency, or institution. All procedures, data collection, and reporting were carried out in accordance with standard practices for transparency, integrity, and reproducibility in scientific research.

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