Extended Data

A Low-Power Biomimetic Cryptography Engine for *All-In-One* IoT based on Programmable and Multifunctional MoS_2 FETs

Akhil Dodda[1] and Saptarshi Das[1,2,3,]*

[1]*Department of Engineering Science and Mechanics, Pennsylvania State University, University Park, PA 16802, USA*

[2]*Department of Materials Science and Engineering, Pennsylvania State University, University Park, PA 16802, USA*

[3]*Materials Research Institute, Pennsylvania State University, University Park, PA 16802, USA*

Extended Data 1

Table S1: Benchmarking Emerging IoT Platforms					
Material		*Sensing*	*Storage*	*Security*	*Reference*
2D	MoS_2	Y	N	N	[1]
	MoS_2, WS_2, $MoSe_2$, WSe_2	N	Y *(Electronic)*	N	[2]
	WSe_2/MoS_2/h-BN/HfS_2/WSe_2/MoS_2	N	Y *(Electronic)*	N	[3]
	Graphene/$MoS_{2-x}O_x$/Graphene	N	Y *(Electronic)*	N	[4]
	Graphene/MoS_2	N	Y *(Electronic)*	N	[5]
	Graphene/h-BN/MoS_2	N	Y *(Electronic)*	N	[6]
	Graphene/h-BN/MoS2	N	Y *(Electronic)*	N	[7]
	Graphene/MoS_2	Y	Y *(Optical)*	N	[8]
	h-BN/WSe_2-h-BN/WSe_2	Y	Y *(Optical)*	N	[9]
	MoS_2/PTCDA	Y	Y *(Optical)*	N	[10]
	MoS_2/Au-Nano Particles	Y	Y *(Optical)*	N	[11]
	WSe_2/h-BN	Y	Y *(Optical)*	N	[12]
	MoS_2/PbS	Y	Y *(Optical)*	N	[13]
	BP/Al_2O_3	N	Y *(Electronic)*	N	[14]
	BP/h-BN/MoS_2	N	Y *(Electronic)*	N	[15]
	BP/Al_2O_3/BP/Al_2O_3	N	Y *(Electronic)*	N	[16]
	MoS_2/Metal Nano Crystal	N	Y *(Electronic)*	N	[17]
	MoS_2	Y	N	N	[18]
	MoS_2	Y	Y *(Electronic)*	N	[19]
	MoS_2/PZT	Y	Y *(Electronic)*	N	[20]
	WSe_2	Y	N	N	[21]
	MoO_x/MoS_2	N	Y *(Electronic)*	N	[22]
	MoS_2	N	N	Y	[23]
Oxide Based Memristors	Ag:SiO_2 or MgO/HfO_2:Ag	N	Y *(Electronic)*	N	[24]
	TiN/TaO_x/$HfAl_yO_x$/TiN	N	Y *(Electronic)*	N	[25]
	ITO/LaAlO3/SrTiO3	N	Y *(Electronic)*	N	[26]
	Ag_2S	N	Y *(Electronic)*	N	[27]
	Indium Gallium Zinc Oxide (IGZO)	N	Y *(Electronic)*	Y	[28]
	Al_2O_3/TiO_{2-x}	N	Y *(Electronic)*	Y	[29]
	Ag:SiO_2	N	Y *(Electronic)*	Y	[30]
	Ag:SiO_2	N	Y *(Electronic)*	Y	[31]
	TiO_2	N	Y *(Electronic)*	Y	[32]
2D	***This Work***	***Y***	***Y (Electronic)***	***Y***	

<u>***Extended Data 2***</u>

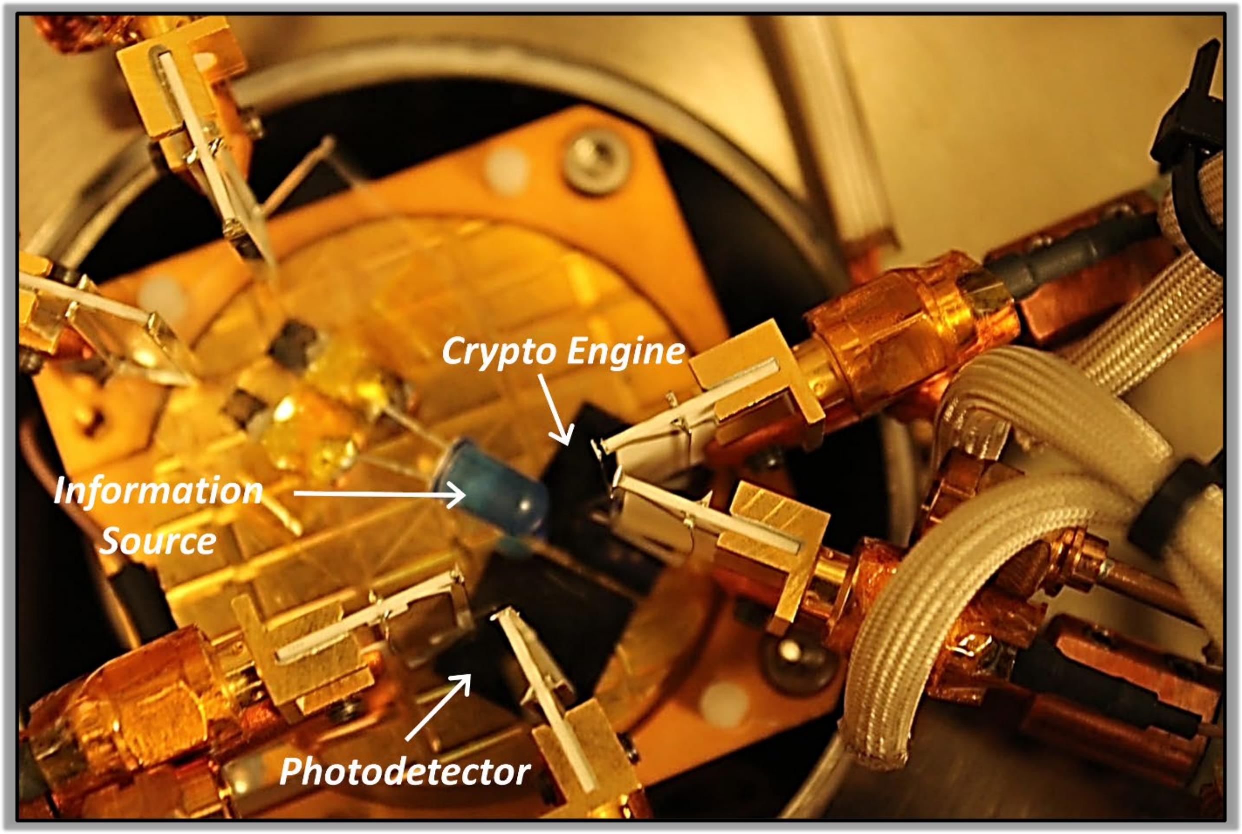


Figure S1: *Experimental setup of all-in-one IoT platform. We have used two chips both containing MoS_2 FETs for the prototype demonstration. One of the chips is used as the photodetector, whereas the other chip is used as the encoder. The encoding chip contains the current adder (CA), look-up-table based white Gaussian noise (WGN) generator, and the artificial neuron (AN). A blue light emitting diode (LED) is used as the source of information. Due to limited number of probes available in our measurement system, we performed the experiments in the following sequence: first, the 8×8 pixelated image of the letter 'N' was converted to a 64×1 array of LED voltages (V_{LED} = 0 V for dark pixel and V_{LED} = 5 V for the bright pixel). In this step we converted the spatial information into a temporal one. Next, we obtained the corresponding photocurrent (I_{PH}) response from the MoS_2 photodetector by illuminating the LED. Naturally, I_{PH} is also a 64×1 array. Next, we programmed 64 MoS_2 FETs in the encoder chip and recorded the corresponding current $I_{NOISE} = [I_1\, I_2\, I_3 \ldots . I_{64}]$ at V_{BG} = 0 V. The threshold voltages of these FETs were programmed such that the conductance values (G_M) at V_{BG} = 0 V follow random Gaussian distribution of a predefined standard deviation (σ). Next, we used the current adder to add these two arrays, i.e. I_{PH} and I_{NOISE}, and obtain another 64×1 array of the post-synaptic voltage (V_{PSV}). Finally, this 64×1 array of V_{PSV} was applied to the AN to obtain 64×1 array of the postsynaptic current. These experiments were repeated for different (σ) and for different encoding threshold (V_{ST}) of the AN.*

Extended Data 3

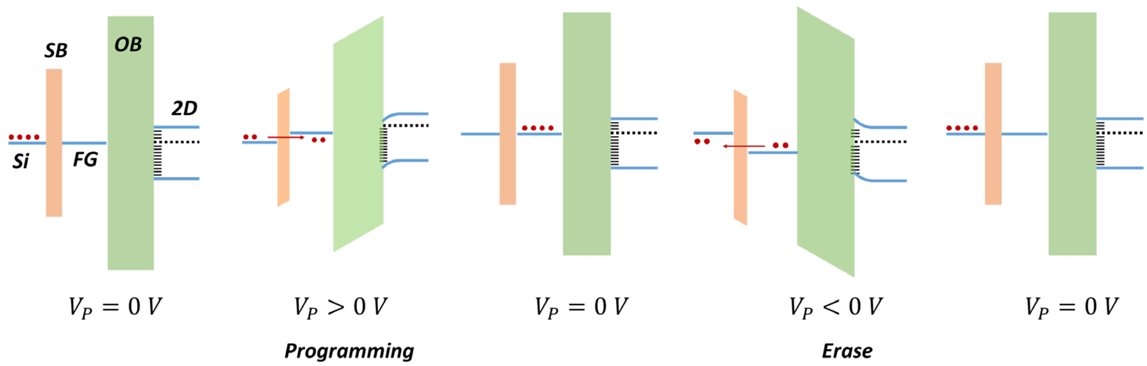


Figure S2: *Energy band diagrams showing the programming and erase operations. The interface between the control gate (CG) i.e. p^{++}-Si and the floating gate (FG), i.e. TiN/Pt metal stack is characterized by a Schottky barrier (SB), which is shown as a rectangular potential barrier for simplicity. Further, 50 nm Al_2O_3 is represented by an oxide barrier (OB). The OB is much wider and taller compared with the SB. This gate stack closely resembles the FG configuration used in non-volatile flash memories. When a "Write" programming pulse, V_P, is applied to the CG, charge carriers tunnel from the p^{++}-Si into the Pt/TiN FG and remains trapped even when V_P is released. These negative fixed charges on the FG screen the electric field from CG and thereby makes the V_{TH} more positive. The total amount of charge injected into the FG, and hence shift in V_{TH} of the MoS_2 field effect transistor (FET) can be controlled by the amplitude, and duration, of the "Write" programming pulses. The device can also be restored to its initial state by removing the trapped charges from the FG by applying a negative V_P or 'erase' pulse to the CG.*

Extended Data 4

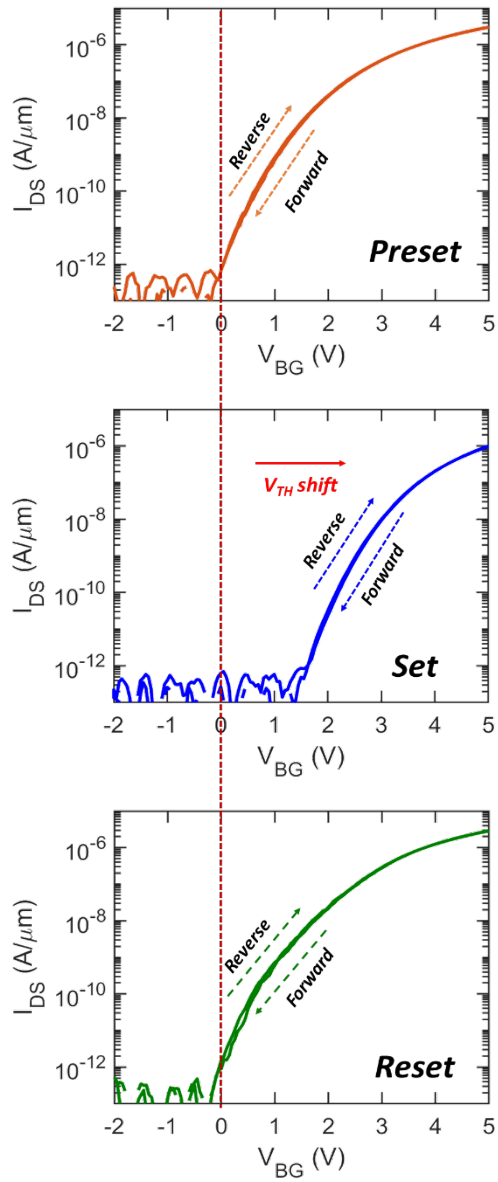


Figure S3: *Transfer characteristics of representative MoS_2 FET measured at V_{DS} = 1 V before programming (Preset), after programming (Set), and after erasing (Reset).*

Extended Data 5

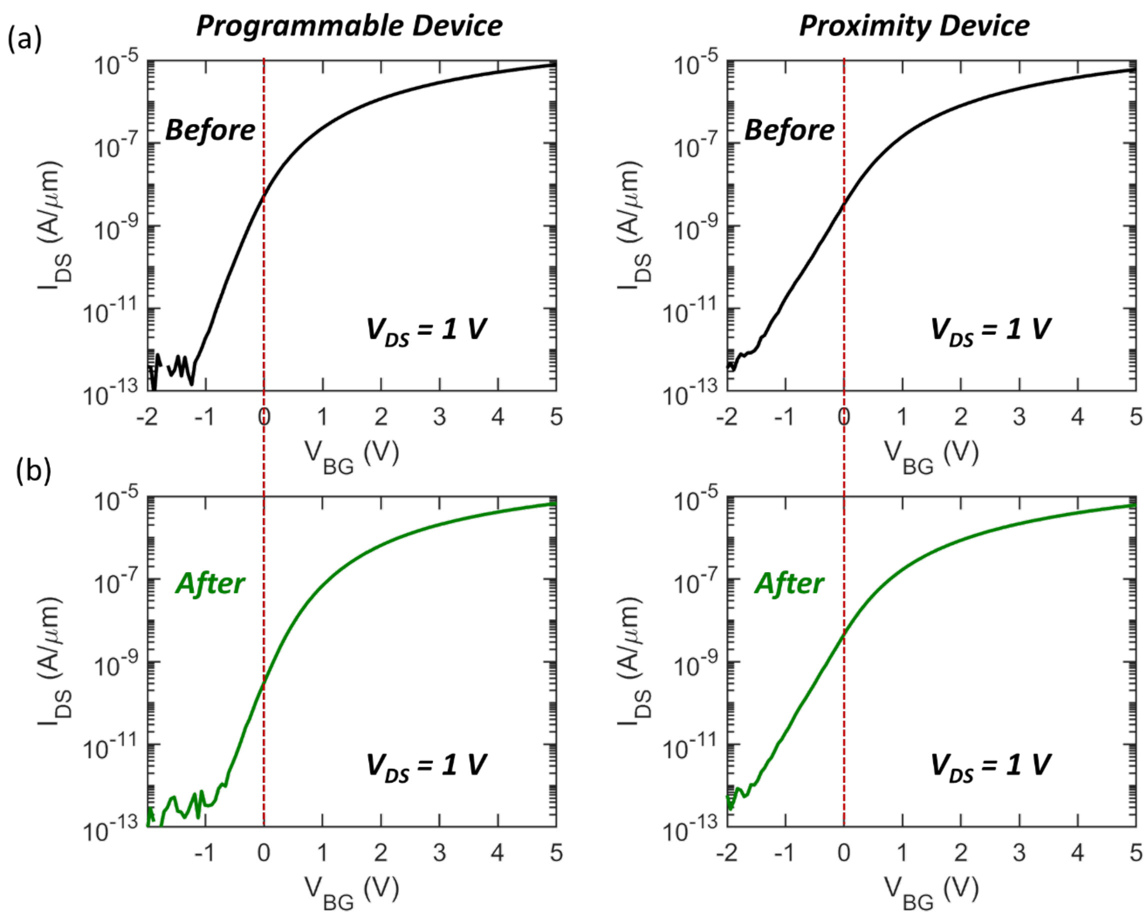
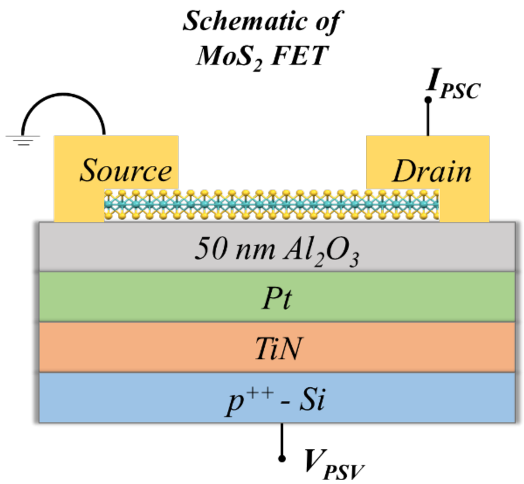


Figure S4: *a) Transfer characteristics of two adjacent MoS_2 FETs one of which is intended to be programmed while the other one is intended to be kept at its original state. b) Corresponding transfer characteristics after the intended device has been programmed. As expected, the programmed device showed a positive shift in threshold voltage, whereas the not-programmed device remains unaltered following the initial transfer characteristics. This confirms the fact that although our back-gate stack is global, programming operation can be performed on individual MoS_2 FETs without impacting the adjacent devices*

Extended Data 6



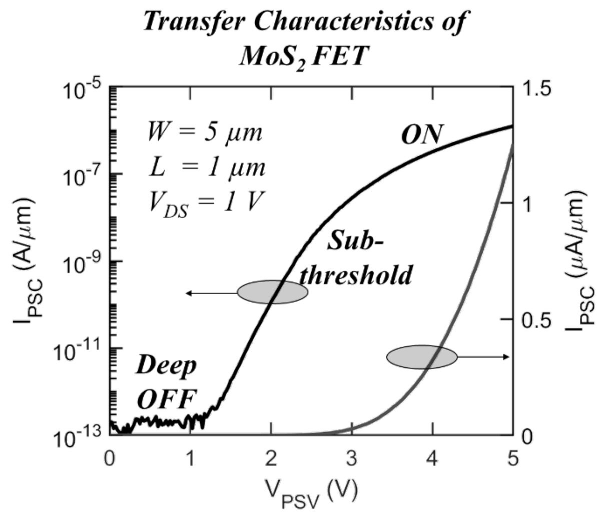


Figure S5: *Schematic and transfer characteristics of the MoS_2 artificial neuron (AN) with pre-synaptic voltage (V_{PSV}) applied to the back-gate terminal and post-synaptic current (I_{PSC}) measured at the drain terminal with a drain bias, $V_{DS} = 1$ V, in both linear and logarithmic scale. The encoding threshold was programmed to be V_{TH} = 1.5 V, such that the presynaptic voltage pulses (V_{PSV}) obtained from the MoS_2 white Gaussian noise adder (WGNA) are primarily subthreshold with occasional threshold crossing events due to the addition of the white Gaussian noise (WGN).*

Extended Data 7

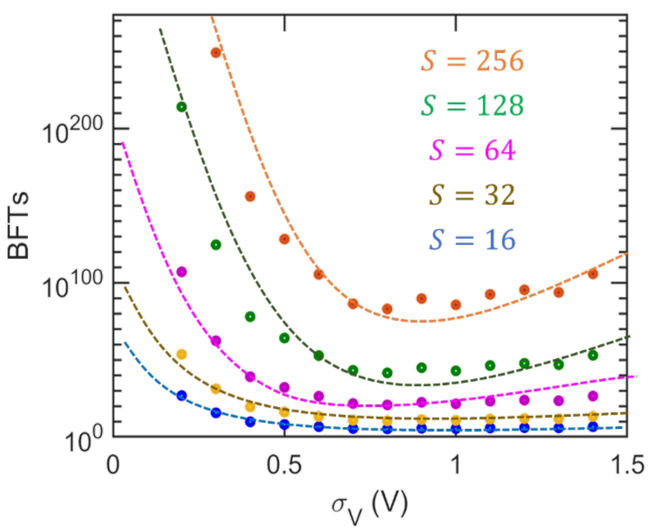


Figure S6: *BFTs required to decode the letter 'N' as a function S for different σ_V.*

Extended Data 8

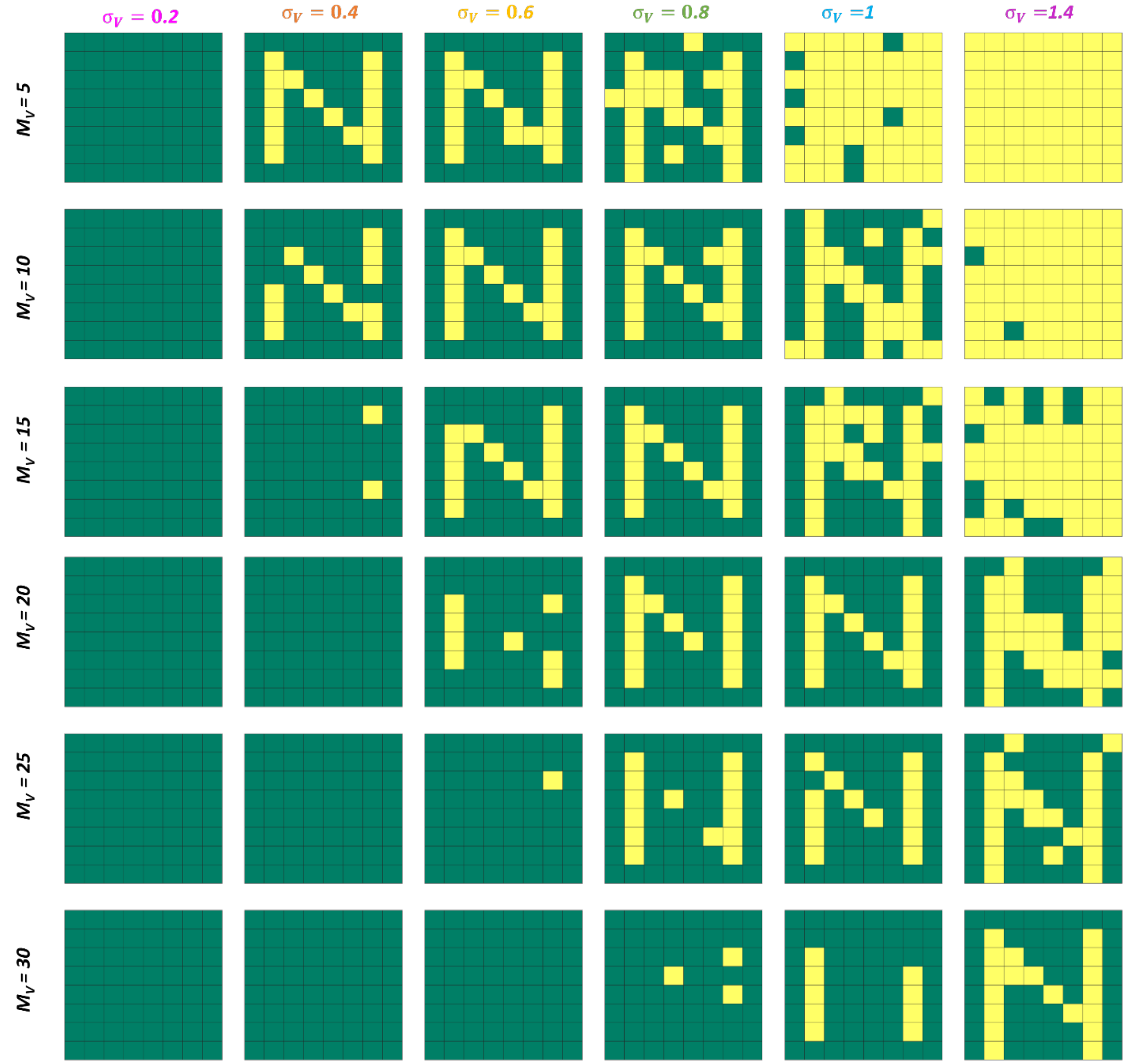


Figure S7: *Decoding of the images of the letter 'N' , for different σ_V and for different number of mandated votes (M_V) required to mark a pixel as bright for P = 50.*

Extended Data 9

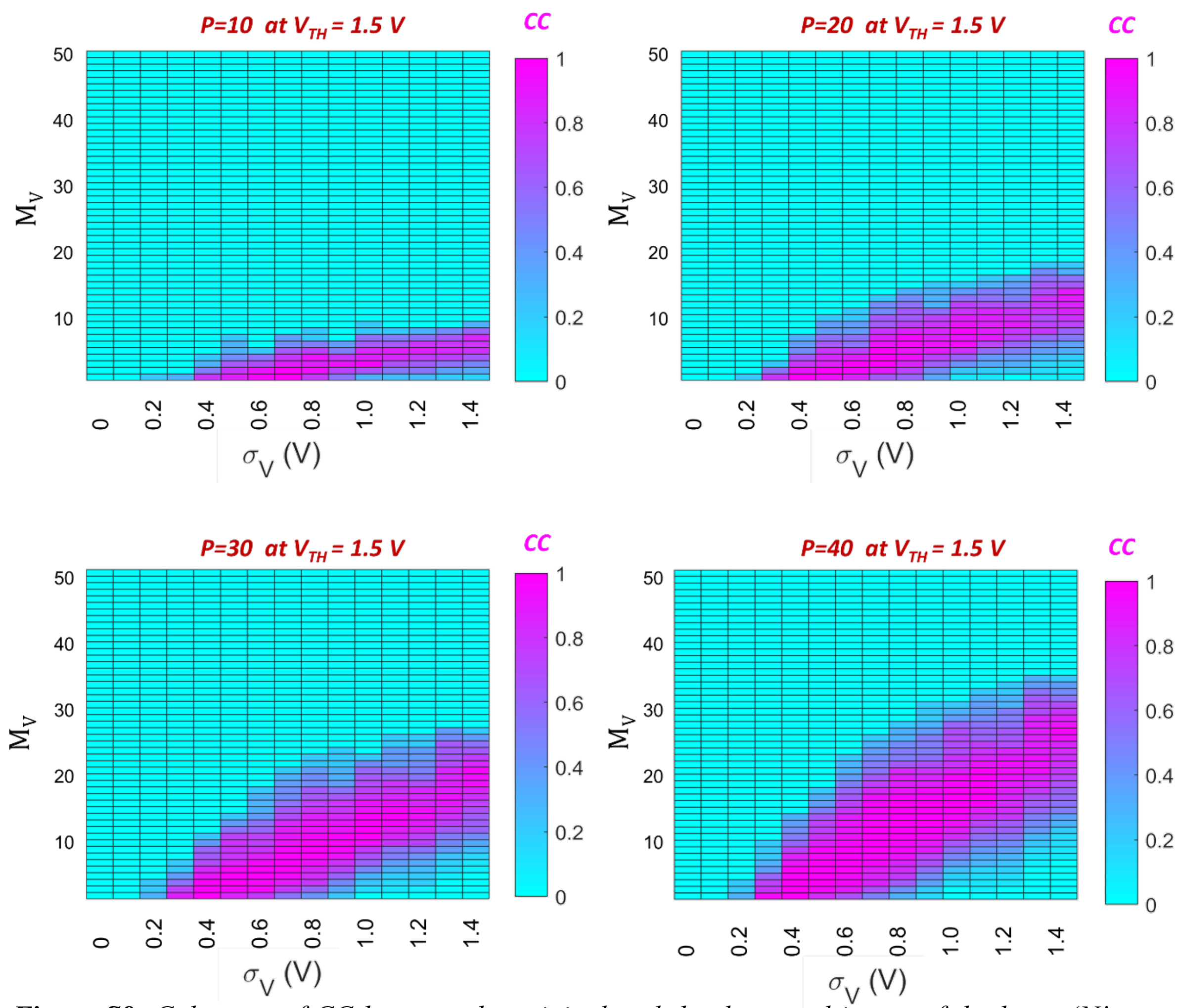


Figure S8: *Colormap of CC between the original and the decrypted image of the letter 'N' as a function of σ_V and M_V, when encryption is done by different size of encoding population (P) with encoding threshold of V_{TH} = 1.5 V. As expected, the optimum number of M_V for accurate decryption is found to be different for similar σ_V. Therefore, without the prior knowledge of the σ_V and P, used by the biomimetic encoder it is difficult to decode the information.*

Extended Data 10

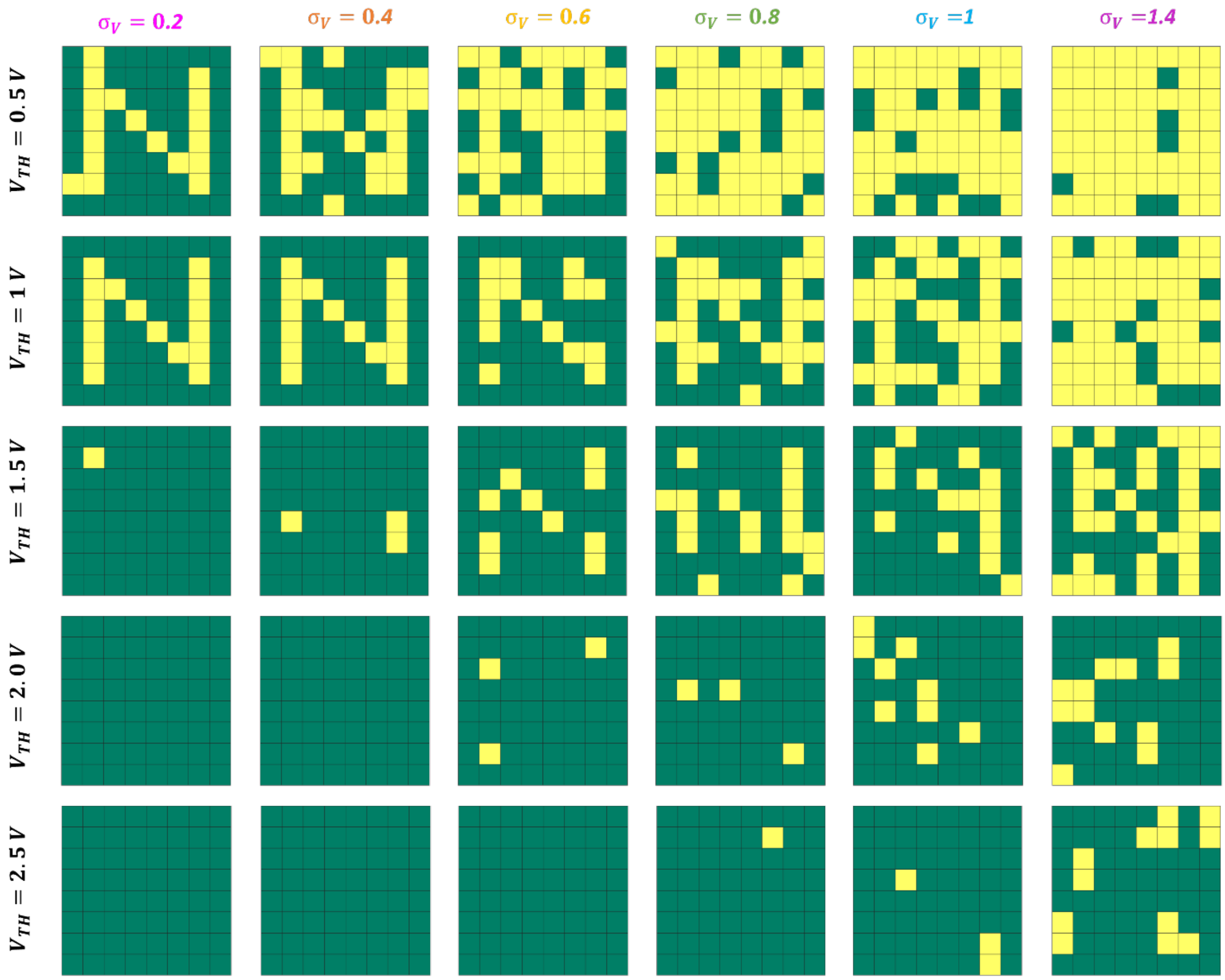


Figure S9*: The encryption of the letter 'N', by encoders with different V_{TH}, at different σ_V. If $V_{PSV} > V_{TH}$, the encryption process or the communication is insecure. For V_{TH} values slightly greater than V_{PSV}, there are more threshold crossing events even for low σ_V, whereas, for V_{TH} values further from V_{PSV}, there are limited threshold crossing events even for high σ_V.*

Extended Data 11

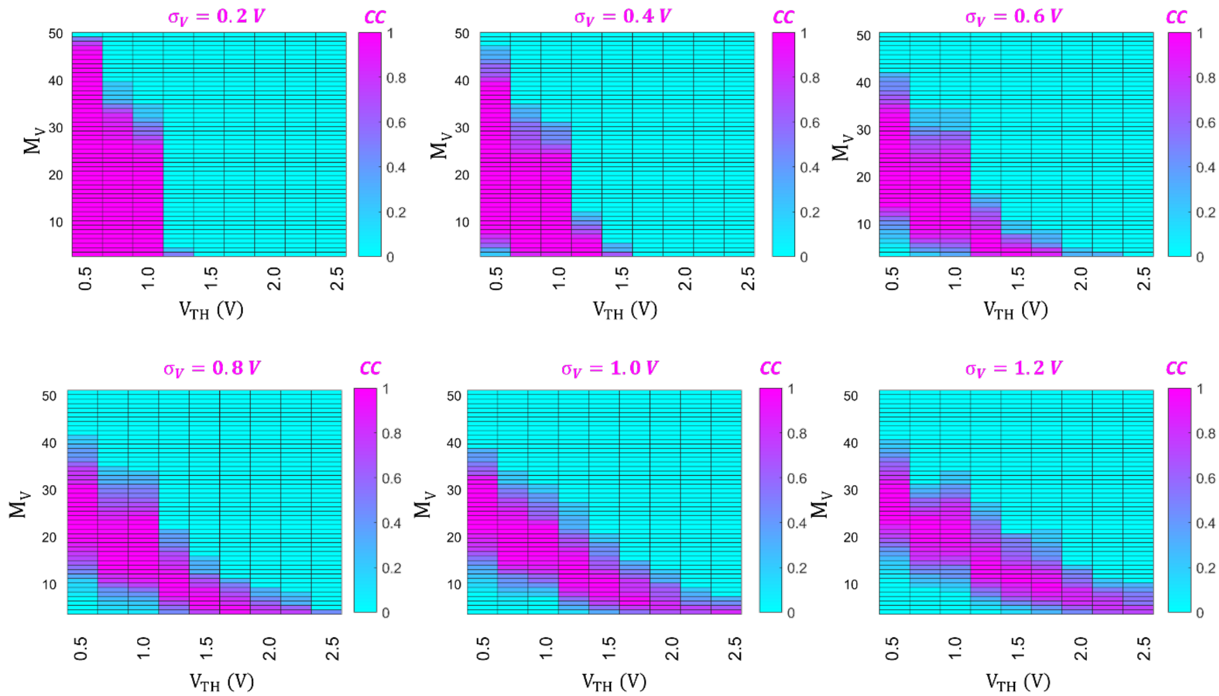


Figure S10: *The colormap of CC between the original and the decrypted image of the letter 'N' as a function of* V_{TH} *of the encoder and* V_M *mandated by the decoder for various* σ_V *at a given population size of P=50.*

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