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Finite Element Investigation of Process Variables in Indium-Based Flip Chip Interconnects

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Research Article

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Finite Element Investigation of Process Variables in Indium-Based Flip Chip Interconnects

A CAD-Driven Computational Analysis Framework

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Abstract

Thermo-compression bonding utilizing indium bumps represents a critical enabling technology for advanced microelectronic systems, particularly in applications involving infrared detection arrays and high-performance integrated circuits operating under extreme thermal environments. Mechanical integrity and long-term reliability of these assemblies depend fundamentally on thermo-mechanical phenomena arising from interface contact mechanics, thermal property differentials among constituent materials, and bonding process parameters including applied pressure and temperature. This investigation presents comprehensive finite element simulations of a representative flip chip structure incorporating Read-Out Integrated Circuit (ROIC) silicon substrate, GaSb-based detector die, electroplated gold metallization pads, and indium solder interconnects, developed entirely within the Autodesk Fusion 360 CAD-simulation framework. Structural analysis under representative bonding loads demonstrates that indium interconnects function as principal stress-absorbing components, experiencing peak equivalent stress values approaching 876.9 MPa localized at bump-metallization boundaries, whereas semiconductor substrates maintain stress levels well below material yield thresholds. Structural margin assessment reveals localized yielding at interconnect interfaces with minimum safety factors near 0.236, while global assembly displacement reaches a maximum of 0.024 mm concentrated at the detector surface. Interface contact mechanics analysis indicates effective pressure distribution

peaking at 808 MPa across bump-pad contact zones. Thermal simulations performed at liquid nitrogen temperature (77 K) establish that indium bumps constitute dominant thermal conduction pathways, with concentrated heat flux and temperature gradient distributions manifesting at metallization interfaces. The observed interdependence between contact pressure and thermal transport characteristics underscores the coupled nature of mechanical bonding quality and heat transfer performance. Results furnish quantitative design guidance for process parameter selection in indium bump interconnect manufacturing, with particular relevance to cryogenic sensor assemblies and infrared focal plane array applications.

Keywords: thermo-compression bonding; indium interconnect technology; computational mechanics; thermal-structural coupling; focal plane array packaging; Von Mises failure criterion; Read-Out IC integration; CAD-based simulation; Autodesk Fusion 360

1. Introduction

1.1 Technological Foundation of Flip Chip Interconnection

Contemporary microelectronic packaging increasingly relies upon flip chip architectures as a preferred interconnection methodology for establishing electrical and mechanical coupling between semiconductor devices and supporting substrates. Distinguished from traditional wire-bond configurations, this approach positions the active device surface in inverted orientation, enabling direct metallurgical contact through arrays of conductive bumps. Such architectural arrangements yield substantial performance advantages: interconnect path lengths experience dramatic reduction, parasitic circuit elements including resistance and inductance decrease correspondingly, and enhanced thermal dissipation pathways emerge naturally from the direct chip-to-substrate mechanical interface. These characteristics translate into measurable improvements in signal transmission fidelity, achievable input/output density, and thermal management capability.

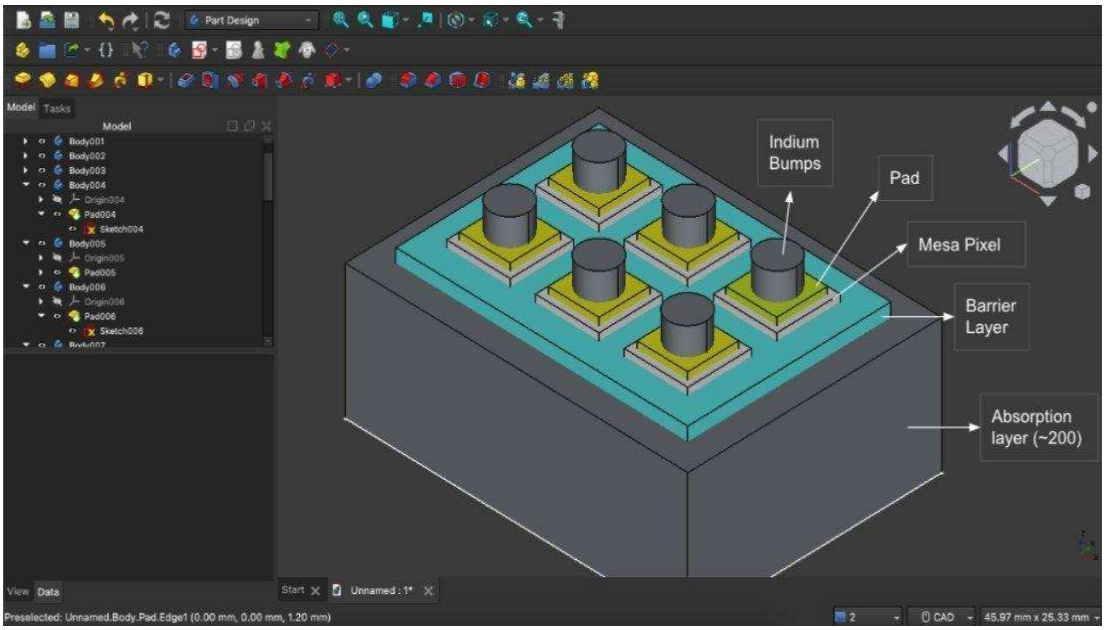


Fig. 1: Three-dimensional CAD representation of detector chip assembly showing indium bump interconnects, metallization pads, mesa pixel structures, barrier layer, and absorption layer (FreeCAD modeling environment)

Application domains for this technology span diverse fields including advanced computing processors, infrared sensing instrumentation, focal plane detector arrays, microelectromechanical devices, and integrated system-on-chip implementations. Ongoing trends toward dimensional miniaturization and functional density escalation drive continued demand for robust, high-density interconnect solutions. Consequently, flip chip bonding methodologies occupy an increasingly central role in state-of-the-art packaging design frameworks.

1.2 Critical Role of Bonding Process Variables

Flip chip assembly processes fundamentally involve simultaneous application of controlled thermal and mechanical loading to achieve reliable metallurgical bonds between bump structures and corresponding substrate pads. Throughout this operation, the multi-material assembly experiences complex thermo-mechanical interactions stemming from elastic modulus differentials, thermal expansion coefficient mismatches, and geometric constraint conditions.

These phenomena generate localized stress and strain concentrations, particularly concentrated at interface boundaries between dissimilar materials.

Interconnect quality depends critically upon appropriate selection and control of multiple process variables: bonding temperature magnitude, applied mechanical force, bump dimensional characteristics, interconnect pitch spacing, and constituent material properties. Insufficient thermal input may prevent adequate plastic flow, resulting in electrically inadequate or mechanically weak joints. Conversely, excessive temperature exposure risks undesirable interdiffusion phenomena or thermal degradation of active semiconductor layers. Similarly, mechanical loading below critical thresholds produces bonds with insufficient strength and reliability, while excessive pressure application may induce bump structural collapse, substrate mechanical distortion, or damage to fragile detector layers. Precise process parameter specification and monitoring therefore constitute essential requirements for achieving consistent bonding outcomes and ensuring long-term interconnect performance.

1.3 Indium as Interconnect Material

Within the range of solder materials employed for flip chip interconnection, indium exhibits distinctive properties that render it particularly suitable for applications demanding exceptional mechanical compliance combined with stable cryogenic operation. Material characteristics include notably low yield strength (approximately 1.5 MPa at room temperature), substantial ductility enabling large plastic deformation without fracture, excellent thermal transport capability (thermal conductivity near 82 W/m·K), and favorable electrical conductance. These attributes facilitate plastic flow under moderate compression forces, promoting intimate metallurgical contact at bonding interfaces while simultaneously limiting stress concentration magnitudes that might otherwise threaten adjacent components.

Indium-based interconnection finds particular application in cryogenic instrumentation and infrared detector systems, where assemblies must maintain mechanical and electrical stability across substantial temperature excursions during both operational cycling and manufacturing processes. The capacity of indium to accommodate thermal expansion differentials between semiconductor and substrate materials substantially reduces interconnect fracture probability during thermal cycling exposure. However, the inherent mechanical softness introduces

corresponding process sensitivity: inappropriate selection of bonding parameters—including pressure magnitude, temperature profile, or bump geometry—can produce non-uniform plastic deformation, premature structural collapse, or excessive residual stress accumulation. These considerations underscore the necessity for rigorous process analysis and optimization.

1.4 Constraints of Purely Empirical Investigation

Traditional development methodologies for flip chip bonding processes have historically relied upon iterative experimental optimization involving repeated fabrication trials and subsequent characterization. While physical experimentation remains indispensable for process validation and qualification, this approach carries inherent limitations. Manufacturing test vehicles requires substantial time investment and material consumption, particularly when working with microscale interconnect geometries and specialized material systems.

Furthermore, experimental characterization provides limited insight into internal thermo-mechanical behavior including three-dimensional stress distributions, localized strain concentrations, and transient thermal gradient evolution within bonded structures.

Direct mechanical measurement at interconnect interfaces presents substantial technical challenges arising from submillimeter dimensional scales and physical inaccessibility of buried contact zones. Consequently, failure mechanisms such as progressive residual stress accumulation or localized plastic deformation often remain inadequately characterized when relying exclusively on experimental methods. These practical constraints motivate integration of computational modeling approaches into flip chip bonding investigation frameworks.

1.5 Finite Element Modeling in Packaging Analysis

Computational mechanics utilizing finite element analysis (FEA) in conjunction with computer-aided design environments has emerged as an effective and widely validated methodology for investigating complex microelectronic packaging phenomena. Through construction of geometrically detailed models, assignment of physically representative material constitutive behavior, and specification of appropriate loading and constraint conditions, FEA

enables prediction of thermal distributions, mechanical stress states, and deformation fields throughout flip chip structures during bonding operations and subsequent thermal excursions.

CAD-integrated simulation frameworks offer substantial advantages in development efficiency and parametric design flexibility. Systematic variation of bonding temperature, applied pressure, or interconnect geometry enables comprehensive evaluation of individual and interactive parameter effects without physical prototype fabrication. This capability supports early-stage identification of critical process variables governing bond integrity, reduces development cycle duration and material expenditure, and facilitates data-informed design decisions by establishing quantitative relationships between process inputs and measurable performance outcomes.

1.6 Investigation Scope and Objectives

Prior research contributions have examined numerous aspects of flip chip interconnection, encompassing bump metallurgy selection, bonding mechanism characterization, and reliability assessment under operational conditions. Computational investigations have advanced understanding of temperature field evolution, residual stress development, and mechanical deformation behavior. Nevertheless, existing studies frequently address isolated aspects of the bonding process or focus on specific material combinations, and comprehensive simulation frameworks simultaneously addressing multiple process parameters within unified CAD environments remain relatively scarce in published literature.

The present investigation addresses this gap through development of a representative three-dimensional CAD-based model of a complete flip chip assembly and execution of coupled mechanical-thermal finite element analysis. Specific research objectives include: (i) construction of a geometrically and materially accurate flip chip model incorporating ROIC silicon substrate, GaSb detector chip, electroplated gold pads, and indium solder bumps; (ii) execution of static structural analysis under representative bonding loads with characterization of structural safety margins, equivalent stress distributions, displacement fields, strain concentrations, and contact pressure distributions; (iii) execution of steady-state thermal analysis under cryogenic boundary conditions at 77 K with characterization of heat flux pathways and thermal gradient distributions; and (iv) interpretation of coupled thermo-mechanical simulation results in the context of bonding parameter optimization for indium-based flip chip manufacturing, with emphasis on cryogenic and infrared sensing applications.

Computational Methodology

1.7 Computational Platform and Analysis Strategy

All geometric modeling and numerical simulation activities were performed utilizing Autodesk Fusion 360 (Education License), a unified platform integrating parametric solid modeling capabilities with finite element analysis functionality. Two independent simulation studies were configured and executed: a static structural analysis to evaluate mechanical response characteristics under bonding load application, and a steady-state thermal stress analysis to evaluate heat transfer behavior under cryogenic temperature boundary conditions. This bifurcated approach permitted isolated examination of each loading condition while maintaining consistency in geometric definition and material property specification across both analyses.

1.8 Geometric Model Development

The flip chip assembly geometry was constructed through sequential solid modeling operations. Principal structural elements included: (i) ROIC silicon chip, represented as a rectangular prismatic solid body; (ii) GaSb-based detector chip, positioned in symmetric inverted orientation above the ROIC substrate; (iii) electroplated gold metallization pads deposited on opposing chip surfaces; and (iv) spherical indium solder bumps bridging corresponding pad pairs across the interconnect gap.

Each functional component—semiconductor substrates, metallization pads, and solder bumps—was created as a discrete solid body rather than employing merged or Boolean-combined geometry. This modular construction approach proved essential for enabling independent material property assignment to individual components and for defining physically realistic contact interface behavior at component boundaries during subsequent simulation.

Geometric symmetry between opposing chips was maintained throughout modeling to ensure uniform load distribution in the final assembly.

Intersecting or overlapping volumes at bump-pad interface regions were resolved through solid body splitting and redundant volume removal operations, producing physically valid contact geometries free from non-physical stress artifacts that might otherwise arise from geometric interference.

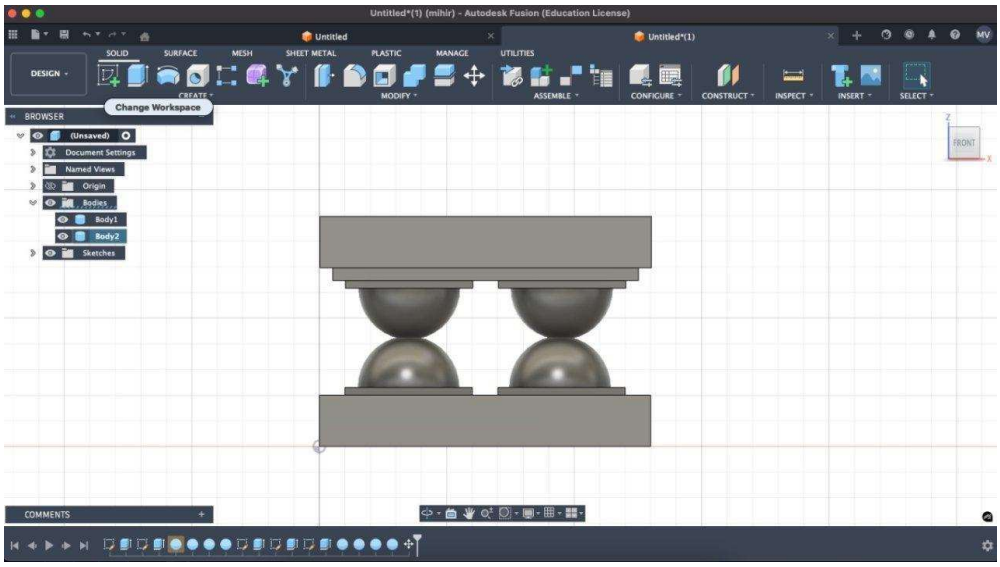


Fig. 2: Frontal elevation view of flip chip assembly in Autodesk Fusion 360 environment, illustrating semiconductor chip components and indium solder bump interconnects

1.9 Material Constitutive Property Assignment

Material property specification was performed following completion of geometric model construction. Standard material definitions from the Fusion 360 material library were employed where applicable; custom material entries were created for materials absent from the default database. Silicon material properties were assigned to the ROIC chip component; gold properties were applied to metallization pad bodies. Indium and gallium antimonide (GaSb) were defined through manual entry of mechanical and thermal property values extracted from published materials databases and peer-reviewed literature sources.

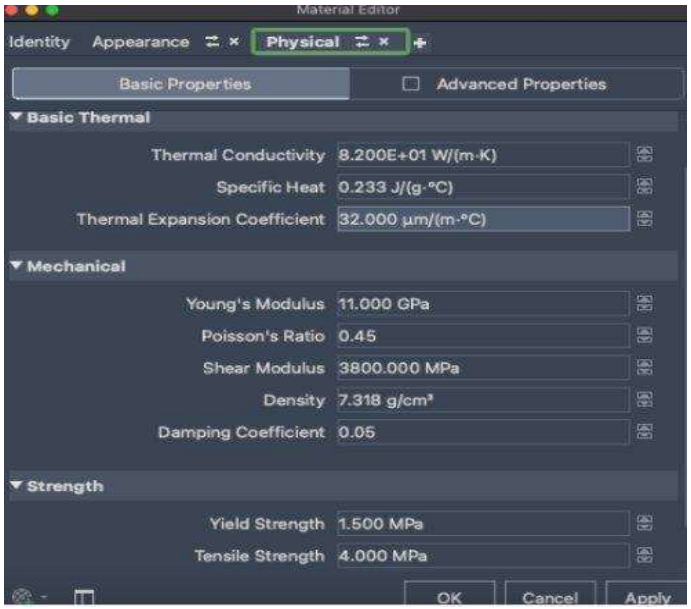


Fig. 3: Material property editor interface displaying thermal, mechanical, and strength characteristics defined for indium

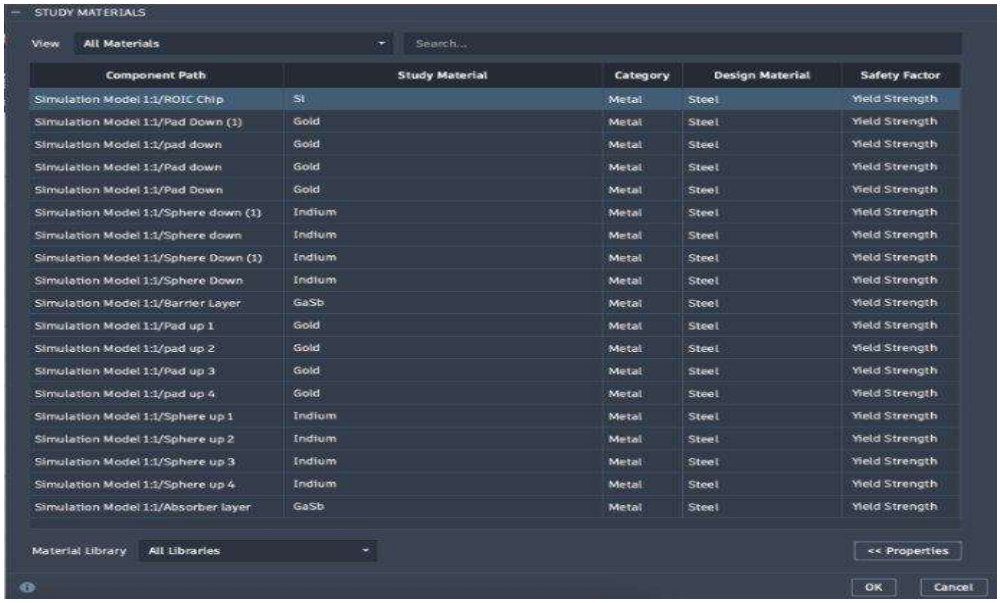


Fig. 4: Study materials panel illustrating component-material assignment relationships across all simulation solid bodies

Table 1. Material Constitutive Properties Employed in Finite Element Simulations

Material Property	Silicon (ROIC)	GaSb (Detector)	Gold (Pads)	Indium (Bumps)
Young's Modulus (GPa)	130	84	79	11.0
Poisson's Ratio	0.28	0.31	0.44	0.45
Density (g/cm³)	2.33	5.61	19.32	7.31
Thermal Conductivity (W/m·K)	148	36	318	82.0
CTE (µm/m·°C)	2.6	6.1	14.2	32.0
Yield Strength (MPa)	~7000*	~1500*	205	1.5

** Effective fracture-based strength for brittle semiconductor materials; CTE = Coefficient of Thermal Expansion.*

1.10 Loading Conditions and Constraint Specification

Assembly constraints were implemented to ensure physically realistic mechanical behavior throughout simulation. Contact pair definitions were established between indium bump surfaces and gold metallization pads, between pad bodies and chip surfaces, and between adjacent structural components, ensuring mechanical coupling among all bodies during load application. A fully constrained (fixed) boundary condition was applied at the bottom surface of the ROIC chip to simulate rigid carrier substrate attachment, preventing rigid-body translation and rotation while establishing a stable reference frame for stress and deformation computations.

For static structural analysis, uniform compressive force was applied to the upper surface of the detector chip to replicate bonding pressure application, distributed symmetrically to prevent induced bending moments or tilting effects. For thermal simulation, identical geometric configuration and constraint definitions were retained; mechanical loading was replaced with a uniform temperature boundary condition of 77 K imposed at the detector chip upper surface, representing cryogenic operational or bonding environments characteristic of infrared detector applications.

1.11 Finite Element Discretization and Convergence Assessment

Model discretization was accomplished utilizing automatically generated tetrahedral finite element meshes, with manual refinement operations applied in regions anticipated to experience elevated stress gradients—specifically within solder bump volumes and at bump-metallization interface zones. Mesh quality was verified through built-in element quality inspection utilities within Fusion 360. Multiple mesh density configurations were evaluated through systematic adjustment of global and local element size parameters until solution convergence criteria were satisfied, balancing computational accuracy requirements against available processing resources. The final mesh configuration provided adequate spatial resolution to resolve localized deformation patterns and field gradients at interconnect interfaces without imposing prohibitive computational expense.

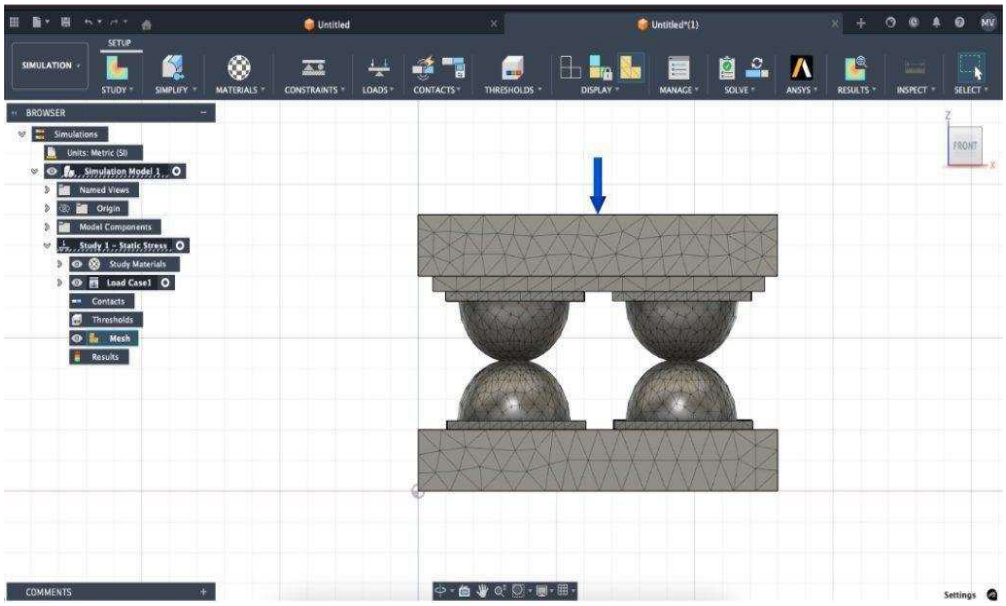


Fig. 5: Tetrahedral finite element mesh with applied compressive bonding load (directional arrow) on upper detector chip surface

2. Results and Discussion

2.1 Structural Safety Margin Distribution

Safety margin distribution under static loading quantifies the relationship between local material strength capacity and induced equivalent stress magnitude, furnishing a global reliability assessment across the complete assembly. Simulation results demonstrate that bulk assembly regions—including ROIC chip, detector chip, and gold pad zones—exhibit safety margin values substantially exceeding design thresholds, represented by blue contour regions in visualization outputs. These stiffer components develop minimal internal stress under applied bonding loads.

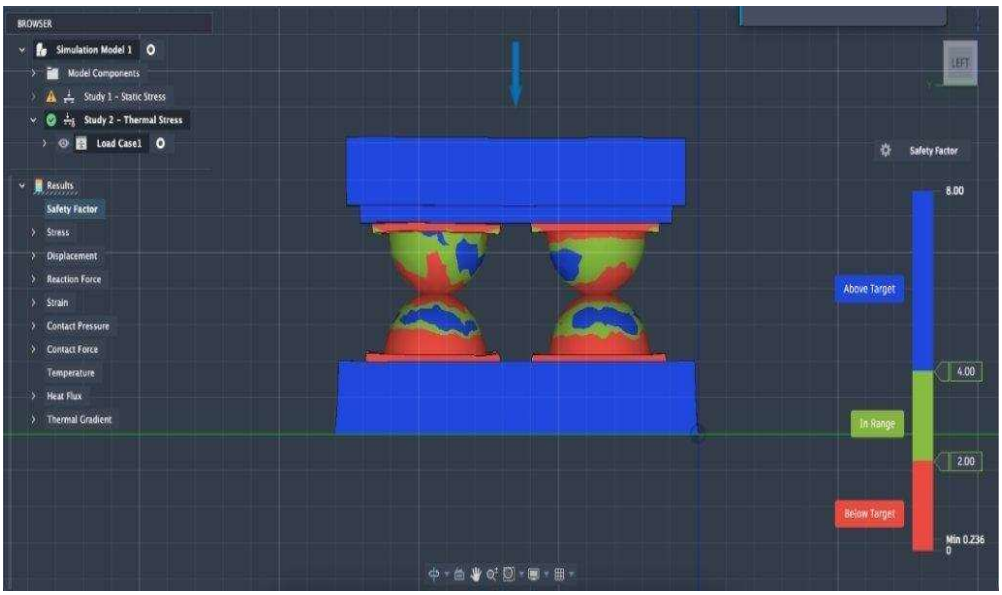


Fig. 6: Safety margin distribution showing minimum value of 0.236 at bump-metallization interface regions (Study 2 - Thermal Stress)

Conversely, indium bump regions display non-uniform safety margin distributions. Central bump volumes exhibit moderate safety margins (green contours), indicating controlled plastic yielding consistent with intended thermo-compression bonding mechanisms.

Localized minimum safety margin values approximately 0.236 occur at bump-metallization interface boundaries, where geometric curvature effects, material property discontinuities, and constrained deformation conditions combine to concentrate stress. These sub-unity values at limited interface regions do not indicate immediate structural failure; rather, localized plastic yielding in indium constitutes a deliberate bonding mechanism feature that enhances metallurgical contact formation and joint strength development. However, extension of low safety margin zones over larger spatial extents—as would result from excessive bonding force application—could precipitate premature bump collapse or long-term fatigue under thermal cycling exposure.

2.2 Equivalent Stress Field Distribution

The Von Mises equivalent stress criterion furnishes the most physically meaningful characterization of stress state in ductile materials such as indium, correlating directly with yielding initiation. Static structural simulation yields maximum Von Mises stress approximately 876.9 MPa, localized at upper and lower interfaces of indium bumps—regions where contact constraints, geometric curvature, and elastic property mismatch combine to intensify stress. The spatial pattern aligns with compressive deformation accompanied by localized shear and bending at contact boundaries, characteristic of thermo-compression bonding operations.

ROIC chip, detector chip, and pad regions exhibit substantially lower stress levels (blue-to-cyan contours), confirming that these stiffer elements function primarily as load-transferring structures rather than deforming components. Minimum stress values approximately 0.24 MPa manifest in regions distant from interconnect interfaces. The absence of widespread elevated-stress zones within chip bodies confirms that applied bonding force does not impose excessive structural risk to bulk semiconductor materials. Overall, indium interconnects absorb applied loading effectively, validating material selection strategy.

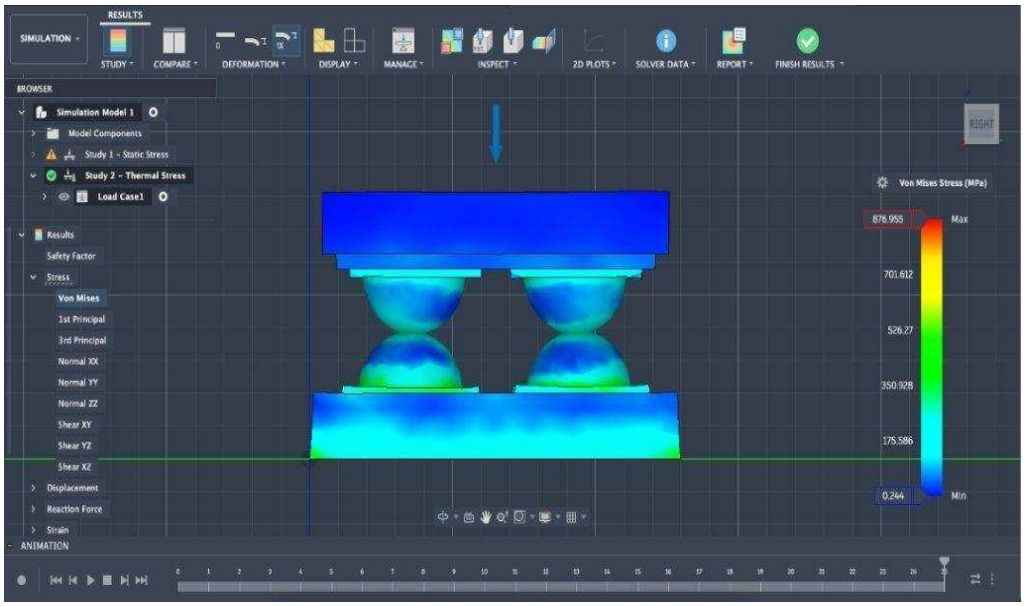


Fig. 7: Von Mises equivalent stress distribution showing peak of 876.955 MPa at bump-metallization interface regions

2.3 Global Displacement Field Distribution

Total displacement field characterizes assembly mechanical compliance under bonding load. Maximum displacement approximately 0.024 mm manifests at the upper detector chip surface, where bonding force application occurs and rigid constraints are absent. Displacement magnitude decreases progressively from detector chip through bump structures to ROIC chip, which exhibits near-zero displacement at its fixed bottom surface, confirming correct boundary condition implementation.

Indium bump regions display intermediate displacement levels (green-to-yellow contours), confirming that global deformation is accommodated predominantly by compliant solder rather than brittle chip bodies. Displacement field within bumps exhibits smooth, symmetric character, indicating uniform compressive deformation across the interconnect array without abrupt gradients or localized collapse zones.

This symmetric, predictable deformation behavior proves essential for maintaining chip planarity and alignment during bonding, and aligns with controlled bump compression objectives in thermo-compression bonding processes.

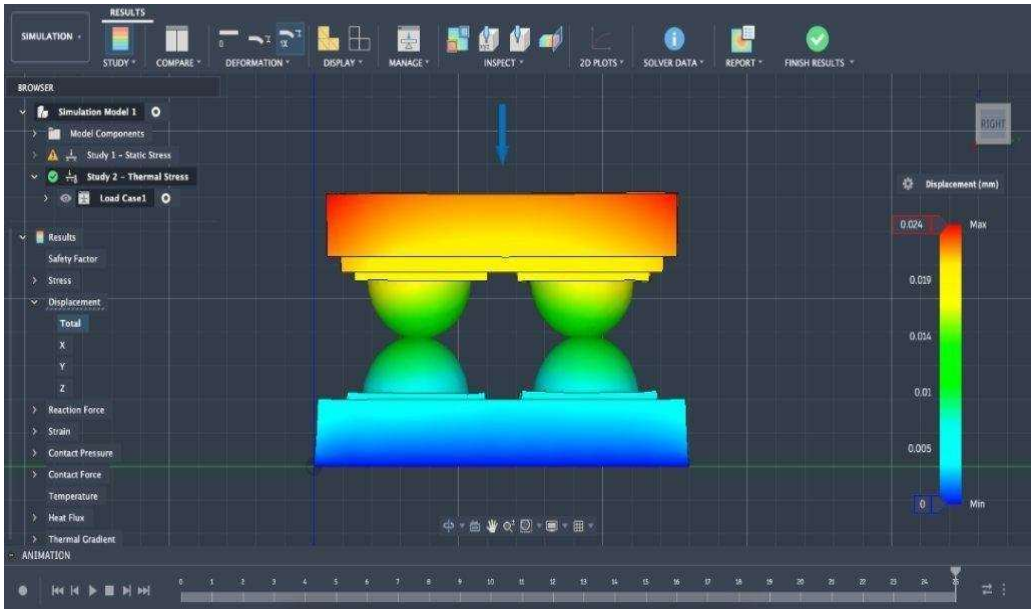


Fig. 8: Total displacement distribution showing maximum of 0.024 mm at upper detector chip surface

2.4 Principal Strain Field Distribution

First principal strain analysis characterizes maximum tensile or compressive strain developed within the assembly. Simulation results indicate maximum principal strain approximately +0.005 and minimum (compressive) strain approximately -0.003, both concentrated in indium bump regions and at their interfaces with gold pads. Chip bodies exhibit low, uniform strain values consistent with high stiffness, confirming that applied bonding force does not introduce harmful mechanical loading in brittle semiconductor components.

Within bumps, strain distribution exhibits symmetric, smoothly varying character, with peak values at upper and lower contact surfaces where interface constraints and material mismatch produce local strain intensification.

Compressive strains in lower assembly regions reflect combined effects of applied downward force and fixed bottom boundary condition. Controlled strain localization within compliant indium interconnects, while surrounding materials remain within elastic limits, represents desired operational mode for reliable flip chip bonding.

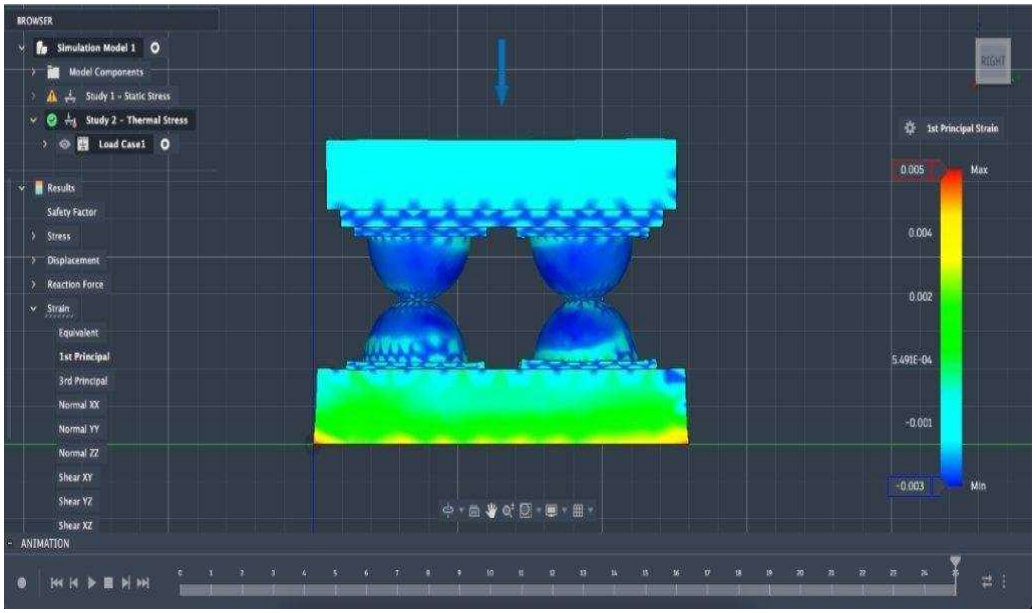


Fig. 9: First principal strain distribution showing maximum +0.005 and minimum -0.003 at bump-metallization interfaces

2.5 Interface Contact Pressure Distribution

Contact pressure distribution at bump-metallization interfaces serves as a direct indicator of bonding quality and electrical contact integrity. Maximum contact pressure approximately 808 MPa manifests at the centers of bump-pad contact areas on both detector and ROIC sides, indicating effective mechanical load transmission through interconnects. Moderate pressure levels (blue-to-green contours) prevail across the majority of contact surfaces, suggesting relatively uniform load distribution that minimizes localized over-compression risk while ensuring sufficient contact area for metallurgical bonding.

Low-pressure regions at bump edges reflect natural stress relaxation at geometric boundaries and do not constitute bonding defects. The absence of zero-pressure (non-contact) zones confirms that complete contact establishment occurs throughout bonding simulation. Symmetric contact pressure profile across both bumps further validates geometric alignment and load symmetry of modeled assembly.

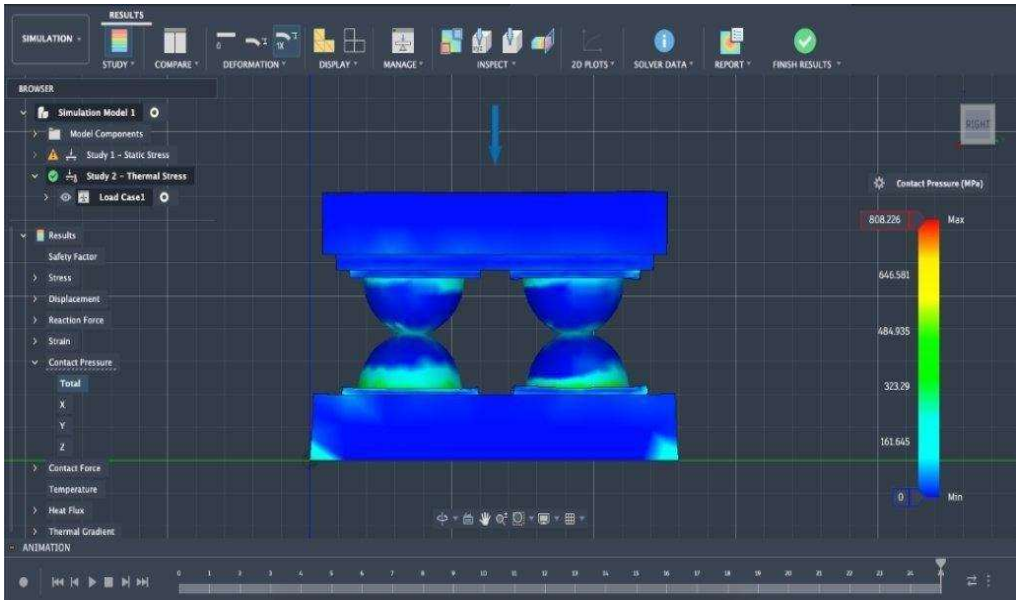


Fig. 10: Contact pressure distribution showing peak of 808.226 MPa at bump-metallization contact centers

Table 2. Summary of Key Simulation Results

Simulation Parameter	Maximum Value	Minimum Value	Critical Location
Safety Factor	> 8.0 (chip bodies)	0.236	Bump-pad interface
Von Mises Stress (MPa)	876.9	0.24	Indium bump interfaces
Total Displacement (mm)	0.024	~0.0	Top surface / ROIC base
1st Principal Strain	+0.005	-0.003	Bump contact surfaces
Contact Pressure (MPa)	808	~0	Bump-pad center / edges
Heat Flux (W/mm²)	3.31×10^{-5}	1.49×10^{-8}	Bump-pad interfaces
Thermal Gradient (K/mm)	2.94×10^{-4}	5.70×10^{-8}	Bump-pad interfaces

2.6 Heat Transfer Pathways under Cryogenic Loading

Under cryogenic thermal loading at 77 K, heat flux distribution reveals the dominant role of indium bumps as thermal conduits within the assembly. Maximum heat flux approximately 3.31 $\times 10^{-5}$ W/mm² concentrates at bump-metallization interfaces, where material continuity and elevated contact pressure facilitate efficient thermal conduction. Chip bodies exhibit low and spatially uniform heat flux levels, indicating that thermal resistance is governed primarily by interconnect regions rather than bulk semiconductor substrates.

Symmetric heat flux distribution across the two bumps confirms uniform thermal coupling and consistent bonding quality in the modeled assembly. Localized heat flux increases near interfaces correlate with regions of elevated contact pressure identified in mechanical analysis, reinforcing the coupled nature of mechanical contact quality and thermal transport efficiency. The absence of abrupt heat flux discontinuities or isolated hotspots indicates stable, continuous thermal conduction paths through the assembly—an important characteristic for cryogenic applications where large thermal gradients can induce significant additional thermo-mechanical stress.

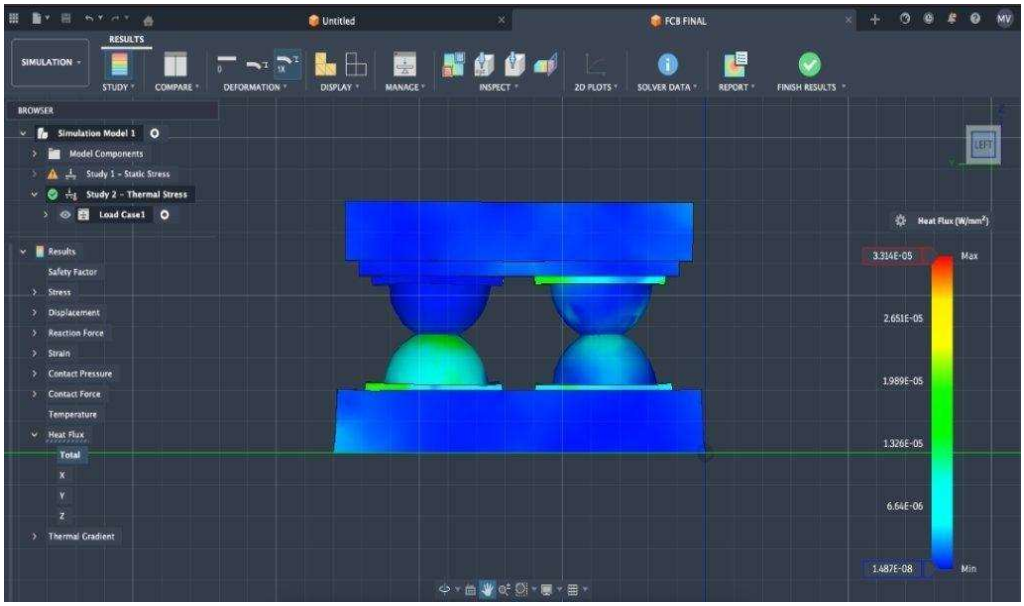


Fig. 11: Heat flux distribution under 77 K cryogenic loading showing maximum 3.314 × 10^{-5} W/mm² at bump-metallization interfaces

2.7 Temperature Gradient Field Distribution

Thermal gradient analysis characterizes spatial temperature change rate, which constitutes a primary driver of thermo-mechanical stress in multi-material assemblies with mismatched

thermal expansion coefficients. Maximum thermal gradient approximately 2.94×10^{-4} K/mm localizes within indium bumps and at bump-metallization interfaces, coinciding with regions of abrupt material property transitions and elevated contact pressure identified in mechanical simulations.

Chip bodies exhibit low, smoothly varying thermal gradients, indicating near-uniform temperature distribution across semiconductor substrates that minimizes internally generated thermally induced stress risk. Thermal gradient concentration within compliant indium interconnects—rather than in brittle semiconductor chips—highlights the dual mechanical and thermal protective function served by solder bump geometry. The correlation between high thermal gradient regions and high contact pressure/mechanical stress regions demonstrates strong coupling between bonding mechanics and thermal performance: improving bonding contact quality simultaneously enhances both electrical conductance and heat transfer efficiency.

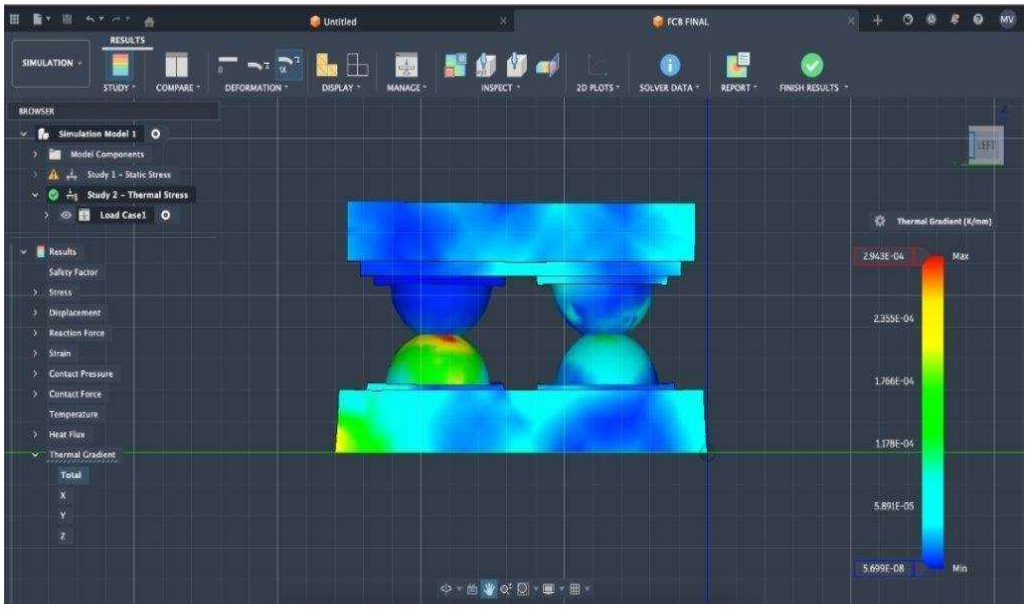


Fig. 12: Thermal gradient distribution showing maximum 2.943×10^{-4} K/mm concentrated at indium bump-metallization interfaces

2.8 Integrated Discussion of Coupled Phenomena

Integrated analysis of static mechanical and cryogenic thermal behavior reveals several design-relevant insights. First, indium bumps serve dual functionality as both primary mechanical stress-accommodation elements and dominant thermal conduction pathways within flip chip assemblies. Their compliance protects brittle semiconductor chips from excessive stress, while their high thermal conductivity ensures efficient heat extraction from detector chip to ROIC.

Second, bump-metallization interface regions consistently emerge as the most mechanically and thermally demanding locations in the assembly. Safety margin minima, Von Mises stress maxima, peak contact pressures, maximum heat fluxes, and maximum thermal gradients are all co-located at these interfaces. This convergence implies that bonding quality at bump-pad contact constitutes the single most influential factor governing both mechanical reliability and thermal performance of the assembly.

Third, displacement and strain results confirm that controlled, symmetric bump compression—without abrupt gradients or localized collapse—is achievable under simulated bonding conditions. This suggests that selected bonding force and bump geometry are compatible with thermo-compression bonding requirements, though experimental validation under varied bonding parameters would be needed to define precise process windows.

3. Conclusions

This study presented detailed finite element computational analysis of a three-dimensional flip chip bonded assembly comprising silicon ROIC, GaSb detector chip, gold contact pads, and indium solder bumps, simulated within Autodesk Fusion 360. The following principal conclusions are drawn:

(1) Mechanical load distribution: Applied bonding load is absorbed predominantly by indium bumps, which undergo controlled plastic deformation while semiconductor chip bodies remain within safe elastic limits. This validates the effectiveness of compliant indium interconnects in protecting brittle device layers.

(2) Critical interface zones: Bump-metallization interfaces are consistently identified as mechanically and thermally most demanding regions across all simulation metrics—safety margin, Von Mises stress, principal strain, contact pressure, heat flux, and thermal gradient—underscoring their central role in governing assembly reliability.

(3) Uniform deformation: Symmetric and smoothly varying displacement field within bump array confirms uniform load distribution and minimal chip tilt risk under applied bonding conditions, consistent with reliable thermo-compression bonding.

(4) Thermal performance: Under cryogenic loading at 77 K, indium bumps act as primary heat-transfer pathways between detector and ROIC chips. The absence of significant thermal bottlenecks or isolated high-gradient zones indicates stable and efficient thermal conduction through the assembly.

(5) Thermo-mechanical coupling: Strong spatial correlation exists between regions of high contact pressure, elevated mechanical stress, and concentrated thermal gradients. This coupling implies that enhancing bonding contact quality—through appropriate pressure and temperature—simultaneously improves both structural reliability and thermal efficiency.

These findings provide quantitative basis for understanding the influence of key process parameters in indium-based flip chip bonding, particularly for cryogenic and infrared detector applications. The methodology and results contribute to the growing body of simulation-driven process optimization knowledge applicable to advanced microelectronic packaging.

3.1 Future Work

The present computational framework establishes foundation for several natural extensions. Planned future investigations include: (i) parametric optimization studies systematically varying bonding temperature, applied force, bump height, and bump diameter; (ii) incorporation of underfill materials and their effect on residual stress distribution; (iii) transient thermal cycling simulations to assess cumulative fatigue damage in interconnects; (iv) expansion to larger multi-bump arrays to capture array-level uniformity effects; and (v) experimental validation of key simulation predictions through fabrication and mechanical characterization of indium bump assemblies.

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Conflict of Interest

The authors declare no conflict of interest.

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