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Supplementary Information

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Cooperative Reconstructive Epitaxy of MoS_2 Monolayers in a Multi-Wafer MOCVD Process Guided by In-Situ Process Monitoring

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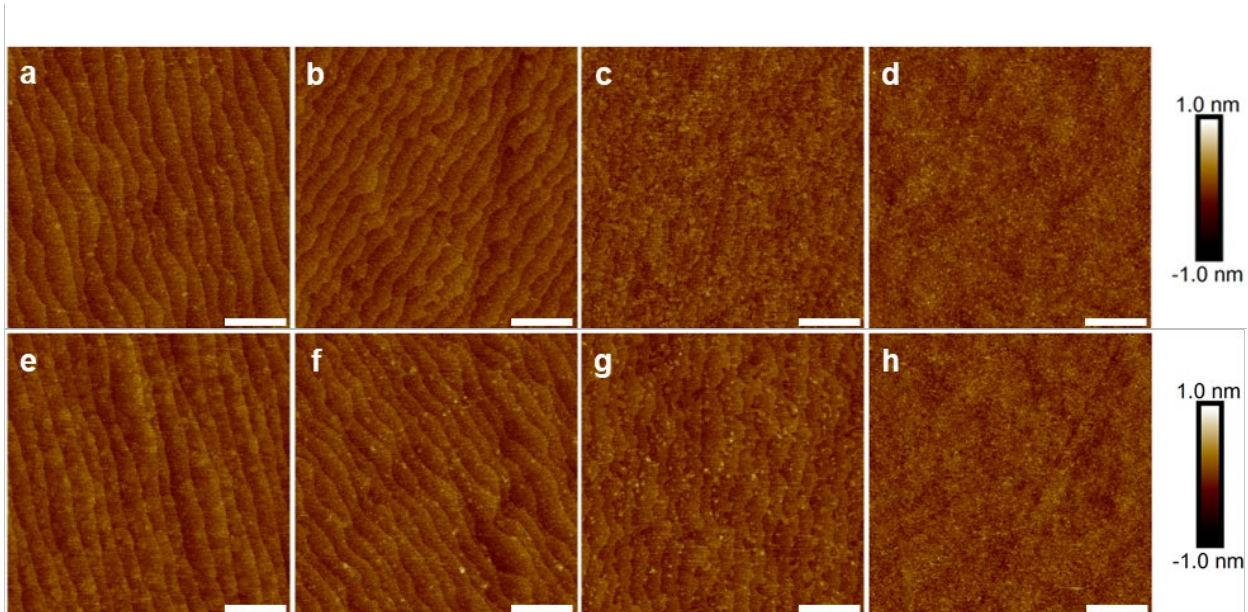
41 Supplementary Figure 1

42 

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44 **a** – **d**, 1×1 μm^2 AFM micrographs of sapphire surfaces annealed under H_2 only at 1000, 900,
45 800, and 700 °C, respectively. **e** – **h**, Sapphire surfaces annealed under H_2S at the same
46 temperatures. All scale bars are 200 nm.
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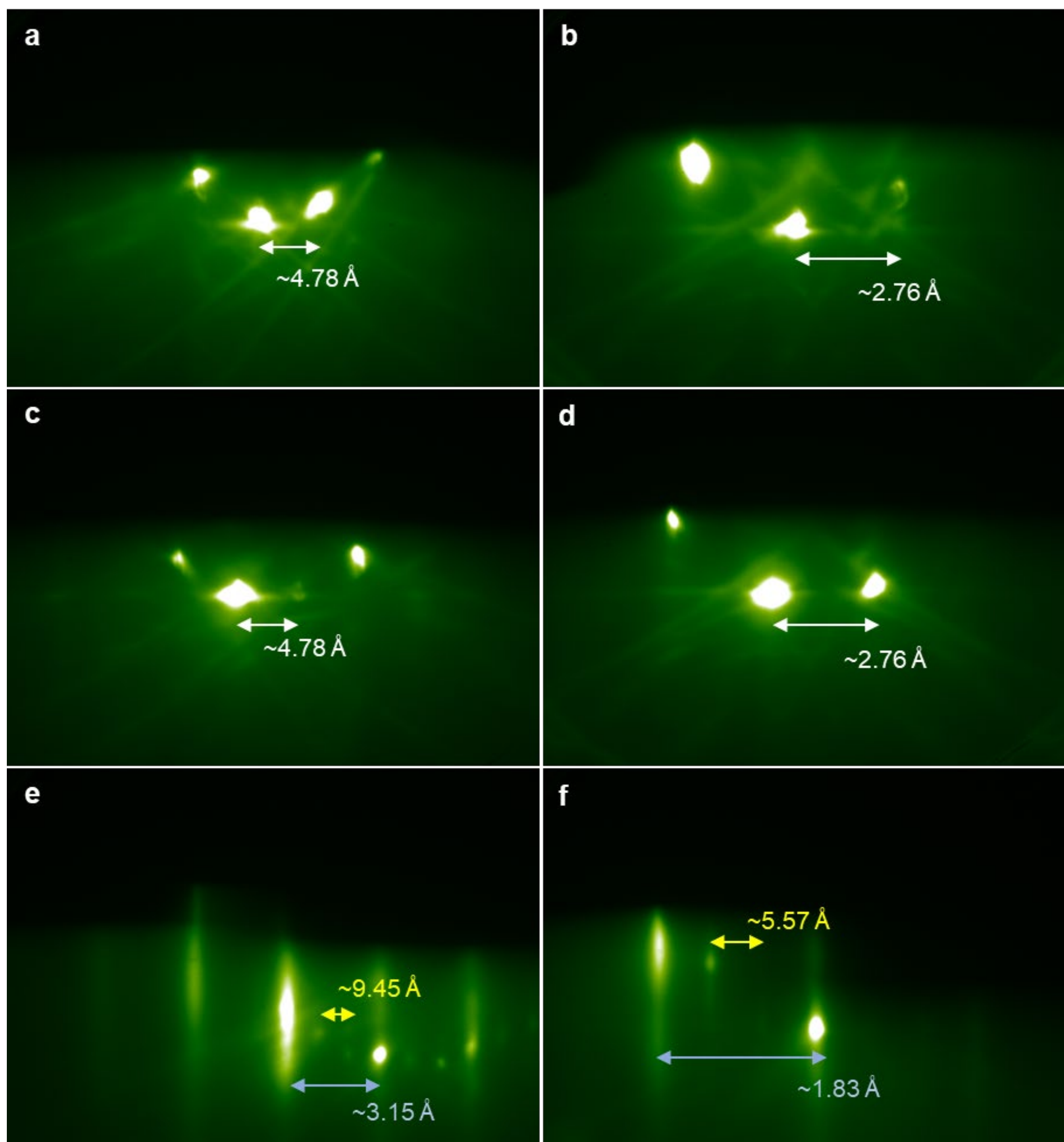
63 Supplementary Figure 2



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65 RHEED patterns from a c-plane sapphire substrate after annealing in H_2 for 30 minutes,
66 measured along **a**, the [112-0] direction and **b**, the [101-0] direction. RHEED patterns from a c-
67 plane sapphire substrate after annealing in H_2 for 15 minutes followed by 15 minutes in
68 H_2/H_2S, measured along **c**, the [112-0] direction and **d**, the [101-0] direction. RHEED patterns
69 from a MoS_2 monolayer grown on c-plane sapphire, measured along **e**, the [112-0] direction
70 and **f**, the [101-0] direction. White and blue arrows indicate spacing of diffraction features
71 related to sapphire and monolayer MoS_2 respectively, converted to real space distances.
72 Yellow arrows indicate spacing of features related to the MoS_2/sapphire superlattice.

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78 Supplementary Figure 3
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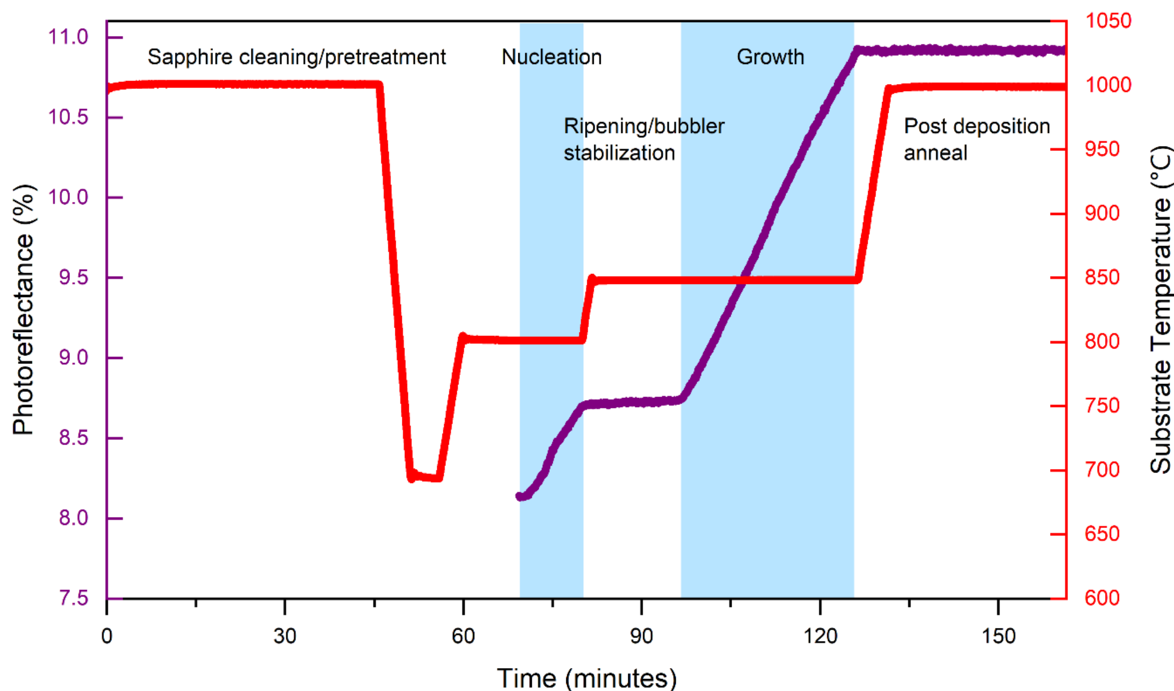

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82 In-situ photoreflectance (violet line) and substrate temperature (red line) from sapphire
83 pretreatment and nucleation through TMD growth to reflectance endpoint and post-deposition
84 anneal. Light blue stages, annotated “Nucleation” and “Growth”, indicate when the MCO
85 bubbler is open to the reactor. H_2S opens 15 minutes into pretreatment and is then constant
86 throughout the rest of the process. The EpiTT photoreflectance measurement is calibrated to
87 the substrate after completion of the pretreatment just before nucleation; photoreflectance
88 readings prior to this have no meaning and are omitted.
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108 Supplementary Figure 4
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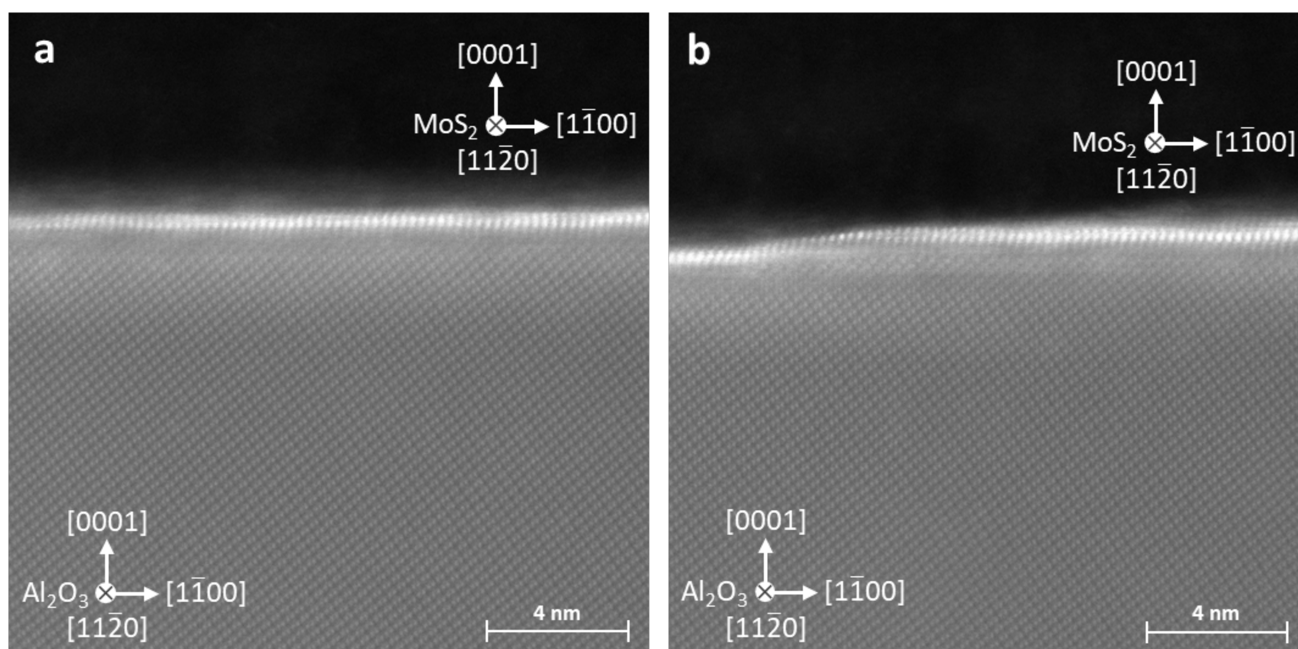

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111 **a**, Raw cross-sectional HAADF-STEM images of MoS_2 monolayer deposited on the sapphire
112 substrate and **b**, over the sapphire terrace step, both observed along $[11\bar{2}0]$.

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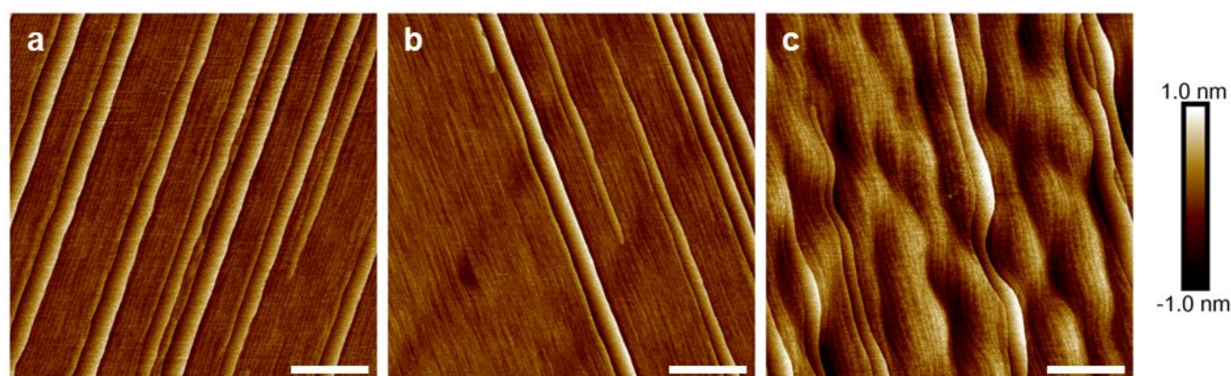
138 Supplementary Figure 5



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140 **a**, 5 x 5 μm^2 AFM micrograph of sapphire surface after extended hydride anneal of 45 minutes
141 at 1000 ºC (rather than the standard 15 minutes). **b**, Sapphire surface after standard 15 minute
142 anneal but at increased temperature of 1100 °C. In both a and b, the bunched steps are larger
143 than double steps. **c**, Sapphire surface after standard 15 minute anneal but at increased
144 temperature of 1200 °C. All scale bars 1 μm.

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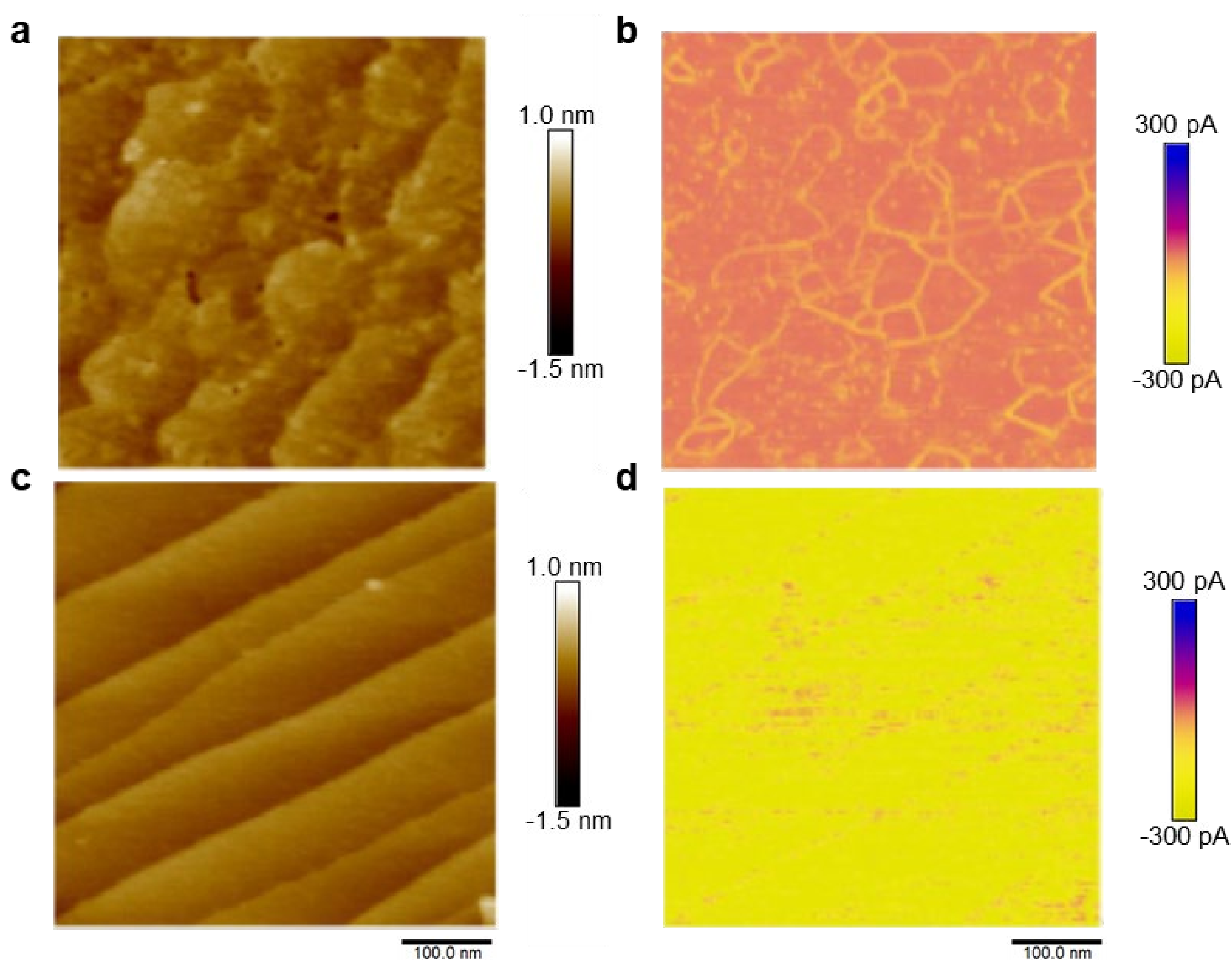
175 Supplementary Figure 6



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178 **a**, 500 x 500 nm^2 AFM topography of MoS_2 layer that did not undergo PDA. **b**, Co-localized C-
179 AFM micrograph of current measurement for region in panel a taken with a -1V sample bias. **c**,
180 500 x 500 nm^2 AFM topography of MoS_2 layer that underwent PDA after growth. **d**, Co-
181 localized C-AFM micrograph of current measurement for region in panel c taken with a -1V
182 sample bias. For the MoS_2 sample that had the PDA treatment the limiting current is around -
183 230 pA, an order of magnitude higher than the MoS_2 layer without PDA treatment.
184 Supplementary Figure 7
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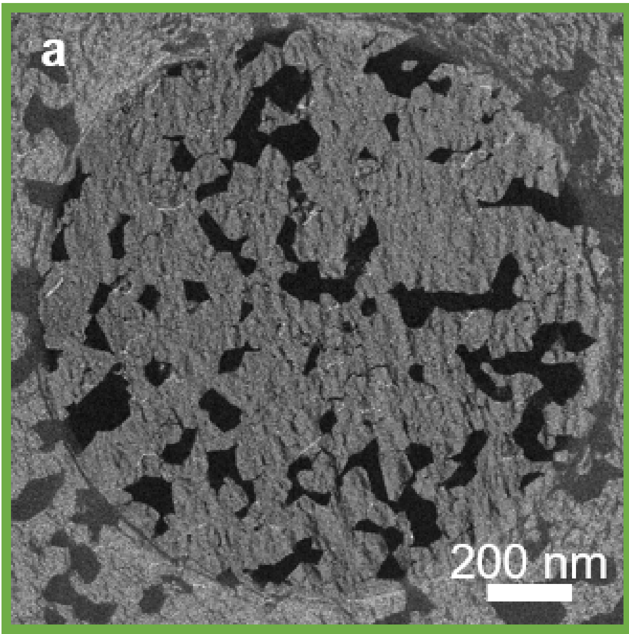

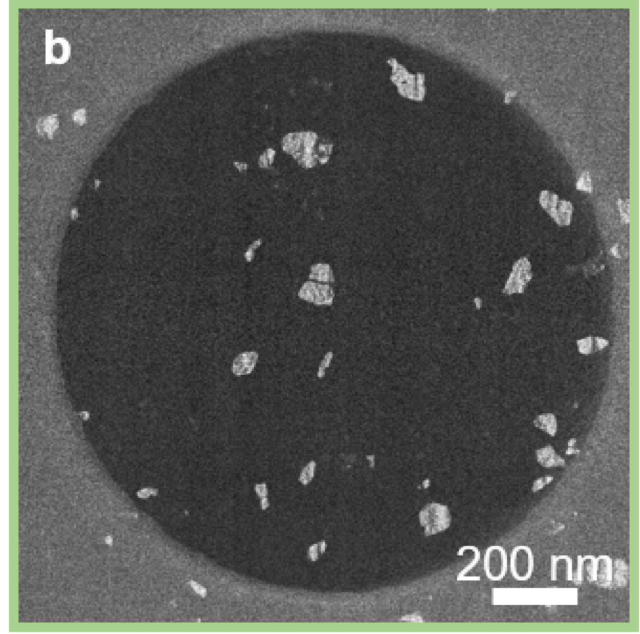

187 Additional dark field TEM of the MoS_2 monolayer grown without a PDA treatment on **e**,
188 oriented and **f**, misoriented $11\bar{2}0$ spots.

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228 Supplementary Figure 8
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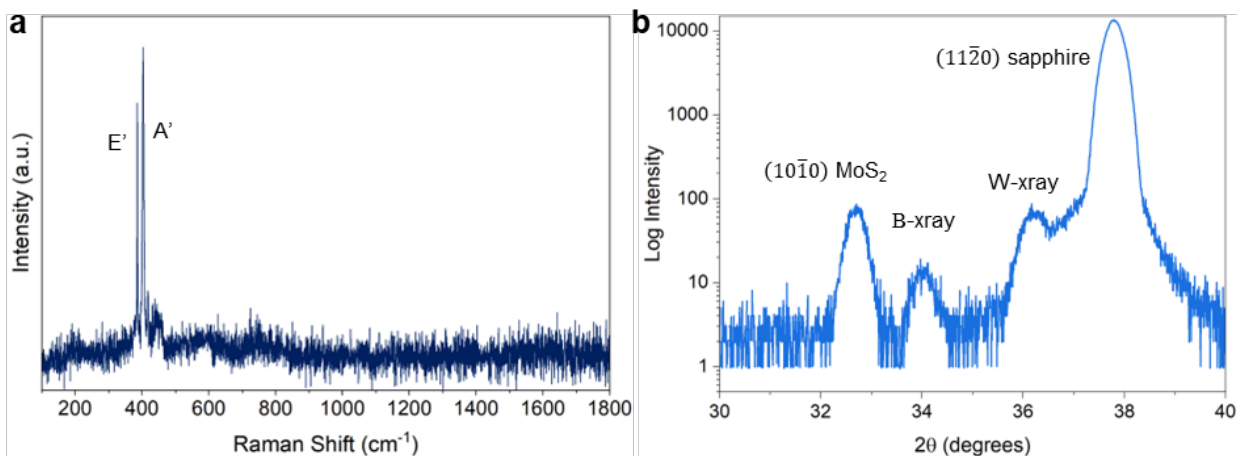

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231 **a**, Raman spectroscopy of a MoS_2 monolayer from 200–1800 cm^{-1} shows only the E' and A'
232 peaks associated with MoS_2, and no indication of carbon related peaks. **b**, In-plane XRD
233 shows the expected (1 0 -1 0) peak for MoS_2 and (1 1 -2 0) peak for the c-plane sapphire
234 substrate.

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263 Supplementary Figure 9
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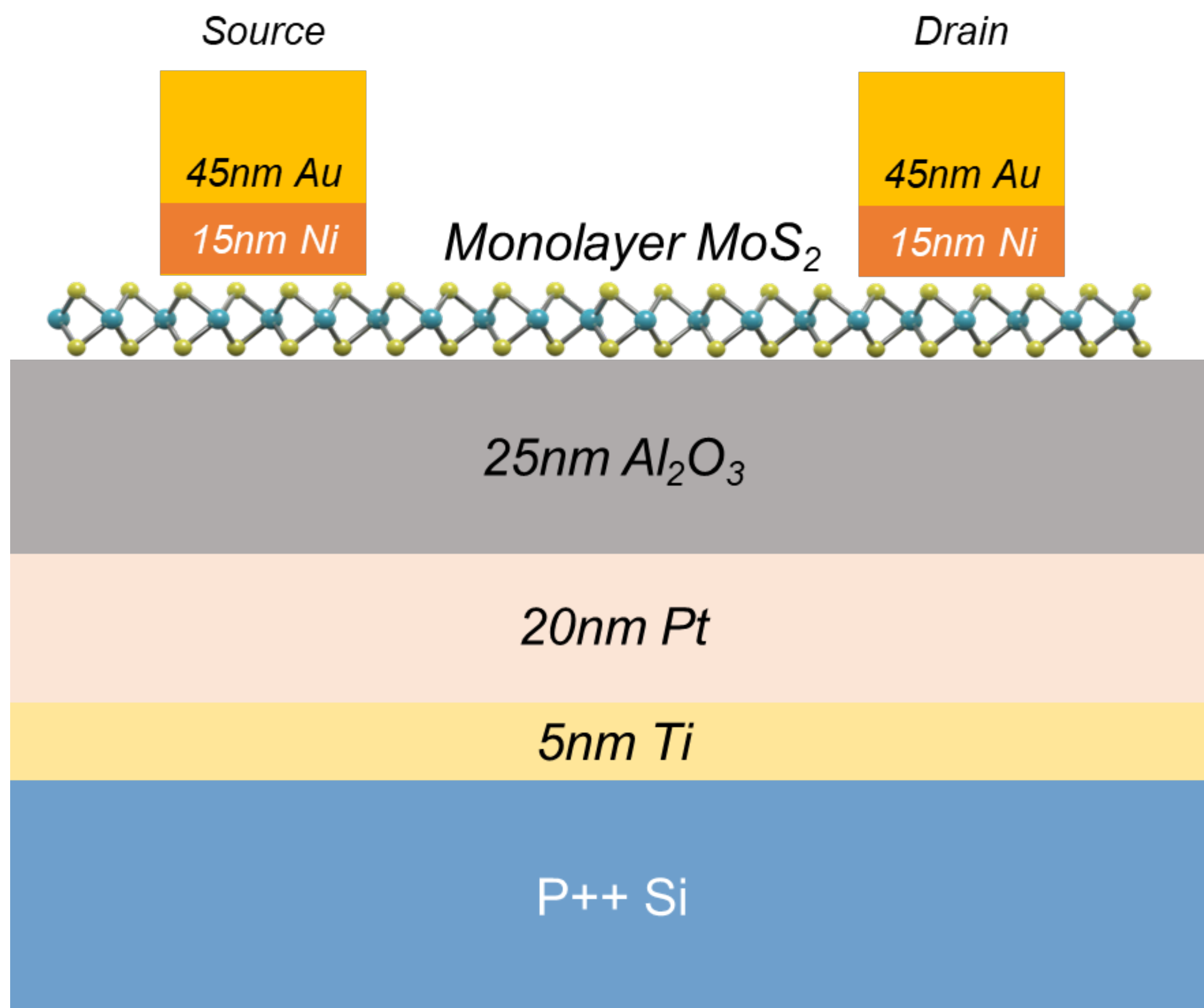

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267 Cross sectional device schematic for back-gated MoS_2 FETs.

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282 Supplementary Table 1
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Ref.	Med. mobility	Max mobility	Med. I_{on}/I_{off}	Max I_{on}/I_{off}	Multi-wafer	substrate	Ex-situ annealing	Growth Chemistries	Contact materials	Gate materials
56	17.5	66	-	$1x10^7$	No	c-plane 0.2° ± 0.1° c/m (on-axis)	Yes, 1 hour 1150 °C in air	MoO_2CL_2 / H_2S	1 nm Ni/30 nm Au source and drain, n^+ Si back gate	90 nm SiO_2
35	18	40	$1.6x10^9$	$2x10^{10}$	Yes	c-plane 0° (on-axis) , 1° c/m	Yes, 1 hour 1175 °C in air	$Mo(CO)_6$ / H_2S	10 nm Ni/20 nm Pd source and drain, p^+ Si back gate	50 nm SiO_2
25	20.5	-	$1x10^7$	-	No	c-plane	No	$Mo(CO)_6$ / H_2S	40 nm Ni/ 30 nm Au source and drain, Pt/Ti/p^{++} Si back gate	50 nm Al_2O_3
78	27	30	-	$2.1x10^7$	No	c-plane	No	$Mo(CO)_6$ / H_2S	40 nm Ni/ 30 nm Au source and drain, Pt/Ti/p^{++} Si back gate	50 nm Al_2O_3
19	-	22	-	-	No	Non-specified sapphire	Yes, 1100 °C in air	Na_2MoO_4 / $((C_2H_5)_2S)$	2 nm Ti/90 nm Au source and drain, n^{++} Si back gate	270 nm SiO_2
43	25	28	-	$1x10^8$	Yes	c-plane 1° c/a	Yes, 1 hour in H_2	$Mo(CO)_6$ / H_2S	10 nm Ni/20 nm Pd source and drain, p^+ Si back gate	50 nm SiO_2

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286 Data from literature used in benchmarking plots in figure 7 of the main text.
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310 Supplementary Figure 10
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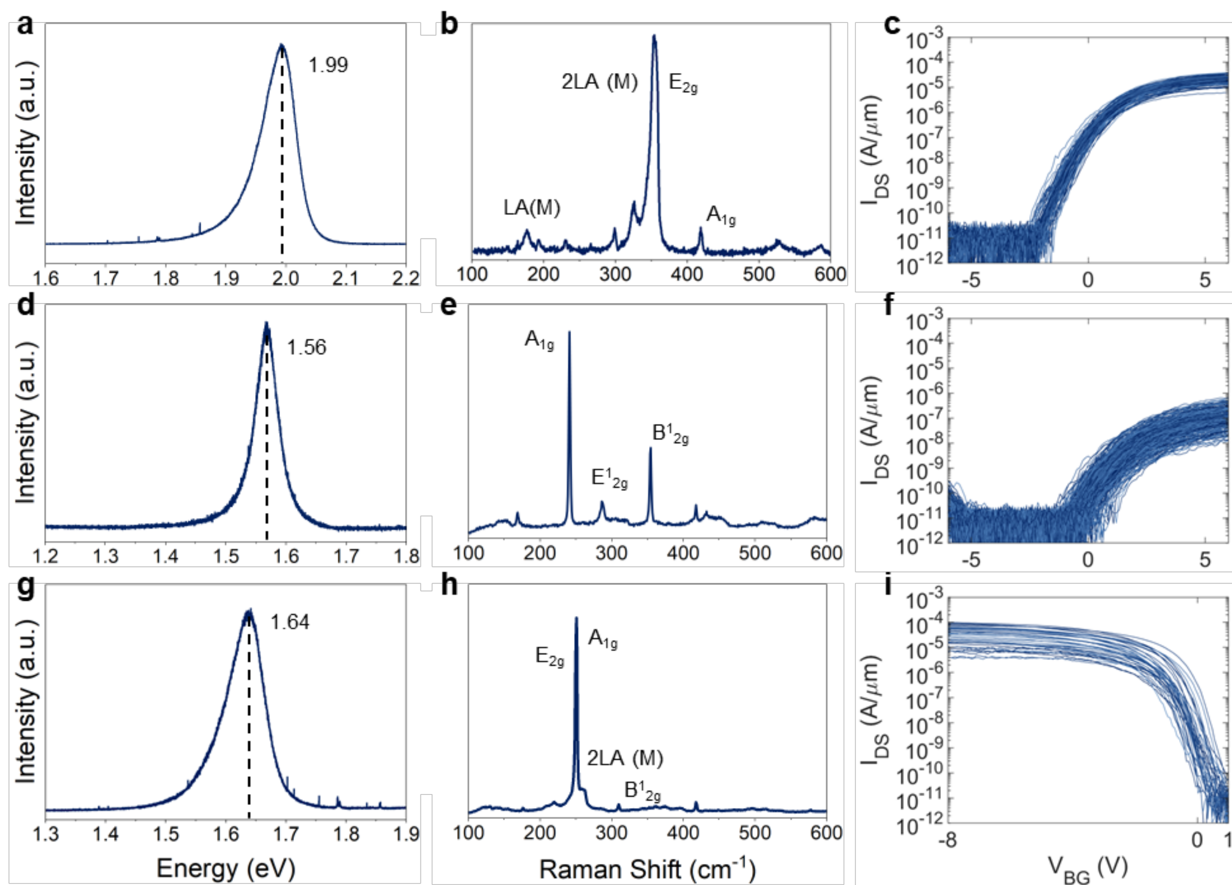

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314 **a**, WS_2 PL spectra. **b**, WS_2 Raman spectra. **c**, WS_2 based transistor transfer curves. **d**, $MoSe_2$
315 PL spectra. **e**, $MoSe_2$ Raman spectra. **f**, $MoSe_2$ based transistor transfer curves. **g**, WSe_2 PL
316 spectra. **h**, WSe_2 Raman spectra. **i**, WSe_2 based transistor transfer curves.