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A 0.00024 m m2, 18.9fJconv-step ClC-reused charge-injection SAR ADC with segmented sampling capacitors for computing-in-memory

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ABSTRACT

This paper presents an area-efficient two-stage charge-injection SAR (CI-SAR) ADC for computing-in-memory (CIM) applications. By using a novel capacitive voltage-division sampling technique and proposed capacitive-divider-based charge-injection cell (CIC) reuse structure, the layout area occupied by the charge injection array is greatly reduced by 93.4%. Through proposed cooperative of coarse quantization stage and fine quantization stage, the sampled CIM signals can be accurately quantized into a 7-bit digital output with high power efficiency. Furthermore, a segmented common-mode shifting (S-CMS) technique maintains a stable common-mode voltage, preserving linearity throughout the entire conversion process. Verified in a standard 28 nm CMOS process, propose ADC occupies a chip area of only 0.00024 mm^2. Operating at 1GS/s with a 1 V supply, it achieves 40.79 dB SNDR and 48.78 dB SFDR with a Walden figure of merit (FoM) of 18.9fJ/conv-step, demonstrating competitive area and power efficiency for medium-resolution CI-SAR ADCs.

1. Introduction

The fast growth of heavy-data applications, such as artificial intelligence, deep-learning, and wired communications, is putting more and more stringent requirements on the energy efficiency and throughput of hardware. The traditional von Neumann architecture suffers from significant power consumption due to data movement because of the "memory wall" problem, which constitutes the primary bottleneck for further improvement of system performance. in this context, CIM architecture is considered a promising solution. By embedding computing units into memory arrays and performing multiply-accumulate (MAC) operations directly in the analog domain, CIM reduces data movement and achieves high computational density and energy efficiency [1].

In a typical CIM macro chip, N channels of parallel analog multiply-accumulate outputs correspond to an N-channel column-parallel ADC array for interface quantization. For a moderate-scale array (e.g. 256 × 256 or 512 × 512), this implies the integration of hundreds of these ADCs must operate within stringent area constraints which are typically limited to micrometer-scale column pitch. In order to meet requirements for high efficiency and precision, SAR ADCs are widely adopted as the preferred architecture [2].

Conventional SAR ADCs require large capacitor arrays to achieve high precision, which limits the area efficiency of this architecture and increases the input loading. Charge-injection DAC-based SAR ADCs have been introduced to address these limitations by replacing the capacitor array with reusable charge-injection cells. However, this architecture exhibits inherent sensitivity of linearity to common-mode voltage variations, and its performance is susceptible to process, voltage, and temperature (PVT) variations [3]. To improve linearity while maintaining a small area, a capacitor-array-assisted cascaded charge-injection SAR structure is proposed in [4], achieving high accuracy through a hybrid DAC and noise optimization techniques. In recent years, various hybrid CI-SAR structures have been further investigated. For instance, a hybrid structure employing a C-CI DAC achieved 8-bit resolution with ultra-low power and minimal area [5], while a third-order capacitor-array-assisted CI-DAC structure realized a compact ADC area through systematic modeling for information rate density optimization [6]. An asynchronous CI-SAR proposed in [7] utilizes replica feedback loops and common-mode shifting techniques, enhancing tolerance to PVT variations and achieving high bandwidth. Concurrently, in-depth analysis of noise and nonlinearity in CI-SARs provides a theoretical foundation for high-precision design [8]. A CI-SAR structure with built-in offset calibration has been successfully deployed in computing-in-memory macros, it reuses the CI-DAC array itself to perform coarse and fine offset detection, significantly improving inference accuracy in multi-ADC array systems [9].

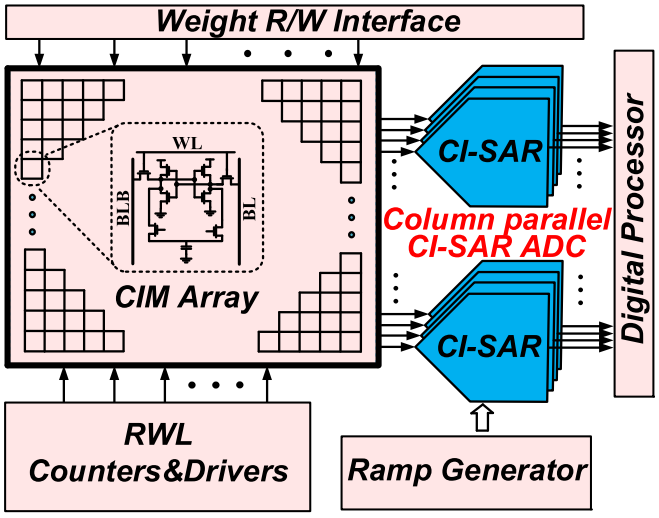


Fig. 1. System architecture of the CIM macro with the integrated proposed ADC.

Recent research efforts focus on the simultaneous optimization of area, energy efficiency, and speed through novel circuit techniques. A cascoded FVF-based CI-SAR reported in [10] achieves high energy efficiency within a minimal area by employing simplified control logic and compact CI cells. A CI-CDAC hybrid SAR ADC introduced in [11] achieves high energy efficiency but results in a relatively large area. A cryogenic CMOS CI-SAR for quantum readout, reported in [12], employs bidirectional charge flow and bottom-plate sampling techniques to achieve high linearity with very low input capacitance. A segmented CI-DAC structure with temperature-aware bias generation technology is introduced in [13], enabling the SAR ADC to achieve high sampling speed while maintaining a small area. For high-speed medium-accuracy applications, [14] employs charge-pump and charge-balancing switching techniques to effectively mitigate linearity degradation caused by common-mode voltage drop during conversion, thereby enhancing dynamic range and linearity to achieve 9-bit resolution. However, the linear increase in the number of physical CICs limits the area advantage. While prior research has made progress in achieving medium-to-high resolution, area reduction techniques still face challenges. This paper presents a hybrid two-stage CI-SAR ADC architecture based on capacitive voltage-division sampling and CIC-reuse. The architecture effectively reduces ADC area through a capacitive voltage-division sampling array and a segmented common-mode shifting technique.

This paper is organized as follows: Section II elaborates on the overall architecture of the proposed ADC and the principle of capacitive voltage division. The implementation details of the circuit modules are provided in Section III. Comprehensive performance evaluation results based on post-layout simulations are presented in Section IV. The paper is concluded with a summary in Section V.

2. Overall architecture and the principle of capacitive voltage division

2.1. Proposed capacitive-divider-based CIC-reuse architecture

The CI-SAR employs an array of charge-injection cells to replace the conventional capacitor array for its digital-to-analog converter function. Each CIC typically consists of several transistors and can be activated by a short pulse to inject a precise amount of charge into the sampling capacitor. The proposed architecture provides an advantage by facilitating the reuse of CICs. For instance, a 6-bit conversion requires 63-unit capacitors in a binary-weighted CDAC, whereas the CI-SAR architecture can accomplish this with far fewer physical CIC units. This results in a significant reduction in area, making the CI-SAR attractive for area-constrained applications. Furthermore, the input capacitance of the CI-SAR is primarily determined by the sampling capacitor, which can be designed to be very small (e.g., ~10fF), thereby significantly relaxing the driving requirements for the preceding stage. Nonetheless, the CI-SAR architecture faces many difficulties. The first reason for the susceptibility of gain error of CICs is that PVT variations most affect the charge injection current of CICs. And this leads to performance degradation in a different process and gain error. Second, the monotonic switching scheme employed in most CI-SARs causes a continuous drop in the comparator's input common-mode voltage, making it susceptible to dynamic offset and speed variations, thereby compromising linearity. Third, the number of physical CICs remains one of the primary factors determining the total ADC area.

Basic principle of the charge-injection SAR ADC is illustrated in Fig. 1. The input signal is first sampled onto the integration capacitor C_{int}. During the conversion phase, a DAC array composed of multiple charge-injection cells is sequentially activated. When each CIC is activated, it draws a precise charge packet $Q_{unit} = I_{unit} \bullet T_{pluse}$ from C_{int} with a current I_{unit} set by a bias voltage over a fixed pulse width. By controlling the number of activated CICs in a binary-weighted manner, corresponding residue voltages are established on C_{int} and decided bit-by-bit by the comparator.

In conventional charge-injection SAR ADCs, achieving N-bit resolution typically requires 2^N-1 equivalent unit charge injection cells in the DAC, as shown in Fig. 1. Although reuse strategies can reduce the number of physical CICs, this number remains proportional to the resolution N, leading to increased circuit area, routing complexity, and matching difficulty with higher precision, which constitutes a major

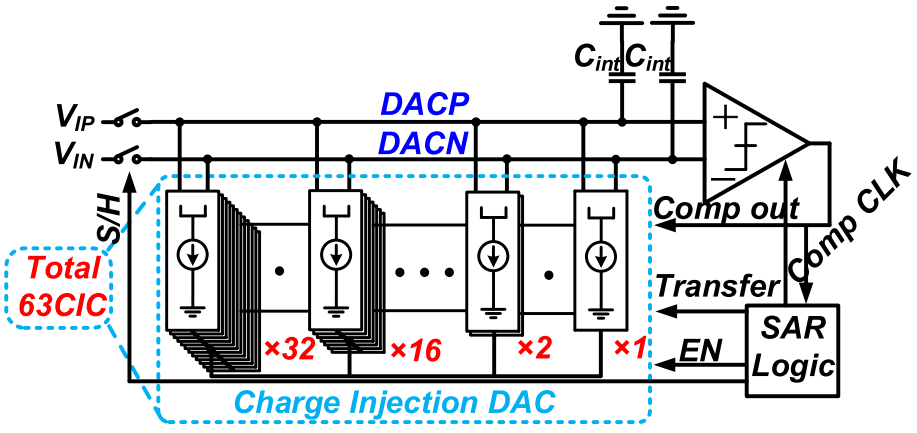


Fig. 2. Conventional CI-SAR ADC architecture.

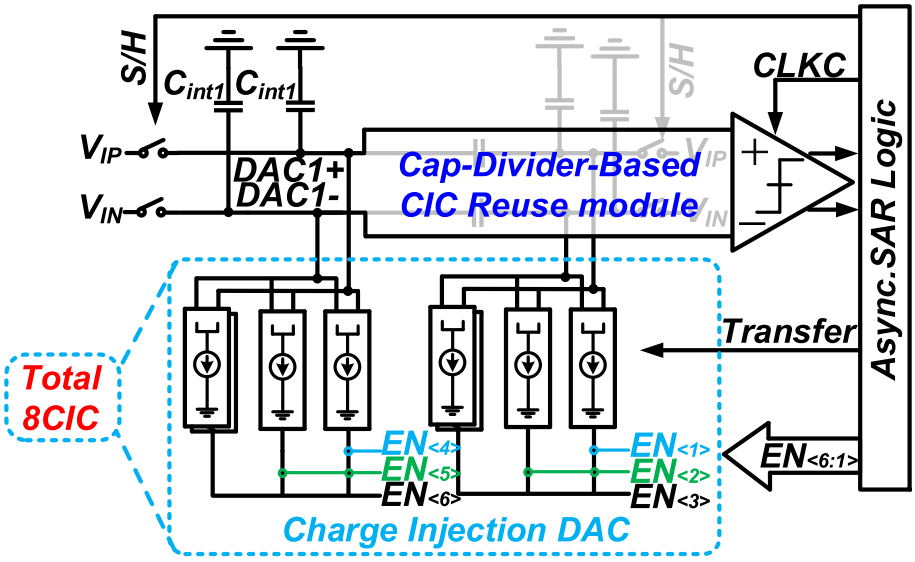


Fig. 3. Proposed CI-SAR structure.

limitation in area-sensitive applications.

For instance, an N-bit conversion requires 2^N-1 equivalent unit charge injection operations, but by using digital logic to control the same set of physical CICs across different cycles, the number of required physical units can be substantially reduced. This significantly shrinks the circuit area of the CI-SAR, while the reduced input capacitance also relaxes the driving requirements for the preceding stage, making it particularly suitable for multi-channel application scenarios such as computing-in-memory and high-speed time-interleaved ADCs.

This paper proposes a hybrid two-stage CI-SAR ADC architecture that incorporates capacitive voltage-division module to overcome these challenges. The overall block diagram is shown in Fig. 2. By introducing a parallel fine-quantization path with voltage attenuation capability, the architecture achieves a substantial reduction in the number of physical CICs.

The architecture comprises two quantization stages:

1. The DAC1-stage (Coarse Quantization, upper 3-bits): consists of a standard CI-SAR structure with 4 CICs, which performs the most significant bit conversions.
2. The DAC2-stage (Fine Quantization, Lower 3-bits +1 Redundant Bit): Incorporates the crucial capacitive voltage-division module (division ratio $\alpha = 1/8$) and is also configured with 4 CIC units.

Owing to the voltage attenuation effect, the charge injected by a single CIC in this DAC2-stage produces a voltage step of αLSB on the main integration capacitor.

The proposed architecture achieves a substantial reduction in the required number of CICs by leveraging the attenuation effect of the capacitive voltage divider. As visually compared in Fig. 1 and Fig. 2, for a 7-bit SAR ADC conversion: the conventional binary CI-SAR requires 63 equivalent CIC units. The attenuation resulting from the capacitive voltage division, the proposed architecture enables a single physical CIC in DAC2-stage to be equivalent to 8 logical LSB units, consequently requiring only 8 physical CICs (4 in DAC1-stage and 4 in DAC2-stage) to complete the conversion process.

2.2. Principle of capacitive-voltage divider module and CIC quantity reduction

To decouple the strong correlation between the number of physical CICs and the resolution in conventional CI-SAR architectures, an additional series capacitor C_{div} is introduced between the sampling capacitor and the charge injection unit. This module work as a precise voltage attenuator, enabling a single physical CIC to generate a voltage step at the sub-LSB level.

Fig. 3 illustrates the basic structure of the capacitive voltage-division module, which consists of the division capacitor C_{div} and the integration capacitor C_{int} connected in series. Here, V_{DAC2} serves as the charge injection node for the second stage, connected to its corresponding CIC array; V_{DAC1} acts as the output node, connected to the main integration capacitor C_{int} and the comparator's input. Its operating principle is as follows: when a CIC injects charge Q_{CIC} into DAC2-stage, a voltage step $\Delta V_{CIC} = Q_{CIC} / C_{div}$ is first generated across the division capacitor C_{div} After being attenuated by the capacitive voltage-division array, the effective voltage step ΔV_{int} produced on the integration capacitor C_{int} is given by:

$$\Delta V_{int} = \alpha \cdot \Delta V_{CIC} = \alpha \frac{Q_{CIC}}{C_{div}} \tag{1}$$

where the division ratio α is determined by the capacitor ratio:

$$\alpha = \frac{C_{div}}{(C_{div} + C_{int})} \tag{2}$$

Since $\alpha < 1$, ΔV_{int} can be made much smaller than the LSB voltage step produced by a single CIC in the conventional architecture. This implies that in this architecture, one physical CIC no longer corresponds to 1 LSB, but rather to αLSB.

The selection of the division ratio α involves a critical trade-off, as it simultaneously influences the total number of required physical CICs and the relative size of the division capacitor C_{div}. The relationship between C_{div} and the integration capacitor C_{int} can be derived from Eq. (2): $C_{div} = \alpha C_{int}/(1-\alpha)$ This relationship indicates that the value of C_{int} also constrains the size of C_{div}.

In conventional capacitor-DAC-based SAR ADCs, the input capacitance is primarily constrained by KT/C noise budget and capacitor matching requirements, typically resulting in large values (several hundred fF) to ensure sufficient linearity and signal-to-noise ratio [15–18]. However, when the total noise power contributed by KT/C noise approaches the quantization noise power, the following relation holds:

$$\overline{V_{n,q}} = \overline{V_{n,ktv}} \tag{3}$$

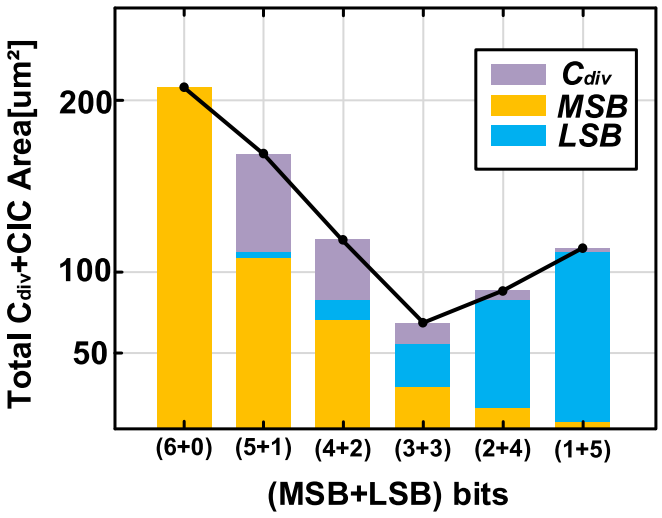


Fig. 5. Total area of DAC and bit allocation for 7b (+1 redundancy bit) DAC.

$$C_{in} = \frac{24KT}{\left(\frac{V_{in,diff}}{2^N}\right)^2} \tag{4}$$

where $V_{in,diff}$ is the differential full-scale input range and N is the ADC resolution. When the designed input capacitance approaches the KT/C noise limit, the sampling capacitor can theoretically be very small. Although using an excessively small sampling capacitor in a conventional CDAC leads to significant nonlinearity and DAC mismatch [19], the CI-SAR employs a non-traditional charge-injection DAC based on CICs, avoiding this drawback. This allows the sampling capacitor to be safely reduced to near the noise limit, thereby significantly enhancing the area efficiency of the CI-SAR ADC. Referring to the discussion on the relationship between input capacitance and SNDR in [6], a sampling capacitor of 16fF is selected for this design.

To determine the optimal division ratio α, it is mapped to the bit allocation problem between the most significant bit MSB path and the least significant bit LSB path. A systematic area optimization analysis is conducted for different allocation schemes, evaluating the impact of the total number of required physical CICs and the relative size of the division capacitor C_{div} on the total area. The analysis results are shown in Fig. 5.

Fig. 5 presents the analyzed results of the normalized total chip area under five different segmentation schemes. All area data are normalized relative to the area of the optimal scheme to clearly compare the relative performance of each scheme. Based on the 28 nm design process, the area of a single CIC unit is determined by its transistor dimensions and routing rules, assumed to be 4μm^2 The unit capacitor area is estimated based on the layout implementation of high-density metal-oxide-metal capacitors. The results indicate that the total chip area is highly sensitive to the bit allocation scheme. The allocation scheme of 3-bit MSB / 3-bit LSB (corresponding to $\alpha = 1/8$) achieves the minimum total chip area.

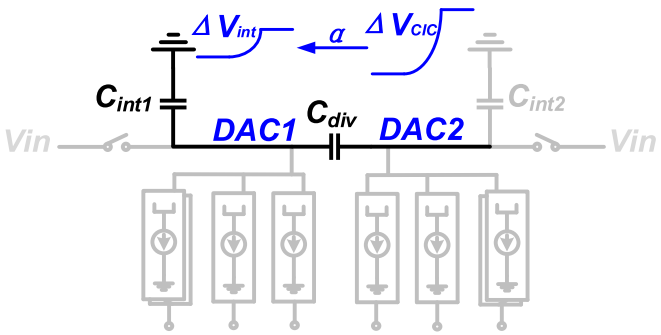


Fig. 4. Working principle of the capacitive voltage-division module.

This scheme strikes a good balance between the number of CIC units and the division capacitor area. Compared to the suboptimal scheme, this scheme saves 40% of the area; compared to the worst scheme, the area saving reaches approximately 65%.

This characteristic enables the potential for an exponential reduction in the number of CICs. For an N-bit resolution ADC, the total number of quantization levels is 2^N. The conventional binary architecture requires 2^N. equivalent unit CICs. In the proposed architecture, to achieve the same total number of levels, the required number of physical CIC activation events M satisfies the following relation:

$$M \cdot \alpha = 2^N - 1 \tag{5}$$

Therefore $M = (2^N - 1)/\alpha$. By incorporating CIC reuse techniques, the total number of required physical CICs can be less than the activation count M. Taking a 7-bit ADC ($N = 7$) as an example, setting $\alpha = 1/8$.

The conventional architecture requires $2^7 - 1 = 127$ equivalent CICs. The proposed architecture, combined with the reuse strategy, requires only 8 physical CICs (accomplishing a total of 14 charge injection operations through reuse) to achieve 128 LSB levels. The reduction in the number of physical CICs from 127 to 8 corresponds to an area saving of 93.4% as presented in Fig. 6.

The linearity of our CIC-reuse structure critically depends on the accuracy of the division ratio α, which is essentially the capacitor ratio $C_{div}/(C_{div} + C_{int})$. In advanced CMOS processes, using high-precision metal-oxide-metal (MOM) capacitors enables matching accuracy better than 0.1%. Also, while the absolute values of the capacitors may change due to process corners and temperature, their ratio remains highly stable. Thus, the division ratio α is fairly stable with process, voltage, and temperature variations, leading to the stability of the ADC gain and relaxing the circuit requirements for complicated external calibration circuits.

During the implementation of this circuit in practice, it is required that the switching transistors within the CIC units are designed to operate in the saturation region so that charge injection does not introduce nonlinearity. As laid out in Section 2.1, this design uses a dual-side sample-at-a-time scheme, as shown in Fig. 4. This offers enough drain-source voltage for the CIC units in the LSB conversion path. Thus, it makes sure the CIC units operate as current sources in their linear

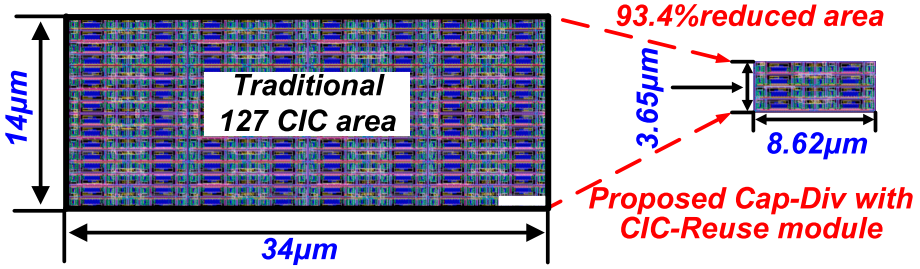


Fig. 6. Comparison of traditional CIC unit with CIC-reuse module.

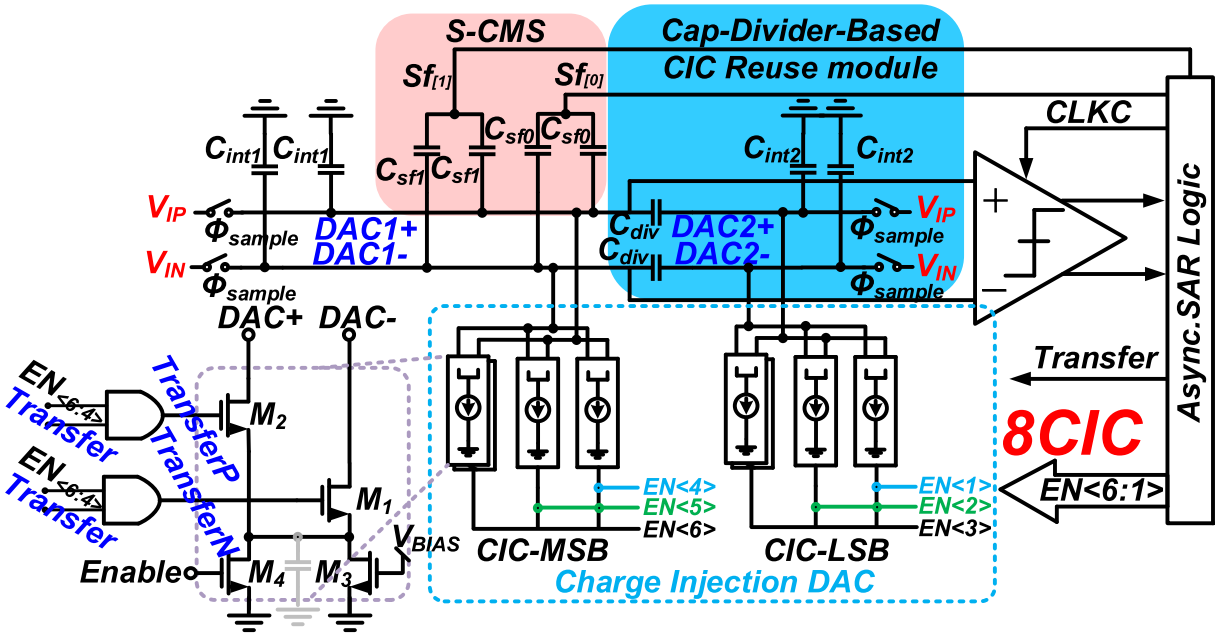


Fig. 8. Detailed circuit implementation of the proposed CI-SAR ADC.

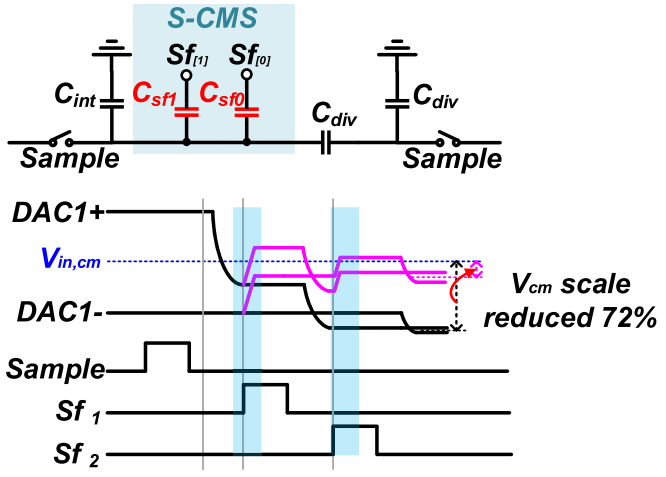


Fig. 7. Operating principle and timing diagram of the s-cms technique.

region. Moreover, it helps to maintain the accuracy of charge injection. (See Fig. 8.)

3. Circuit implementation

3.1. Segmented common mode shifting module

As already stated, common-mode voltage $V_{in,CM}$, at the comparator input node decreases continuously during conversion, which degrades linearity. As shown in Fig. 7, each charge injection event by a CIC unit removes a fixed amount of charge from the integration capacitor, causing a negative step in $V_{in,CM}$. This voltage drop causes rather significant degradation in performance. The value of V_{DS} of the transistor M3 being the current source in the unit CIC decreases accordingly. Lowering V_{DS} near the linear area. Then, linear area is obtained. However, it also alters the trans conductor and output resistance of transistor. This creates a change in the input voltage that defines injected charge amount Q_{CIC}. Thus, it causes nonlinear distortion. Conventional dynamic comparators like the strong arm latch show a large sensitivity of regeneration speed and offset voltage to input common-mode voltage. A reduction in $V_{in,CM}$ leads to an increase in the comparator's decision delay, which in turn creates a dynamic offset that degrades the ADC's linearity significantly.

To overcome the degrading effects of common-mode voltage drop, conventional methods-e.g. the use of fully customized comparators with a high common-mode rejection ratio, or the introduction of PMOS pull-up CIC arrays at the cost of area and matching performance-often have high complexity or cost. To overcome this, a low-complexity segmented S-CMS technique is employed in this work.

The signal path uses two coupling capacitors Csf1 and C_{sf2} controlled by switches. The capacitors are engineered precisely so that $C_{sf1} = 2C_{sf2} = 2C_{unit} = 1.15fF$. This particular capacitance ratio is scaled to counter the successive halving of common-mode voltage drops, which are caused by binary-weighted charge injection, compensating for drops of varying magnitudes.

The working principle of this technique is based on capacitive coupling and charge conservation. Specifically, through precise timing control, after each major charge injection and before the comparator's next decision, the control signals $Sf_{[1]}$ or $Sf_{[0]}$ instantaneously switch the bottom plate of the corresponding coupling capacitor C_{sf1} *or* C_{sf2} from the ground potential to the supply voltage V_{DD}. Taking C_{sf1} as an example, at the switching instant, the potential of its bottom plate transitions from *GND* to V_{DD}, generating a positive voltage step with an amplitude of V_{DD}. Because the charge across the capacitor cannot change instantaneously, following the principle of charge conservation, this voltage step is coupled through the capacitor, appearing largely across the capacitor's top plate (i.e., the plate connected to the DAC1 node), thereby generating a positive voltage lift with a magnitude of V_{shift1} at this phase. The amplitude of this lift voltage is determined by the capacitive division ratio and can be expressed by Eq. (6):

$$V_{shift1} = \frac{C_{sf1}}{C_{total}} \cdot V_{DD} \tag{6}$$

where C_{total} is the total capacitance to ground at the DAC1 node. The main aspect of this circuit is that the coupling path is implemented using switched capacitors. After the switching operation is completed, the switch opens, leaving the path in a high-impedance state with no DC current path. Consequently, the voltage lift generated via capacitive coupling can be effectively maintained at the DAC1 node, enabling an active and low-power method for common-mode voltage regulation.

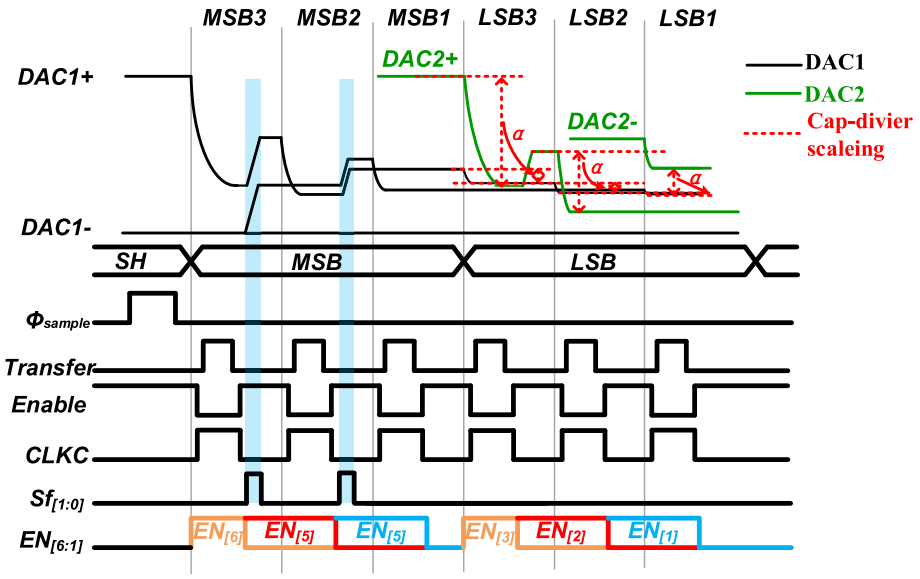


Fig. 9. Operation and control timing of the proposed CI-SAR ADC.

The timing of this technique is closely synchronized with the conversion flow, as shown in Fig. 7. During the sampling phase, $Sf_{[1:0]}$ are at low levels, the bottom plates of the coupling capacitors are grounded, the shifting circuit is inactive, and normal signal sampling is unaffected [20–22]. The first shift occurs after the first comparison and charge injection in the MSB stage, when $V_{in,CM}$ experiences its first large drop. The control logic then sets the $Sf_{[1]}$ signal, connecting the bottom plate of $Sf_{[1]}$ to V_{DD}. As described earlier, this induces a voltage lift V_{shift1} at the DAC1 node via capacitive coupling. Its value can be designed to be 12 ΔV according to Eq.(6), thereby compensating for most of the common-mode drop caused by the first large-weight charge injection and restoring $V_{in,CM}$ to a higher and safe operating range. After the second bit decision and charge injection, $V_{in,CM}$ drops again but with a smaller magnitude than the first time. The $Sf_{[0]}$ signal is then activated, generating a smaller voltage lift $V_{shift0} = 6\Delta V$ through C_{sf0} to counteract this drop. Upon entering the LSB conversion stage, the change in $V_{in,CM}$ caused by each charge injection in stage DAC2-stage is significantly reduced due to the attenuation of the capacitive voltage-division module, falling within the circuit's tolerable range. Therefore, no active shifting is performed thereafter to reduce power consumption and simplify timing control.

To sum up, the common-mode shifting technique which is segmented in nature succeeds to stabilize the common-mode voltage at a low, safe and high level between the supply voltage and ground with the help of precise voltage adds at critical conversion nodes requiring minimal hardware overhead. Compared to the uncompensated case, this technique reduces the drift range of the common-mode voltage by 72% (from $-25\Delta V$ to-$7\Delta V$), significantly relaxing the design constraints for the subsequent comparator and CIC units.

To meet the stringent requirements for high area efficiency and energy efficiency in computing-in-memory macros, a 7-bit column-parallel ADC is implemented in this work. Fig. 9 shows the architecture block diagram of the ADC. It is primarily composed of a charge-injection DAC module, a capacitive-divider-based CIC reuse module, a segmented common-mode shifting block, and an asynchronous SAR logic scheme. The charge-injection DAC comprises 8CIC units. These CICs are controlled by the enable strobe signals $EN_{<6:1>}$, generated by the shift register within the asynchronous SAR logic, to achieve reuse. During the

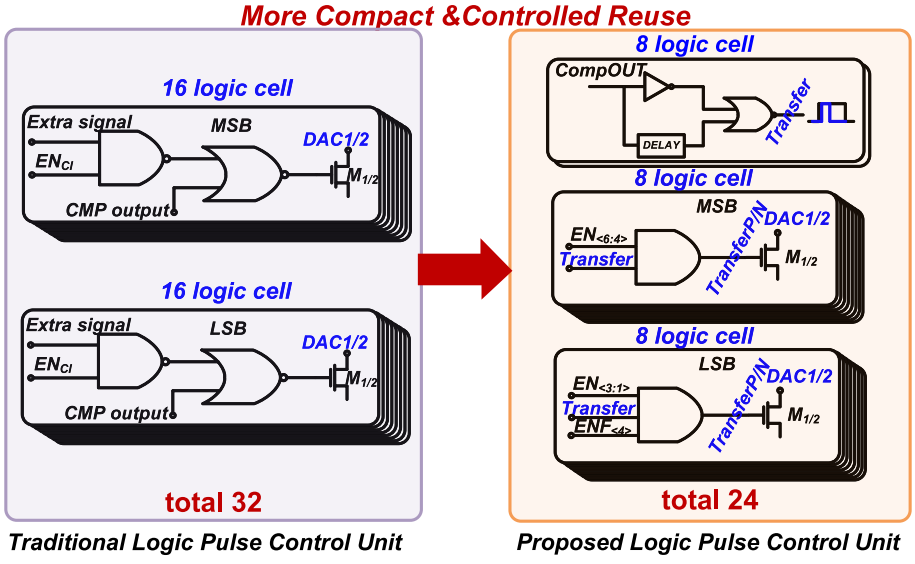


Fig. 10. Conventional and Proposed pulse gating logic circuits.

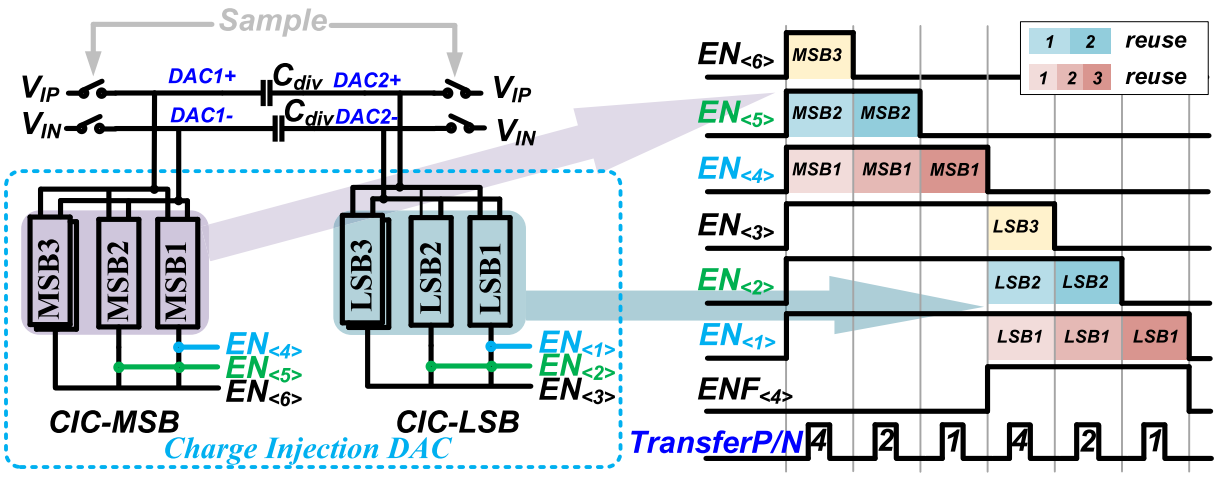


Fig. 11. Logic implementation of the two-stage CIC Reuse strategy.

sampling phase, the input switch closes, and the analog multiply-accumulate result (i.e., the analog MAC voltage V_{MAC}) output from the CIM array column line is sampled and held as the initial voltage for the ADC conversion. In the subsequent conversion phase, the switch array is reconfigured, and the ADC enters a two-stage charge injection conversion process. Through the cooperative operation of stage 1 coarse quantization and stage 2 fine quantization, the sampled voltage is accurately quantized into a 7-bit digital code.

Fig. 10 illustrates the operation timing diagram of the ADC. The complete workflow consists of three stages: sample-and-hold, MSB conversion, and LSB conversion. During the sampling phase, the sampling switch closes, directly sampling the analog MAC voltage V_{MAC} output from the CIM array and storing it onto the differential integration capacitors C_{int1} and C_{int2}. The purpose of this operation is to introduce the differential voltage at the comparator input equal to VMAC. After the sampling phase is complete, it enters the quantization phase. The sampling switch opens at this point, and the differential nodes connected to C_{int1} and C_{int2} enter a high-impedance state, preserving the sampled charge. Concurrently, the CIC array begins operation. During the MSB conversion stage, DAC1-stage is activated by $EN_{[4]}$. The enable signals $EN_{[6:4]}$ control the corresponding number of CIC units to perform charge injection, accomplishing the successive approximation conversion for the upper three bits (MSBs). After the first two conversions within the MSB stage are completed, the control signals $Sf_{[1:0]}$ sequentially switch the bottom plates of the coupling capacitors C_{sf1} and C_{sf2} from ground potential to the supply voltage, generating voltage steps that lift the integration node voltage V_{int}, thereby implementing the segmented common-mode shifting. Subsequently, the diagram enters the LSB conversion stage, where stage 2 is enabled. The enable signals $EN_{[3:1]}$ control the CIC units within the fine quantization stage to perform charge injection, thereby achieving high-precision quantization for the lower three bits (including 1 redundant bit).

The charge-injection cell is the main circuit for achieving precise charge injection. The simplified CIC circuit adopted in this design is shown on the left side of Fig. 9. This cell primarily consists of transistors M1, M2, and M3. M1 and M2 serve as a differential pair, with their drains connected to the top-plate nodes DACP and DACN of the differential integration capacitors, respectively. M3 acts as a common-source node, forming a current source controlled by the bias voltage V_{bias}, which is used to precisely set the discharge current. The operation of the CIC comprises two key phases: the discharge phase and the reset phase. During the discharge phase, the enable strobe signals $EN_{[6:1]}$ and the global transfer signal $T_{transfer}$ are used as logic AND gates to generate the activation signals. $T_{transferP}$ or $T_{transferN}$. When an activation signal is high, the corresponding switch transistor M1 or M2 turns on, forming a discharge path from the integration capacitor through M3 to ground. The integration capacitor is discharged by the constant current set by M3. The net effect is the injection of a charge packet that is equal to Q_{CIC} within the fixed pulse width. After the discharge is completed, the global transfer signal Transfer goes low during the reset phase. Now, both M1 and M2 are off irrespective of the state of enable signals $EN_{[6:1]}$. At the same time, a dedicated reset signal Enable goes active (e.g., goes high) to turn on transistor M4. The reset switch M4 quickly pulls the drain node potential of M3 down to ground. Transistor M4 is assigned for reset operation in this design, which effectively prevents any leftover charge from one injection affecting the next. Each charge injection is independent and helps reset the cell for the next discharge.

In the CIC-reuse architecture, the LSB weight represented by the CIC is directly determined by Q_{CIC}. For the first stage, or MSB path, a single CIC is designed to correspond to 8 LSBs. For the second stage, or LSB path, a single CIC corresponds to 1 LSB. The gate bias voltage V_{bias} of M3 is adjusted to achieve this weighting. Nevertheless, the amount of the CIC discharge is very sensitive to PVT (process corner, voltage and temperature). The final Q_{CIC} is influenced by V_{bias}, transistors' threshold voltage V_{TH}, and the width of the control pulse, possibly causing gain mismatch of DAC1-stage and DAC2-stage.

To compensate for these PVT variations, V_{bias} is designed to be adjustable. An off-chip calibration circuit or an on-chip calibration module based on a single replica CIC can be employed to generate an optimized V_{bias} voltage, which is then shared among all channel ADC units. As there is 1-bit redundancy introduced in the architecture, the requirements for V_{bias} calibration accuracy can be relaxed, thereby simplifying its calibration process.

3.2. Area-efficient pulse gating and reuse logic

In order to further improve the area utilization, an efficient pulse gating logic is adopted in the driving circuit of CIC cells. The conventional driver is present in the left of Fig. 10. By inserting a number of logic gates into the pulse path, this will increase the circuit area and logic delay, which is also sensitive to PVT variations. Along with that, this affects the effective pulse width being delivered to the CICs, which in turn impact the accuracy of charge injection.

This work employs a simplified pulse gating strategy, whose structure is shown in the right Fig. 10. The pulse signal CompOUT from the global comparator is directly fed to the input of an AND gate that drives each CIC unit. The signal of this AND gate is controlled by the corresponding strobe signal $EN_{<6:1>}$. When the *EN* signal is inactive, the driver gate is powered down, and no output pulse is generated. When the *EN* signal is active, the driver gate is powered, allowing the global pulse signal to be delivered to the target CIC unit without any additional logic delay. This method ensures the integrity and consistency of the pulse

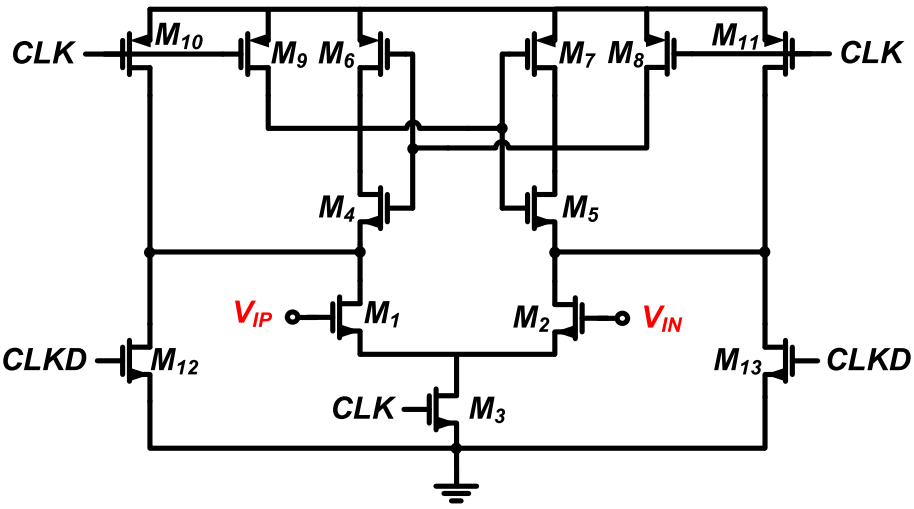


Fig. 12. Proposed g_m-boosted strong-arm comparator.

width, achieving robust charge control that is insensitive to PVT variations.

The specific reuse logic is implemented in Fig. 11. A simple shift-register-based state machine generates the $EN_{<6:1>}$ strobe signals according to the conversion sequence determined by the SAR logic. The total of 8 CIC units are divided into two independent groups, used for the MSB and LSB conversion stages respectively, with the switching between the two groups controlled by the highest-order enable signal $ENF_{<4>}$.

During the MSB stage (upper 3 bits), the strobe signals $EN_{<6:4>}$ activate the corresponding CIC groups in the binary-weighted sequence [1,3,4]. During the LSB stage (lower 3 bits +1 redundant bit), the strobe signals $EN_{<3:1>}$ are activated following the same [1,3,4] sequence. It is important to note that different *EN* signals have different fan-out loads (e.g., $EN_{<6>}$ drives the gate capacitance of 4 CICs, while $EN_{<1>}$ drives only one). To ensure consistent pulse edge rates across all *EN* signal paths, buffers driving different fan-out loads are custom sized with different transistor widths W/L. For example, the buffer that drives $EN_{<6>}$ has the highest width/length ratio while the buffer that drives $EN_{<1>}$ has the lowest width/length ratio. The load-matching scheme causes the activation pulses entering each respective CIC unit to have fixed settling times throughout the conversion process and improves linearity even further.

3.3. Strong-arm comparator

The fall of common-mode voltage, as mentioned in Section 2, deteriorate the performance of standard comparators. This issue can be resolved with the help of techniques like the use of a pre-amplifier but they usually incur large power and area overheads [23,24]. To fix this trade-off, we use an area-efficient g_m-boosted strong-arm comparator in our work, whose circuit structure is shown in Fig. 12.

The comparator builds upon the classic strong-arm latch structure by adding only two pull-down transistors M12, M13 controlled by a delayed clock signal, CLKD. The basic idea is to make use of simple timing control not complex analog circuitry to improve the comparator performance under low common-mode voltage. In the beginning, this comparator works like the Strong-Arm latch. When the regeneration phase starts, delayed clock (CLKD) signal gets activated, switching on M12 and M13. The additional discharge path is not limited by the transconductance of the input differential pair as caused by these transistors. This dynamically enhances the effective transconductance of the comparator at the critical time of regeneration, which substantially accelerates the decision-making under low common-mode voltage and helps to suppress dynamic offset. When compared to the construction of

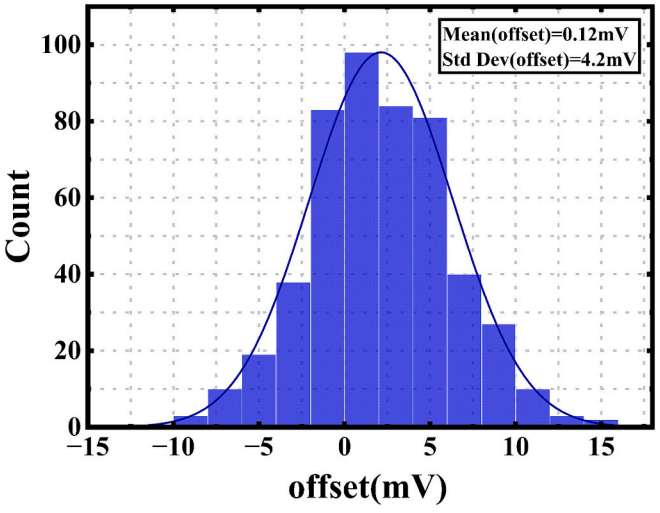


Fig. 13. Monte-Carlo analysis with 500 iterations:offset.

a pre-amplifier, this design has a very efficient area. It adds only minimum-sized two transistors with negligible area overhead. For column-parallel ADC arrays, this is important because the small area saving per comparator translates to a significant amount when

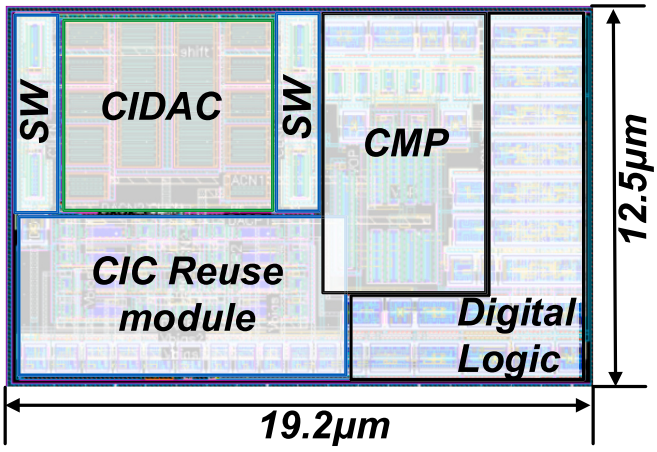


Fig. 14. Layout implementation for the proposed ADC.

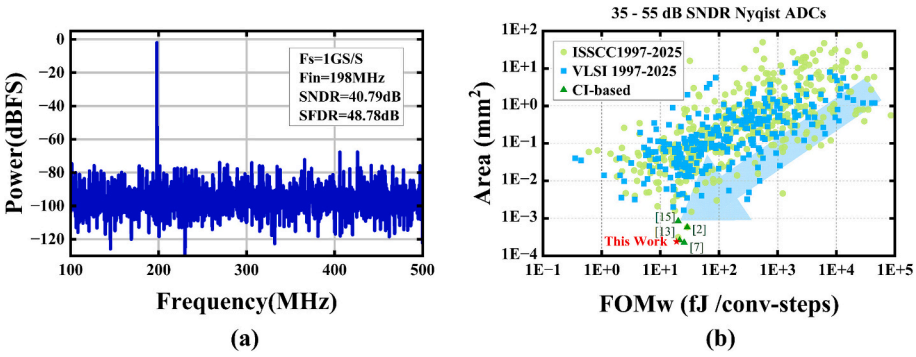


Fig. 15. (a) Simulated power spectral density (b) Performance comparison by area versus FoMw.

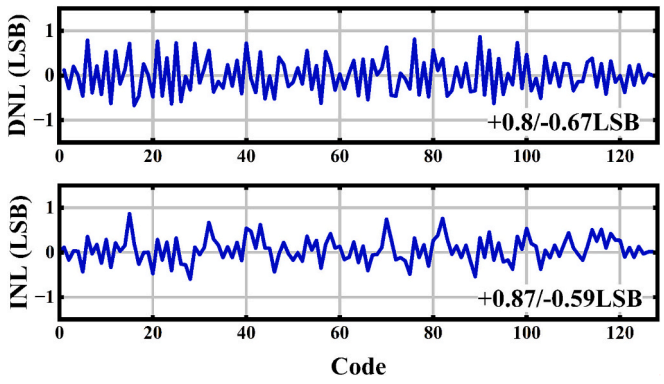


Fig. 16. Simulated DNL and INL.

multiplied by hundreds of ADCs. Thus, this structure guarantees the linearity and conversion speed of the ADC over a large common mode voltage range without actually taking up any area. It is a fundamental building block in realizing a highly robust area-efficient CI-SAR ADC.

The output offset performance of the g_m-boosted strong-arm comparator design is evaluated using a 500 run Monte-Carlo simulation as shown in Fig. 13. The simulation accounts for both transistor threshold voltage VTH mismatches and process variations. Overlaying the input-referred offset voltage distribution results in a standard deviation $\sigma = 4.2$ mV. It equals to a 3σ offset of 12.6 mV. Therefore, it is well within the acceptable offset for the ADC's 7-bit resolution target and does not require extra calibration circuitry.

4. Simulation results

A standard 28 nm CMOS process validates the suggested implementation of proposed ADC design. The layout is displayed in Fig. 14 and proposed 7-bit CI-SAR architecture has strong area efficiency as shown with a compact core area of only 0.00024 mm^2.

Under 1 V and at a sampling frequency of 1 GS/s, the ADC exhibits good dynamic performance characteristics. Fig. 15(a) shows the simulated output power spectral density for near-Nyquist input signal of 198 MHz. The ADC achieves a signal-to-noise distortion ratio (SNDR) of 40.79 dB and spurious-free dynamic range (SFDR) of 48.78 dB. Thus, ADC shows good dynamic performance making it suitable for medium-resolution applications. As in Fig. 15(b), the area-efficiency comparison against the FoMw is present for recent reports in ISSCC1997–2025 and CICC 1997–2025. Because the lower left corner is the optimal solution, that compared with almost all previous report works, our design has the best compromise between area and FoMs.

The differential non-linearity (DNL) and integral non-linearity (INL) measurements help to evaluate the linearity performance of the ADC. As depicted in Fig. 16, The INL is within +0.87/−0.59 LSB, and DNL is within +0.8/−0.67 LSB for the ADC. The segmented common-mode shifting technique achieves linearity of conversion during the quantizing process, as confirmed by these results.

The dynamic performance across frequency and amplitude variations is also systematically characterized. Fig. 17(a) illustrates the SNDR and SFDR versus input frequency, showing stable operation across the entire Nyquist band with minimal performance degradation. Fig. 17(b) demonstrates the SNDR versus normalized input amplitude, confirming the ADC's linear scaling with input signal strength and proper handling of full-scale inputs.

To assess the robustness of the proposed design against manufacturing and operational variations, we did detailed post-layout PVT corner simulations involving five process corners and a supply voltage of 0.9 V to 1.1 V, and a temperature range between −40 °C and 85 °C.The SNDR results for all the 45 corners are summarized in Fig. 18 and plotted for three typical temperatures, respectively .In total, the SNDR varies within a window of 3.1 dB, from a minimum of 38.7 dB to a maximum of 41.8 dB. The only discrepancy is the effect of PVT-dependent discharge current of the CIC units on the effective LSB weight. In particular, the worst drop from nominal is less than 2.1 dB,

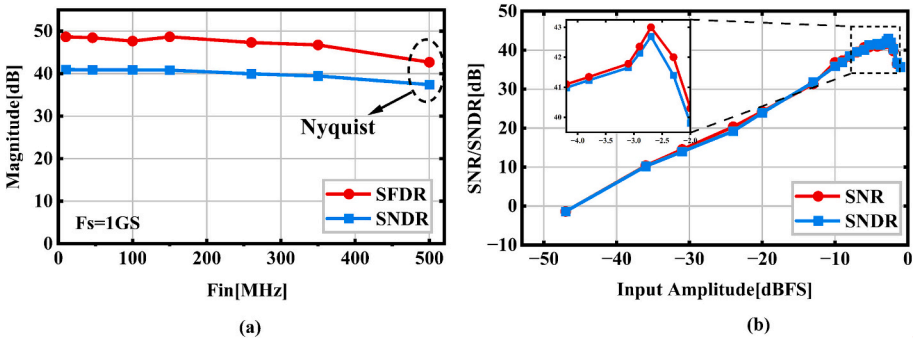


Fig. 17. (a) Simulated SNDR and SFDR across $F_{in.}$ (b) Simulated SNDR over different input amplitude.

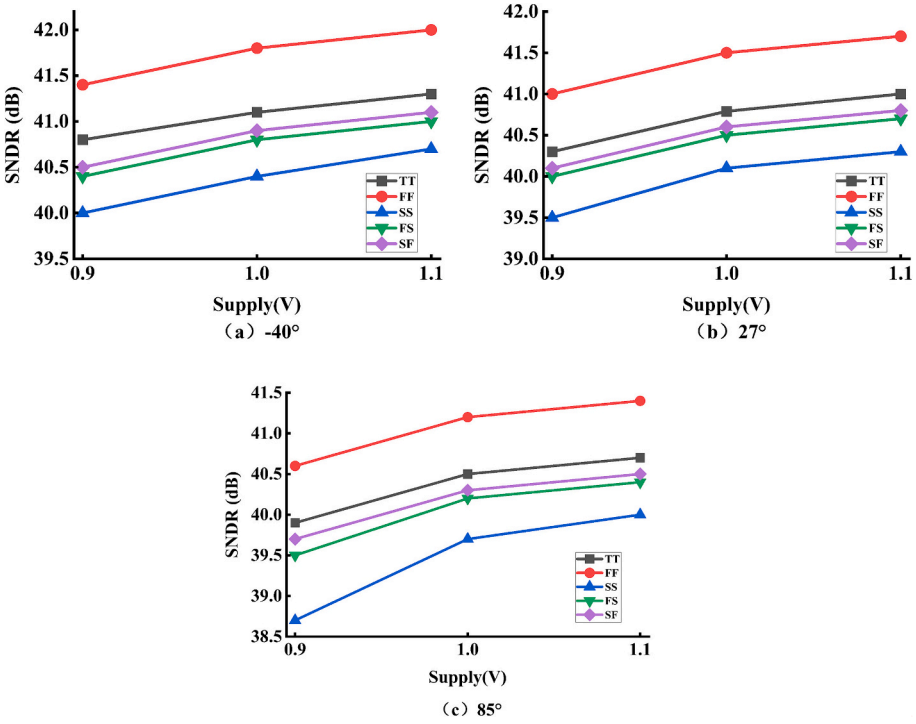


Fig. 18. Simulated SNDR across PVT 45 corners: (a) -45°, (b) 27°, (c) 85°.

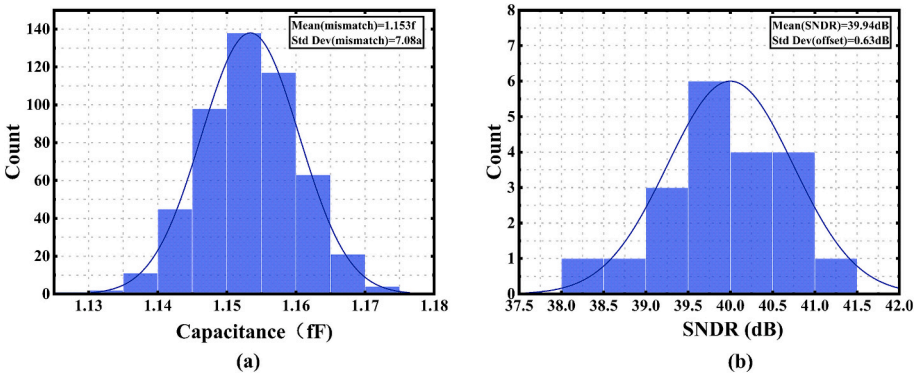


Fig. 19. (a) Monte-Carlo analysis with 500 iterations: unit MOM capacitor (b) Monte-Carlo analysis with 500 iterations: SNDR of the ADC.

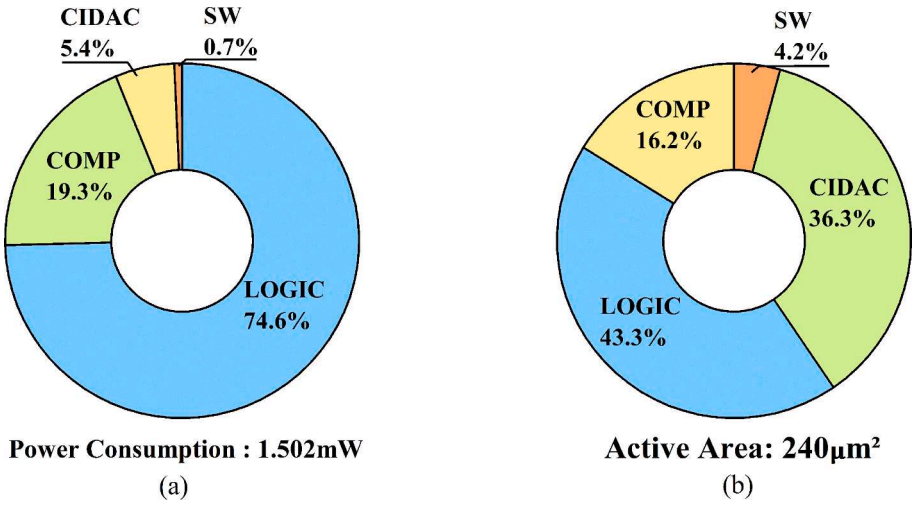


Fig. 20. (a) simulated power and (b) area breakdowns.

Table I
Performance comparison with other works.

Reference	[10]2025 TCASII	[9]2025 TCASII	[13]2023 ASSCC	[12]2025 ISSCC	[7]2024 JSSC	[25]2022 ISCAS*	This Work*
Architecture	C-CI SAR	CI-SAR	C-CI SAR	CI-SAR	CI-SAR	CI-SAR	CI-SAR
Technology	28 nm	65 nm	28 nm	40 nm	28 nm	22 nm	28 nm
Supply (V)	0.9	1.2	1	1	0.95	0.8	1
Fs (Hz)	0.7G	0.16G	1G	0.8G	1.1G	34 M	1G
Resolution(bits)	7	8	8	7	6	5	7
SNDR	38.7	44.9	43.5	40.7	35.2	30.5	40.79
SFDR	53.1	49.9	54.1	64.1	49.4	–	48.78
Power(mW)	0.835	0.65	2.61	2.89	1.32	2.924 pW	1.502
Area(μm^2)	259	1300	261	5600	2400	75	**240**
[1]Walden FoM (fJ/conv-step)	17.03	28.2	21.3	40.6	25.5	21	18.9

[1] Walden Figure of Merit , $FoM = P_{DC}/(F_{S,NYQ} \bullet 2^{ENOB})$.
* Post-simulation Results.

demonstrating the inherent stability of the capacitor-ratio-based voltage division and affirming the overall robustness of the proposed architecture.

These Monte Carlo simulations are also performed to look at the effect of device mismatch, taking into account both transistor local variation and capacitor mismatch. The unit MOM capacitors of 1.153fF are given by the 28 nm PDK itself with an existing statistical model. Run Monte Carlo simulation of one capacitor shown in Fig. 19(a) gives the average capacitance 1.153fF, and standard deviation 7.08aF which is well below the required tolerance of 7 bits. CI-SAR ADC 200-run Monte Carlo simulations at 1 GS/s with a 198 MHz input, including the transformer mismatch of the transistor and capacitor are shown in Fig. 19(b). The SNDR has mean 39.94 dB and std. dev 0.63 dB, and the minimum SNDR>38.4 dB.

The power distribution across the major circuit blocks is illustrated in Fig. 20(a). It is clear from the diagram that the circuit blocks with the most power consumption are the CIC array and the digital logic. Fig. As illustrated in Fig. 20(b), a breakdown of the area is shown indicating a significant total area saving due to the capacitive-division CIC-reuse technique. It can be noted that the area of the CIC array is 36.3% of total area for this design.

Performance comparison with the recently published state-of-the-art works of similar resolution is made in Table I. The proposed design achieves a good trade-off between area 240μm^2, sampling rate up to 1GS/s and energy efficient FoMw of 18.9 fJ/conv-step. Compared with almost all recent works, our ADC achieves a greatly superior area efficiency and competes in energy efficiency. Thus, it is suitable for CIM and other multi-channel applications with area constraints.

5. Conclusion

An area-efficient, 7-bit CI-SAR ADC is presented for integration into CIM macros to achieve high computational density and energy efficiency. To overcome chip area limitation, a novel capacitive-divider-based CIC-reuse idea is introduced. Proposed architecture seamlessly integrates a capacitive voltage-division scheme with a CIC reuse strategy, enabling a single CIC-cell to generate precise sub-LSB voltage steps, thereby achieving a drastic 93.4% area reduction. The accompanying segmented common-mode shifting technique provides a low-overhead solution to maintain conversion linearity under varying operating conditions by stabilizing the common-mode voltage. Simulation results demonstrate state-of-the-art area efficiency with a FoMw of 18.9 fJ/conv-step and a compact chip area of only 0.00024 mm^2.

CRediT authorship contribution statement

Siwan Dong: Writing – review & editing, Writing – original draft, Funding acquisition, Conceptualization. **Zhao Liu:** Writing – original draft, Data curation. **Bin Zhang:** Software, Data curation.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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Data availability

No data was used for the research described in the article.

References

[1] Liu Y, Zhao R, Xiao H, et al. An XOR-10T SRAM computing-in-memory macro with current MAC operations and time-to-digital conversion for BNN edge processors. AEU Int J Electron Commun 2024;182:155346.
[2] Amir M. Hajisadeghi, Hamid R. Zarandi, Mahmoud Momtazpour. Stoch-IMC: a bit-parallel stochastic in-memory computing architecture based on STT-MRAM. AEU Int J Electron Commun 2025; 190:155614.
[3] Choo K, Bell J, Flynn MP. 27.3 Area-efficient 1GS/s 6b SAR ADC with charge-injection-cell-based DAC. In: IEEE International Solid-State Circuits Conference (ISSCC); 2016. p. 460–1.
[4] Choo K, An H, Sylvester D, Blaauw D. 27.2 14.1-ENOB 184.9 dB-FoM capacitor-array-assisted cascaded charge-injection SAR ADC. In: IEEE International Solid-State Circuits Conference (ISSCC); 2021. p. 372–4.
[5] Lee K, Song S, Chae H. A 389μm 2 26.7 nW 8-bit 100kS/s SAR ADC with Hybrid C- CI DAC. In: IEEE International Symposium on Circuits and Systems (ISCAS); 2025. p. 1–4.
[6] Kye CH, Byeon YJ, Choo K, Choo MS. Design methodology for compact Single-Channel 3-stage capacitor-Array-assisted charge-injection DAC-Based SAR ADC. IEEE Trans Circuits Syst I: Regular Papers 2024;71(11):4973–84.
[7] Kim J, Cho G, Kim J. A 7 GHz ERBW 1.1 GS/s 6-bit PVT tolerant asynchronous charge-injection SAR with only 8.5 fF input capacitance in 28 nm CMOS. J Solid-State Circuits 2024;59(3):765–73.
[8] Runge M, Schmock D, Gerfers F. Noise and non-linearity analysis of a charge-injection-cell-based 10-bit 50-MS/s SAR-ADC. In: IEEE 60th International Midwest Symposium on Circuits and Systems (MWSCAS); 2017. p. 1025–8.
[9] Dong S, Wang J. An 8-bit 160-MS/s charge injection SAR ADC with build-in offset calibration for computing-in-memory macros. Trans Circuits Syst II: Exp Briefs 2025:1–5.
[10] Park J, Park J, Song S, Chae H. A 17-fJ/conv-step FoMw and 259-um2 7-bit C-CIDAC SAR ADC. Trans Circuits Systems II: Exp Briefs 2025;72(11):1535–9.
[11] Caselli M, Papistas IA, Cosemans S, et al. Charge sharing and charge injection A/D converters for analog in-memory computing. In: IEEE International New Circuits and Systems Conference (NEWCAS); 2021. p. 1–4.
[12] Veraverbeke B, Tavernier F. A Cryo-CMOS 800MS/s 7b CI-SAR with only 4fF Input Capacitance and 64dB SFDR. In: IEEE International Solid-State Circuits Conference (ISSCC); 2025. p. 1–3.
[13] Kye CH, Choo K. A 0.000261 mm 2 single-channel 1 GS/s 8-bit 3-stage capacitor array-assisted charge-injection DAC-based SAR ADC in 28 nm CMOS. In: IEEE Asian Solid-State Circuits Conference (A-SSCC); 2023. p. 1–3.

[14] Runge M, Schmock D, Scholz P, Gerfers F. A 100-MS/s 9-bit charge-injection cell based SAR-ADC in 65nm LP CMOS. ITG/GMM-Symposium 2020:1–4.
[15] Ma Y, Yu X, Tan Z, Zhao L. A sram compute-in-memory macro based on direct coupling sar adc and dac reuse. In: IEEE International Symposium on Circuits and Systems (ISCAS); 2024. p. 1–5.
[16] Zang Q, Goh WL, Lu L, Yu C, Mu J, Kim TT, et al. 282-to-607 TOPS/W, 7T-SRAM based CiM with reconfigurable column SAR ADC for neural network processing. In: IEEE International Symposium on Circuits and Systems (ISCAS); 2023. p. 1–5.
[17] Jo Y, Yang C, Zheng Y, Kim TT. Similarity-Aware Transposable SRAM Computation-In-Memory with Pulse-Based SAR ADC. In: IEEE Asian Solid-State Circuits Conference (A-SSCC); 2024. p. 1–3.
[18] Xu X, Ma Y, Yu X, Meng F, Yu WH, Zhao L. A 10-bit Two-Stage Pipeline SAR ADC in 55nm CMOS for Compute-in-Memory Applications. In: IEEE Asia Pacific Conference on Circuits and Systems (APCCAS); 2024. p. 140–3.
[19] Jo YJ, Zhang X, Liu J, Zhou J, Zheng Y, Kim TT. Transposable 9T-SRAM computation-in-memory for on-chip learning with probability-based single-slope SAR hybrid ADC for edge devices. IEEE Solid-State Circuits Letters 2023;6:81–4.
[20] Song S, Lee K, Chae H. An 8-bit 20.2 fJ/conv-step FoM CI-C Asynchronous SAR ADC with Common-mode Level Shifting. In: IEEE Asian Solid-State Circuits Conference (A-SSCC); 2024. p. 1–3.
[21] Wang P, Li F, Wang Z. A single-channel 8-bit 1.6-GS/s alternate-comparator SAR ADC with dither-based background offset calibration in 28-nm CMOS. IEEE Transactions on Circuits and Systems I: Regular Papers 2025;72(9):4527–38.
[22] Park S, Kim C, Choi Y, Shim M, Lee W, Seo D, et al. A 7-bit 1.15-GS/s 2.6-bit/cycle asynchronous SAR ADC using comparator decision skip technique with background offset calibration. J Solid-State Circuits 2025:1–12.
[23] Xiao S, Li F, Hao T. Analog-to-Digital Converter Design for Diverse Performance Computing-in-Memory -Systems: A Comprehensive Review. In: IEEE Integrated Circuits and Systems (ICAS); 2025. p. 81–9.
[24] Ahrar A, Makhlooghpoor A, Lu X, Xu J, et al. A Capacitor-Saver Redundant SAR ADC to Optimize Readout in Compute In-Memory Systems. In: IEEE International Symposium on Circuits and Systems (ISCAS); 2025. p. 1–5.
[25] Caselli M, Bhattacharjee D, et al. Tiny ci-SAR A/D Converter for Deep Neural Networks in Analog in-Memory Computation. In: IEEE International Symposium on Circuits and Systems (ISCAS); 2022. p. 1823–7.