Research Square

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Passivation in Tunnel Oxide of Doped Polysilicon Structures Degraded by Spin-Dry Induced Charges and A Strategy to Reverse the Degradation

Vibhor Kumar
Rutgers, The State University of New Jersey
Munan Gao
Rutgers, The State University of New Jersey
Ngwe Zin
ngwe.zin@rutgers.edu

Rutgers, The State University of New Jersey

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Abstract

This study examines the impact of the **spin-dry process** on the surface passivation of silicon solar cells. Ultrathin silicon oxide layers were grown using the dissolved-ozone (DI-O_3) technique, producing highly uniform films with a thickness of 1.76 nm (± 2.42%). Despite this uniformity, samples subjected to spin drying and capped with n-type polysilicon exhibited markedly degraded passivation, reflected in a minority-carrier lifetime of 206 µs and an implied open-circuit voltage of 656 mV. The degradation was attributed to electrostatic charges generated by air–surface friction during spin drying, which accumulate on the insulating oxide and interfere with field-effect passivation. To mitigate this effect, an **enhanced spin-dry (SD) protocol** incorporating a brief deionized-water immersion was implemented. This modification effectively neutralized SD-induced charges and yielded substantial improvements, achieving a lifetime of 1,248 µs and an iVoc of 702 mV for n-poly-Si structures. These results underscore the importance of **charge management** during wafer drying and provide a practical route to improving passivation in advanced silicon solar-cell architectures.

Introduction

Crystalline silicon (c-Si) solar cells account for more than 90% of the global photovoltaic (PV) market, owing to the abundance of raw materials, cost-effectiveness, and well-established industrial production processes [1]. Despite these advantages, defects and surface contamination on silicon wafers remain critical challenges, as they intensify carrier recombination losses and thereby reduce both efficiency and open-circuit voltage [2–4]. To address these limitations, advanced surface cleaning techniques are essential, particularly for high-efficiency c-Si architectures such as passivated emitter rear contact (PERC), bifacial n-type, and interdigitated back contact (IBC) cells [5]. Broadly, cleaning approaches can be categorized into wet and dry methods. Wet cleaning employs solvents, additives, surfactants, scrubbing, oxidation, etching, and dissolution to remove contaminants, whereas dry cleaning relies on gas-phase chemistry driven by thermal, plasma, or radiation energy [6]. Although dry cleaning techniques using gases such as H_2 and CF_4 offer cost advantages over wet methods, they are less widely adopted due to their tendency to induce surface damage, which negatively impacts solar cell performance [7].

A wide range of wet-cleaning methodologies has been reported in the literature to achieve smooth, contamination-free silicon surfaces [5, 8–10]. An essential component of these processes is the final drying step, which is required not only after wet cleaning but also following every wet process in silicon solar cell fabrication, including saw-damage removal and surface texturing. Several drying techniques are employed for wet-cleaned wafers, such as spin drying, isopropyl alcohol (IPA) vapor drying, gas blow drying, hot air blow drying, vacuum drying, wafer withdrawal from hot water or IPA, and infrared drying [11–13]. Among these, spin or centrifuge dryers are widely adopted for processing large batches of wafers. However, the spin-drying process can introduce surface charging effects due to triboelectric interactions between the wafer and the drying environment. Reported phenomena include both localized charge accumulation and uniform charging across the wafer surface [14, 15]. While the consequences of

such charging effects have been extensively examined in semiconductor device manufacturing [13], their specific impact on silicon photovoltaic performance remains largely unexplored.

This study investigates the impact of spin-dry–induced surface charges on the passivation quality of silicon solar cells. A systematic analysis was conducted on two configurations: (i) an AlO_x/SiN_x/phosphorus-doped polysilicon (n-poly-Si) stack, and (ii) AlO_x deposited on ozonated silicon oxide (DI-O_3 oxide) grown silicon substrates. The results demonstrate that surface charges generated during spin drying significantly degrade passivation performance in both sample types. To address this issue, we introduce and implement an optimized spin-dry strategy that enhances passivation quality while maintaining compatibility with standard in-line manufacturing processes.

Experimental

In this experiment, n-type DSP Cz silicon wafers with a thickness of 250 µm, diameter of 100 mm, and resistivity of approximately 1 Ω·cm were employed. The wafers underwent a multi-step cleaning protocol beginning with treatment in 10 ppm ozone-dissolved deionized water at 25°C for 5 minutes, followed by immersion in 5% dilute hydrofluoric acid (HF) and rinsing with deionized water (DIW). Surface smoothing was subsequently performed using 25 wt% aqueous tetramethylammonium hydroxide (TMAH) at 85°C for 10 minutes, after which the wafers were rinsed again with DIW. To eliminate residual oxide formed during the TMAH etching step, a final HF dip was carried out, followed by a concluding DIW rinse.

Following the cleaning process, a fresh DI-O_3 oxide layer was grown on the silicon wafers. The oxide was formed by immersing the wafers in a dissolved ozone bath for 5 minutes, after which drying was performed using the spin-dry technique. For comparison, a subset of wafers was dried using an N_2 gun. The thickness and uniformity of the resulting oxide layers were characterized using a Filmsense ellipsometer.

Recent studies have highlighted the advantages of employing thinner polysilicon layers, which reduce deposition time and consequently lower the cost of ownership. Optimized thin polysilicon is also beneficial for minimizing free-carrier absorption in doped layers, thereby enhancing the bifaciality factor and reducing etch-back requirements [16–18]. In this work, the first set of DI-O_3 oxide–grown wafers was coated with 60 nm amorphous silicon (a-Si) on both sides using radio-frequency plasma-enhanced chemical vapor deposition (PECVD) at 350°C, with silane serving as the precursor gas. The deposited a-Si was subsequently phosphorus-doped in a furnace at 900°C for 30 minutes. Following doping, a dielectric stack comprising AlO_x/SiN_x (15 nm/70 nm) was deposited on both sides of the polysilicon structures. Finally, thermal annealing was performed in a box furnace at 450°C for 30 minutes under an N_2 atmosphere.

To corroborate the results obtained from the first wafer set, a complementary second set of DI-O_3–grown silicon wafers was prepared with 15 nm AlO_x deposited on both sides using a Fiji F200 thermal atomic layer deposition (ALD) system. Both wafer sets were subjected to spin-dry (SD) and N_2-gun dry

(ND) processing. Trimethylaluminum (TMA) and H_2O precursors were employed for AlO_x deposition, yielding a growth rate of 0.088 nm per cycle at 200°C. Following deposition, the AlO_x-coated samples were annealed in a box furnace under identical conditions to the n-poly-Si samples, i.e., at 450°C for 30 minutes in an N_2 ambient.

The third set of wafers was subjected to an enhanced SD process, consisting of a deionized water (DIW) dip followed by N_2 drying. Within this set, one group was subsequently deposited with an AlO_x/SiN_x/n-poly-Si stack, while the other group received only a DI-O_3 oxide/AlO_x stack on both sides. The deposition procedures for both groups followed the same protocols as those applied to the first and second wafer sets. For all sample sets, effective carrier lifetime (τ_{eff}) and saturation current density (J_0, per side) were measured using the transient photoconductance decay (PCD) technique with a Sinton system at excess carrier densities of $1x10^{15}$ cm^{-3} and $5x10^{15}$ cm^{-3}, respectively. J_0 was determined at injection levels several times higher than those used for τ_{eff} to improve measurement accuracy. This methodology ensures that excess carrier densities substantially exceed substrate doping, thereby extending the linear regime of carrier lifetime dependence on carrier density and enabling clear separation of surface and bulk recombination effects. Wafer spin drying was performed using a Semitool STI 870 Spin Rinser Dryer Double Stack, while SiN_x deposition was carried out in a Plasmatherm PECVD reactor. Uncalibrated photoluminescence (PL) imaging was employed to assess PL lifetime distributions. In this study, n-poly-Si refers to the stack configuration of n-poly-Si/DI-O_3 oxide/Si.

Results and Discussion

The thickness and spatial uniformity of the DI-O_3 oxide layer were measured at 49 locations across each sample, excluding a 5-mm edge region on all sides. The results, obtained via ellipsometry, are presented in Fig. 1(a) and 1(b).

Figure 1(a) shows that the DI-O_3 oxide grown on the SD-processed sample exhibits a thickness of 1.76 nm with a uniformity of ± 1.97%. The remaining wafers processed in the same run yielded a comparable average thickness of 1.76 nm with a uniformity of ± 2.42%. In contrast, Fig. 1(b) illustrates that the ND-processed sample displays significantly poorer uniformity, measured as 1.87 nm ± 13.5%. This non-uniformity is likely attributable to the drying step inherent to the ND technique, during which the DI-O_3 solution may remain in contact with certain wafer regions longer than others. Prior studies have shown that non-uniform oxide or dielectric layers in solar cells can degrade device performance: thinner regions can increase leakage current, suppress open-circuit voltage, and elevate interface-state density, while excessively thick regions can reduce fill factor and short-circuit current density [19, 20]. Taken together, these results indicate that the SD technique enables more precise and controllable formation of ultrathin DI-O_3 oxide layers compared to the ND method.

Figure 2(a) presents the τ_{eff} plots for the SD-processed n-poly-Si samples (pSi-SD_1 and pSi-SD_2), along with the corresponding iV_{oc} values obtained during the τ_{eff} measurements. Despite the highly uniform

and well-controlled DI-O_3 oxide thickness achieved by the SD technique, the measured PCD lifetimes—206 µs and 105 µs—and the associated iV_{oc} values—656 mV and 639 mV—are markedly low. These results indicate that the SD-processed samples exhibit notably poor surface passivation. To determine whether this poor passivation is specific to n-poly-Si, a second set of samples was prepared in which only AlO_x was deposited on DI-O_3-grown Si substrates (Si-SD_1 and Si-SD_2). As shown in Fig. 2(a), these SD-processed AlO_x/DI-O_3 samples also yielded low τ_{eff} and iV_{oc} values—276 µs and 666 mV, and 294 µs and 670 mV, respectively. Above experiments imply that the poor surface passivation arises from the SD processing itself rather than from the specific materials deposited. To further assess the influence of the processing method, a set of ND-processed DI-O_3-grown Si samples (Si-ND_1 and Si-ND_2) was also coated with AlO_x only. The corresponding PCD results, shown in Fig. 2(a), reveal that the ND-processed samples exhibit τ_{eff} and iV_{oc} values at least four times higher than those of the SD-processed counterparts—1190 µs and 716 mV, and 1327 µs and 719 mV, respectively. Quokka3 simulations were performed to fit the measured PCD data for both SD- and ND-processed AlO_x samples by varying J_0, substrate resistivity, substrate thickness, dopant concentration, and τ_{bulk}. As shown in Fig. 2(b), the simulated curves align well with the experimental data across most injection levels.

Figure 3 presents the uncalibrated PL lifetime images of the ND- and SD-processed AlO_x/DI-O_3-grown silicon samples. In general, strong PL intensity corresponds to enhanced radiative recombination of photogenerated carriers, whereas reduced PL intensity indicates suppression of radiative recombination due to the presence of interface defects [21, 22]. In the present study, the SD-processed samples exhibit noticeably lower—or nearly absent—PL emission compared to the ND-processed samples, indicating a high density of interfacial defects and consequently very poor surface passivation. Such defects promote non-radiative recombination, leading to significantly darker PL images [13].

The PCD and PL results collectively indicate that the SD technique induces unintended recombination pathways for photogenerated carriers, leading to markedly poor surface passivation in the processed samples [23]. In contrast, although the ND method provides superior passivation, its significant oxide-thickness non-uniformity makes it a less desirable option. The degradation in passivation observed for the SD technique may stem from static charges generated on the wafer surface during the spin-dry process. Prior studies [24, 25] have shown that spinning wafers in air produces electrostatic charge due to frictional interactions. For insulating layers such as the DI-O_3 oxide used here, these charges cannot readily dissipate and therefore remain trapped at the surface. The PCD and PL results suggest that such SD-induced charges counteract the beneficial fixed charges inherent to the passivating AlO_x/DI-O_3 stack, ultimately diminishing the overall passivation quality. A schematic illustration of this mechanism for SD-processed AlO_x/DI-O_3 structures is provided in Fig. 4(a).:

It is also well established that DIW contains ionic impurities originating from sources such as piping, processing equipment, and the intrinsic charging of the water itself [26]. We hypothesize that these ionic species may help mitigate or neutralize the static charges induced on the wafer surface during SD processing. A schematic representation of this mechanism for AlO_x/DI-O_3-passivated samples is shown

in Fig. 4(b). As a result, wafers subjected to a DIW immersion step are expected to exhibit improved surface passivation characteristics.

To validate the above hypothesis, SD-processed DI-O_3-grown samples were subjected to a brief DIW immersion followed by ND drying. This modified sequence is referred to as the enhanced SD process in this work. The DI-O_3 oxide thickness and uniformity obtained from ellipsometry measurements were 1.77 nm ± 2.59%, as shown in Fig. 5, demonstrating that the enhanced SD process achieves uniformity comparable to that of the conventional SD method. It is noteworthy that the DI-O_3 oxide uniformity achieved with the enhanced SD process—where drying concludes with ND—is still significantly better than that of the ND-only process, despite the poor uniformity previously reported for ND in Fig. 1(b). This is because ozone, the primary reactive species responsible for oxide growth, is expected to dissipate during the spinning step. Consequently, during the subsequent DIW dip and ND drying, the absence of reactive ozone and the presence of an already-formed DI-O_3 oxide layer prevent further oxidation of the silicon surface. A subset of the enhanced-SD samples was then coated with either an AlO_x/SiN_x/n-poly-Si stack or AlO_x alone, followed by furnace annealing as described in the Experimental Section.

Figure 6 presents the carrier-lifetime curves and extracted electrical parameters for the AlO_x/SiN_x/n-poly-Si and AlO_x samples processed using the enhanced SD technique. The resulting values of τ_{eff}, iV_{oc}, and J_0 are 1248 µs, 702 mV, and 18 fA/cm² for the n-poly-Si samples, and 1521 µs, 720 mV, and 3 fA/cm² for the AlO_x-only samples, respectively.

The uncalibrated PL images of the enhanced-SD-processed AlO_x/DI-O_3 and AlO_x/SiN_x/n-poly-Si samples are shown in Fig. 7(a) and 7(b), respectively. The PL intensities in both cases are substantially higher than those of samples processed using the conventional SD technique (see Fig. 3(b)). The extracted electrical parameters, together with the enhanced PL response, indicate a significant reduction in surface-related defects and, consequently, a reduction in non-radiative recombination of photogenerated carriers. Overall, the enhanced SD process improves surface passivation by approximately fivefold compared to the conventional SD method.

These results confirm that static charges generated during the SD process interfere with the surface passivation of the structures examined. Achieving high-quality passivation therefore requires the removal or neutralization of SD-induced charges. The implications of this work extend beyond DI-O_3-grown oxides: any insulating film subjected to a spin-dry process may experience similar charge-induced degradation in passivation.

Conclusion

In conclusion, this study demonstrates the significant impact of the spin-dry process on the surface passivation quality of silicon solar cells. Ultrathin DI-O_3 oxides were grown on the samples, followed by conventional SD processing, and passivation was achieved using an AlO_x/SiN_x/n-poly-Si stack. Our

results show that static charges generated during the SD step severely degrade surface passivation. To address this issue, we introduced an enhanced SD process incorporating a brief DIW immersion after spin drying. This modification led to substantial improvements in carrier lifetime, reductions in J_0, and increases in iV_{oc}. These enhancements indicate effective mitigation or neutralization of SD-induced static charges, thereby significantly improving the overall surface passivation of the samples.

Declarations

Funding Declaration

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Author Contribution

V.K. and M.G. undertook experiments, analyzed results, wrote and reviewed the manuscript.N.Z. acquired the funding, conceptualized the idea, managed the project, designed experiments, analyzed results, wrote and reviewed the manuscript.

Data Availability

This study generated original experimental data through ellipsometry, photoconductance decay, and photoluminesence.

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Figures

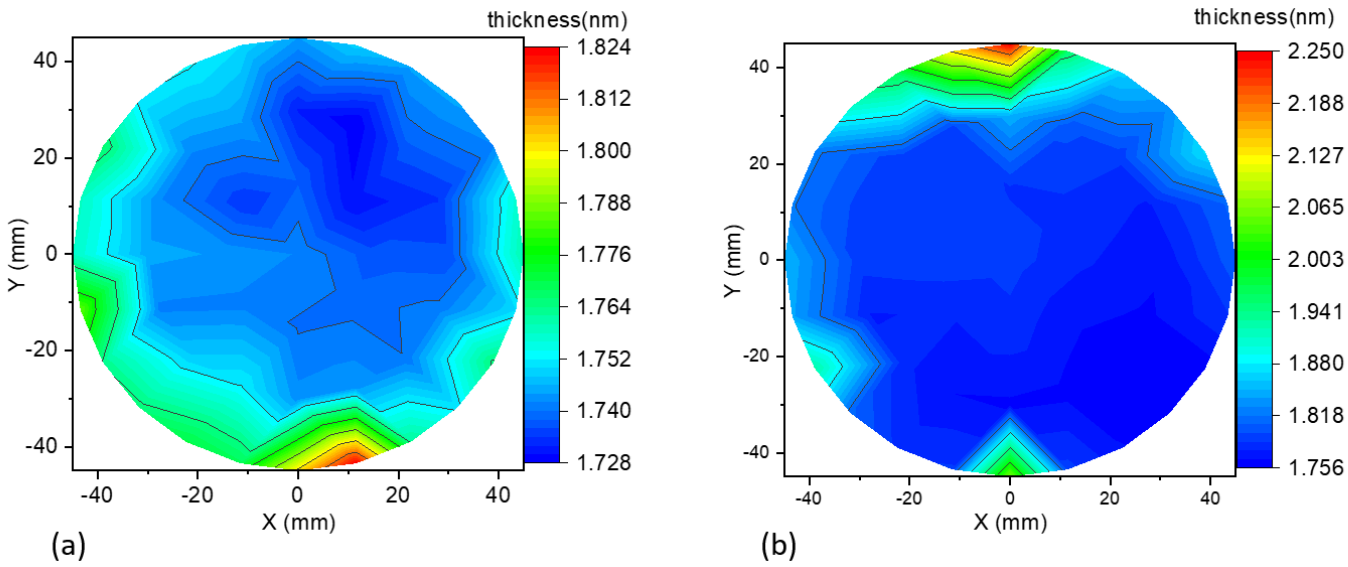


Figure 1

Ellipsometer measured contour chart of the thickness and uniformity (at 49 points) in the DIO_3 grown samples processed by (a) SD and (b) ND.

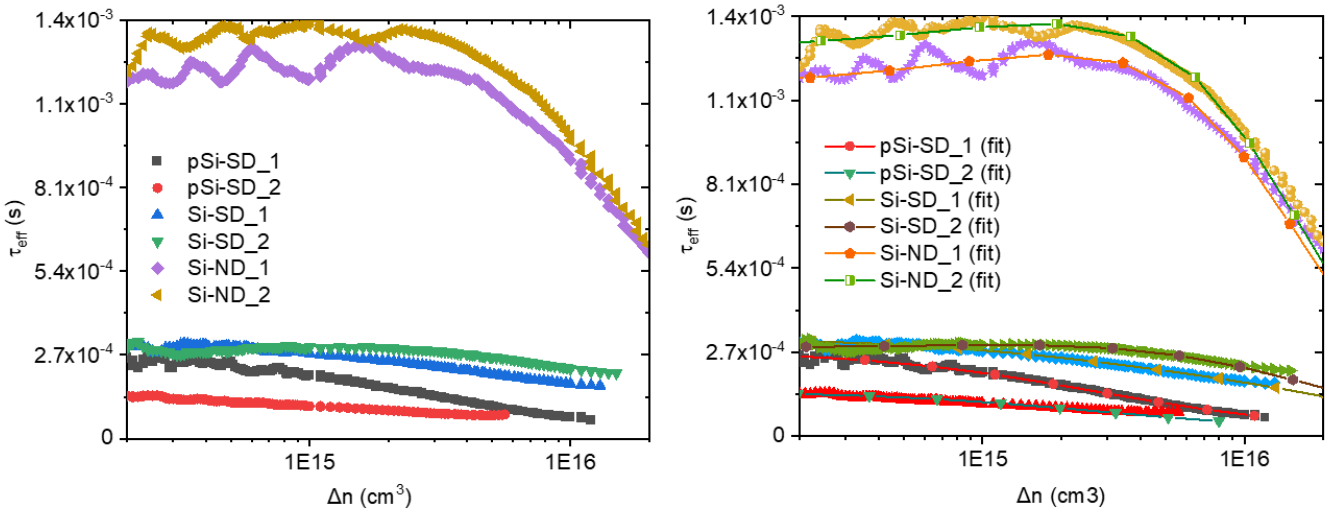


Figure 2

(a): PCD measured plots of AlO_x/SiN_x/n_poly-Si samples (pSi-SD_1 and pSi-SD_2), AlO_x/DI-O_3 oxide/Si samples (Si-SD_1 and Si-SD_2) processed by SD, and AlO_x/DI-O_3 oxide/Si samples (Si-ND_1 and Si-ND_2) by ND; and (b): measured data fitted by Quokka3.

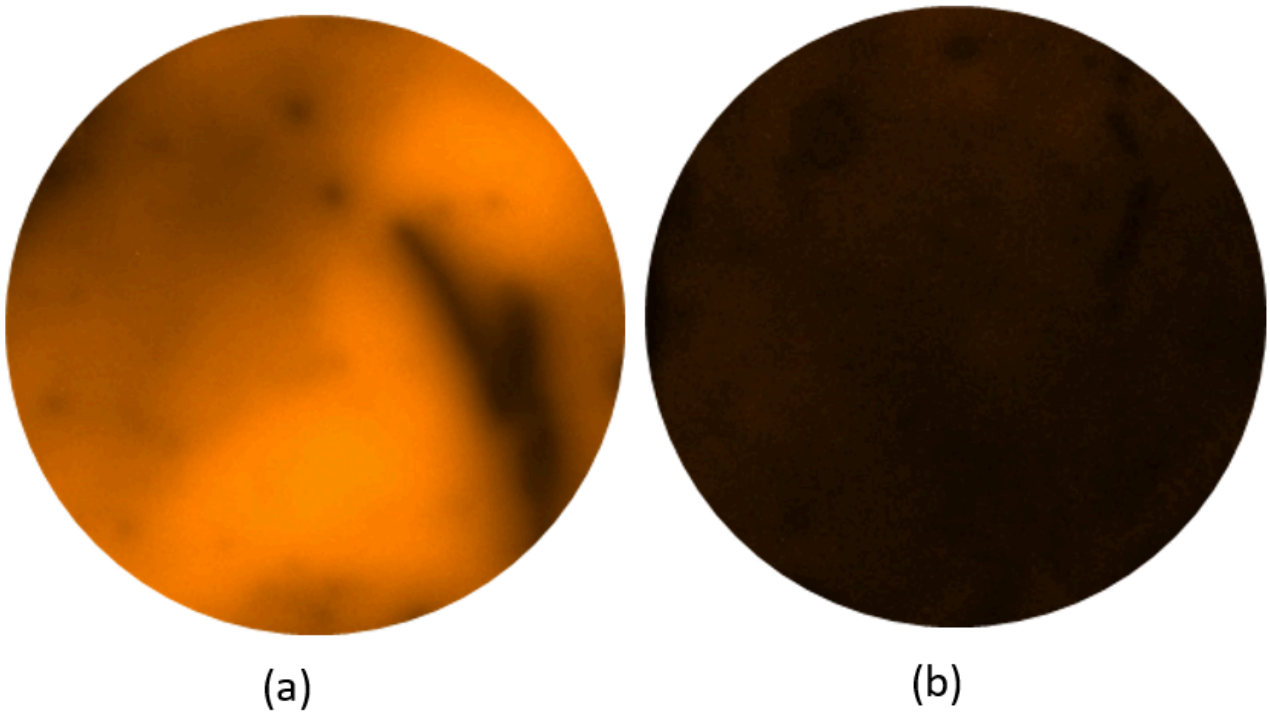


Figure 3

The uncalibrated PL images of AlO_x/DI-O_3 oxide sample processed by (a) ND and (b) SD techniques.

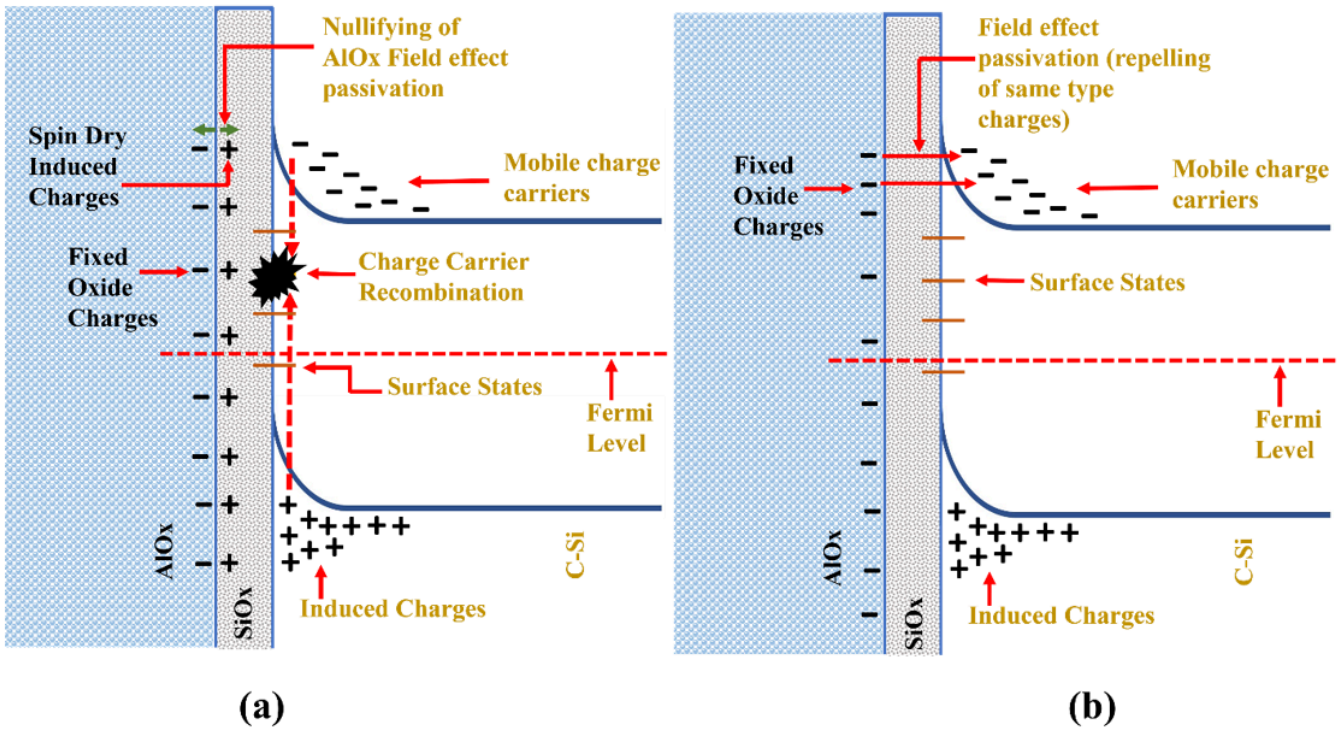


Figure 4

(a) SD induced surface charges that leads to poor surface passivation in AlO_x passivated samples (b) nullifying the effect of SD induced charges in enhanced SD process.

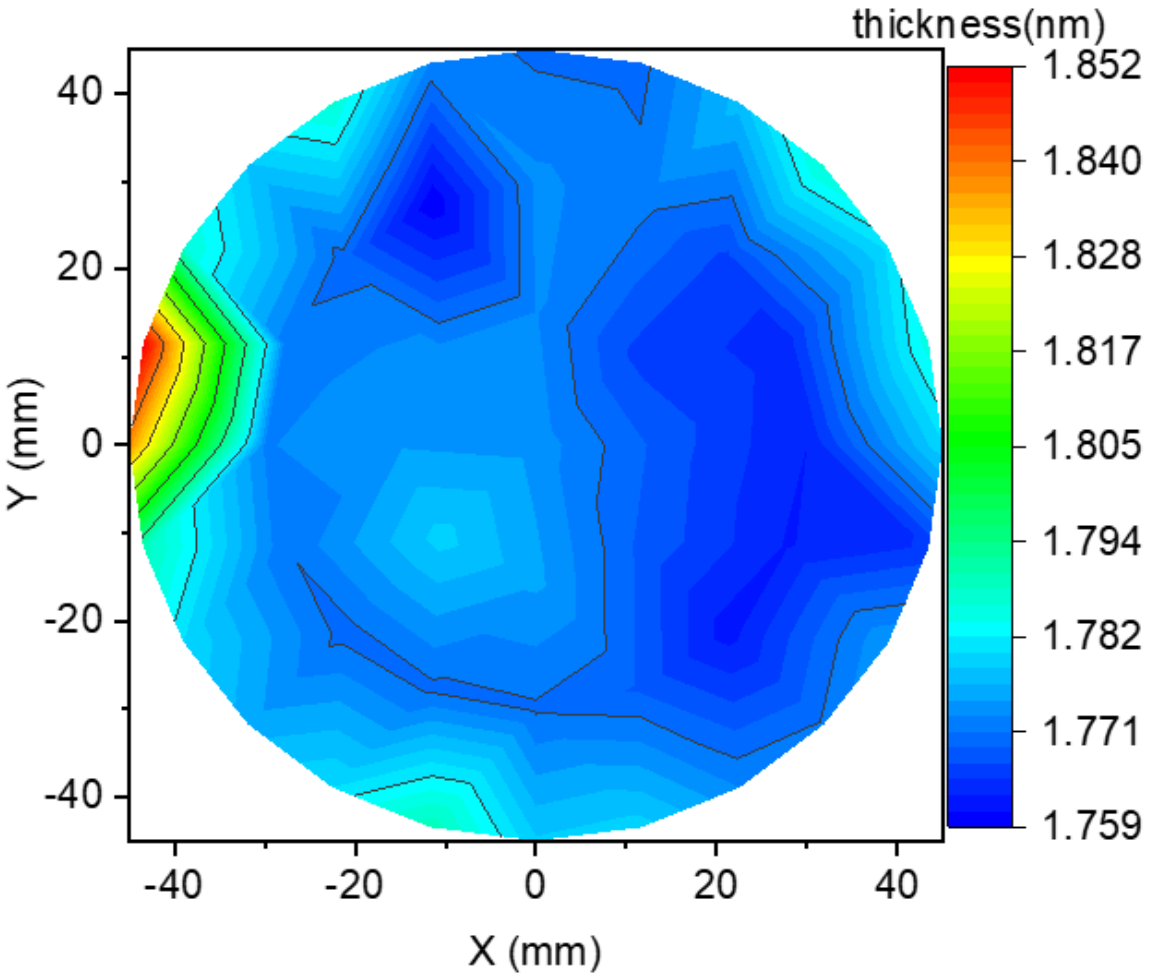
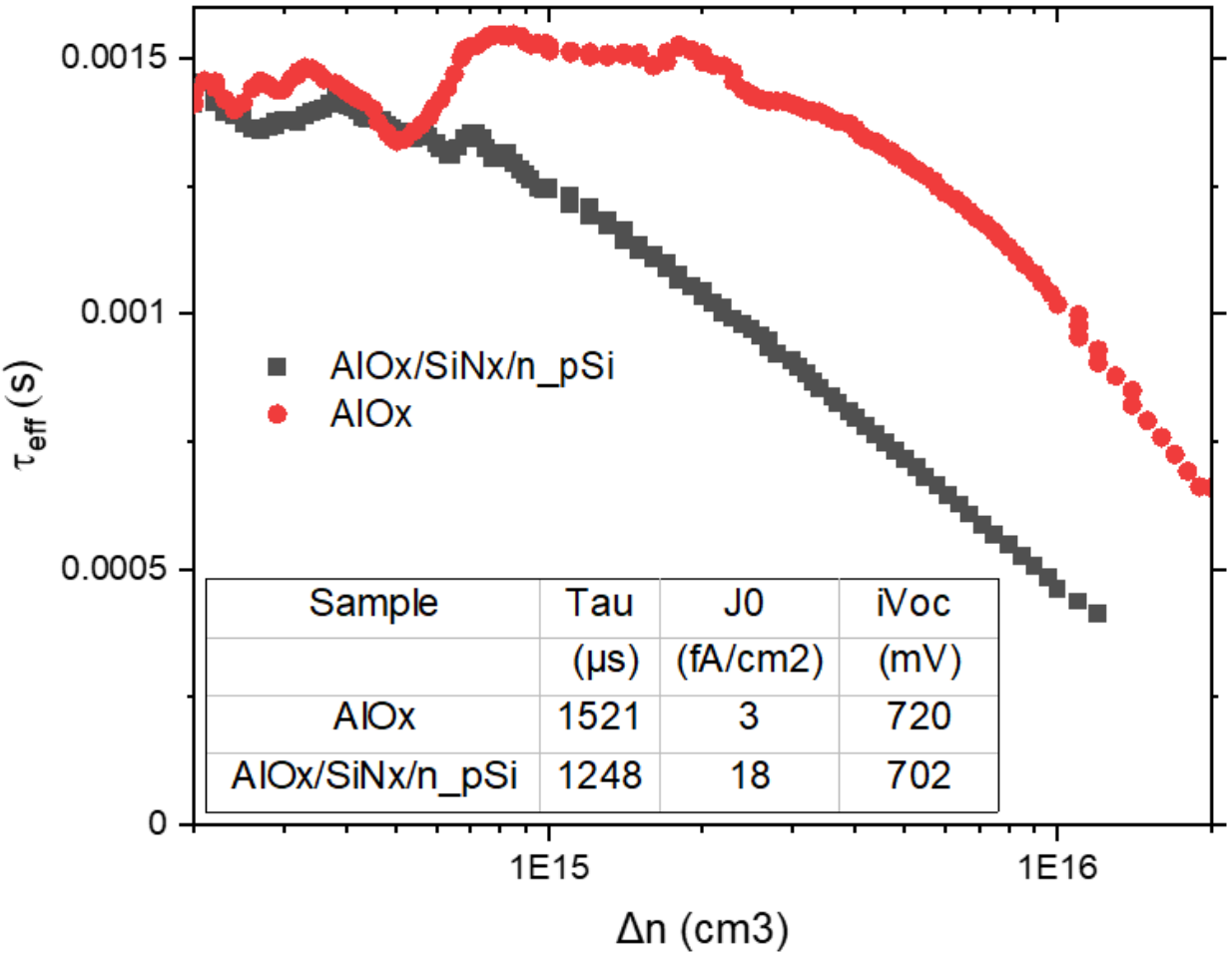


Figure 5

Ellipsometer measured contour chart of the thickness and uniformity (at 49 points) in the DIO_3 oxide grown samples with enhanced SD process.



Sample	Tau	J0	iVoc
	(µs)	(fA/cm2)	(mV)
AlOx	1521	3	720
AlOx/SiNx/n_pSi	1248	18	702

Figure 6

τ_{eff} and measured electrical parameters of n_polySi and AlO_x grown samples processed by enhanced SD technique.

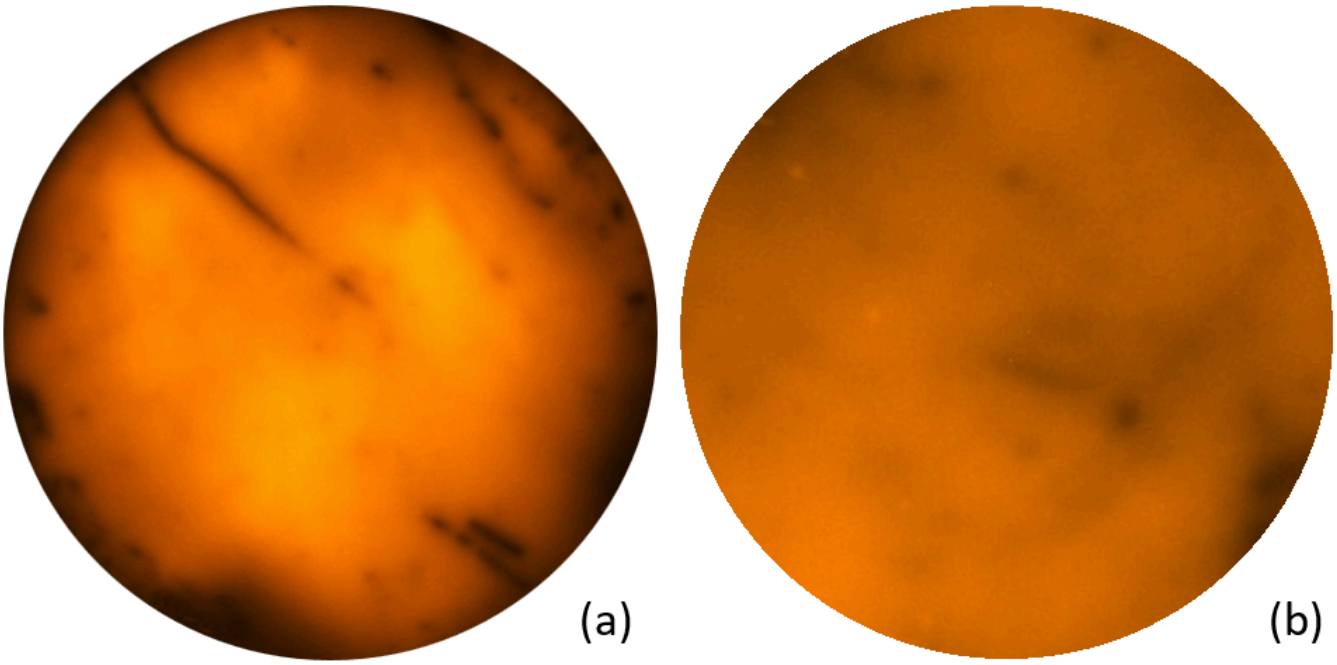


Figure 7

PL images of the (a) AlO_x and (b) AlO_x/SiN_x/n_poly-Si samples incorporating enhanced SD process.