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Evolution of Nanotechnology Using Quantum Dot Cellular Automata

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Research Article

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Evolution of Nanotechnology Using Quantum Dot Cellular Automata

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Abstract: The use of Quantum-dot Cellular Automata (QCA) has come to light as a promising nanoelectronic technology that can surpass the scaling restrictions, high power consumption and area of the Complementary Metal Oxide Semiconductor (CMOS) circuits. In this chapter, compact QCA-based combinational and sequential circuits are designed and analyzed for performance, with a particular focus on an optimized D-latch and memory architecture based on SRAM. QCA Designer 2.0.3 is used to implement and analyse fundamental QCA logic gates, multiplexers and memory structures. The single-layer QCA D-latch is realized with just 14 cells, the cell layout area 0.007 μm² and the clock latency 0.5 cycles. The proposed structure results in approximately 21% reduction of layout area as compared to the existing QCA latch design, 20% increase in operational speed and nearly 49.6% reduction in overall QCA cost when compared to the existing QCA latch design. Moreover, a new 15-cell QCA D-latch with embedded SET and RESET is suggested which consumes almost 22% less energy dissipation and has an area of 0.0048 μm² for SRAM application. A comparative study with available QCA and CMOS memory architectures shows that their compactness, power consumption, and scalability are significantly improved. The simulation results obtained confirm stable logic propagation, data reliability in memory, and efficient operation of memory devices, all of which show that QCA technology is suitable for the development of next-generation ultra-dense low power nanoelectronic systems and memories.

Keywords: *Quantum-dot Cellular Automata (QCA), Nanoelectronic Memory Circuits, QCA D-Latch, Static Random Access Memory (SRAM), Majority Gate Logic*

I. INTRODUCTION

Quantum-dot Cellular Automata (QCA) is an innovative approach within the realm of nanoelectronics, advancing the execution of different quantum designs. Unlike traditional computers, quantum arrays are created in QCA through arrangements of electron pairs that represent digital data [1]. Using these arrays, different Boolean expressions are realized within QCA software tools. The growth of QCA, along with advancements in quantum mechanical effects, enables digital circuits to achieve significant size reductions, resulting in smaller area requirements and high-speed operation at minimal power consumption. In this system, neighbouring cells interact with one another, and transition occurs due to electrostatic or magnetic influences within QCA [2]. Unlike conventional systems, which continuously vary parameters such as voltage or current to encode digital values 1 and 0, QCA uses electron localisation to represent these values within quantum dots. A huge amount of advanced and compact QCA circuits have been developed, achieving densities of up to 10^14 cells/cm², with circuit switching frequencies approaching terahertz levels. Although there are several advantages of this, such as stability, low energy consumption, compact size and high speed, the development of the Nano-electronics technology has been hampered by the absence of

advanced design techniques, efficient circuit modular designs, and execution and fabrication for each application. Being low power consumption, compact and fast, QCA has become popular among a lot of research scholars for implementing different digital circuits and topologies. Basic logic gates are the building blocks of any digital circuit and are designed in the first part of this work. The most repetitively used component in a digital circuit or processor is a latch. The latch is used to make circuits like flip-flops, shift registers, and memory cell architectures. The fundamental device used for the temporary storage of data within a digital system is called a Data Latch (D Latch) or a level-triggered system. This circuit serves the purpose of storing and managing binary data [4]. By employing this storage device, one can realize various intricate digital circuits and a memory unit. In the current designs of QCA Data-Latches, which rely on multiplexer structures that incorporate multiple majority gates and inverters, the proposed design introduces a single 3-input majority gate with a feedback loop to establish a majority-feedback structure. This approach eliminates the need for an inverter and necessitates a 14-cell configuration. Consequently, the area, delay, and QCA cost are diminished, rendering the structure more appropriate for assured QCA implementations. The innovation of this proposed work lies in a majority-feedback-based QCA D-latch architecture that substitutes the conventional MUX-inverter structures, resulting in enhancements in output, QCA cost, clock delay, energy dissipation, and cell area. The basic functional unit of a QCA cell having four quantum dots placed in square shaped box at four individual corners. Each cell contains two electrons, which are placed diagonally opposite side to each other because of Coulombic interaction, as shown in Figure 1, Logic One and Logic Zero [5].When electrons are placed diagonally on right hand side in QCA cell then it is considered as Logic “1” and when electrons are placed on diagonally left-hand side of cell then it is considered as Logic “0” [6]. Figure 2 shows the Input and Output cell, whereas Figure 3 shows different arrangements of cells, such as crossover cell, normal cell, and vertical cell.

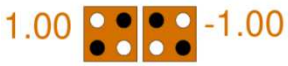


Figure 1. Polarization States Of A Quantum-Dot Cellular Automata (Qca) Cell Representing Binary Logic ‘1’ And Logic ‘0’ Based On Electron Localization



Figure 2. Basic input and output qca cells illustrating binary signal propagation through cell polarization

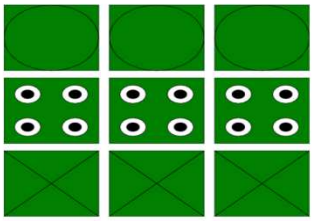


Figure 3. Different Qca Cell Arrangements Used In Circuit Implementation, Including Crossover, Normal, And Vertical Cell Structures

Table 1 provides a detailed comparison to recently published QCA-based latch and SRAM architectures. It suggests that the proposing 14-cell QCA D-latch has less area for use and less clock latency than previous designs. Moreover, the proposed SRAM-oriented latch with integrated SET and RESET function has been implemented in an energy efficient manner and with a reduced size, while ensuring sequential operation.

Table 1. Comparative Analysis of Recent QCA-Based D-Latch and SRAM Architectures

Ref.	Year	Design Type	Technology	Cell Count	Area (μm²)	Clock Latency	Energy Efficiency	Key Contribution

[12]	2021	QCA D-Latch	QCA	24	0.015	1.0 cycle	Moderate	Basic latch structure using majority gates
[13]	2021	QCA SRAM Cell	QCA	30	0.021	1.5 cycles	Moderate	Loop-based SRAM architecture
[14]	2022	Compact D-Latch	QCA	21	0.011	1.0 cycle	Improved	Reduced area through optimized layout
[15]	2022	Edge-Triggered D Flip-Flop	QCA	35	0.028	1.5 cycles	Moderate	Sequential memory implementation
[16]	2023	Low-Power SRAM	QCA	28	0.019	1.0 cycle	High	Reduced power dissipation architecture
[17]	2023	Fault-Tolerant D-Latch	QCA	32	0.024	1.5 cycles	Moderate	Improved reliability under cell defects
[18]	2024	Single-Layer QCA Latch	QCA	19	0.009	0.75 cycle	High	Compact coplanar implementation
[19]	2024	Energy-Efficient SRAM	QCA	26	0.016	1.0 cycle	Very High	Optimized clocking and energy reduction
[20]	2025	Majority Gate Based D-Latch	QCA	18	0.008	0.75 cycle	High	Reduced majority gate utilization
Proposed Work	2026	Proposed QCA D-Latch	QCA	14	0.007	0.5 cycle	Very High	Compact low-latency latch design
Proposed Work	2026	Proposed SRAM-Oriented D-Latch	QCA	15	0.0048	0.5 cycle	Very High	Integrated SET/RESET SRAM functionality

II. QUANTUM GATES

The majority gate and inverter are very important gates in QCA technology implementation to design any logic circuit. To design a Majority gate five QCA cells are used as shown in Figure 4a. It Consist of total five cells out of which 3 are input cells, middle cell is called as driver cell and last is output cell [7]. The output of majority gate depends on applied majority inputs. For example, if input is applied as “011” then it produces output as “1” and if input is applied as “010” then it produces output as “0” which represents maximum digit repetition in input as shown in Figure 4b. It is possible to build NOT gate using QCA cell. Figure 4c shows the inverter gate; if the input is “1” then it produces output “0” and vice versa.

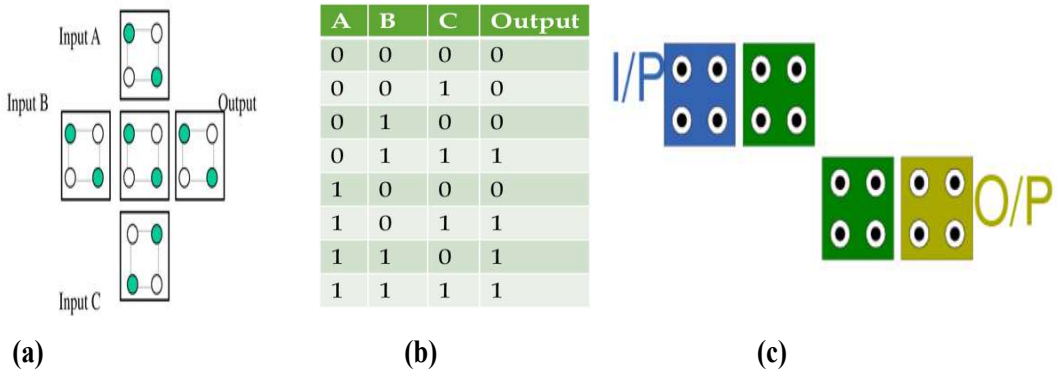


Figure 4. Fundamental QCA logic structures: (a) three-input majority gate configuration, (b) truth table of the majority gate, and (c) QCA inverter structure.

In order to synchronize and control the flow of information, as well as provide power to energize the circuits, a clock is needed for each QCA circuit design [8]. For the tunnelling, clock signals are used in the QCA computations that are basically divided into 4 zones. By adjusting the potential barriers between adjacent dots present in quantum cells, the clocking mechanism in QCA can be achieved. Clock pulses are necessary for QCA circuits to function. This is a QCA technology clocking mechanism is shown in Figure 6. The QCA clocking will be broken down into four categories: relax, release, hold, and switch. The starting point for the switch process is random QCA cells that have low energy to move between the two regions. However, as the phase proceeds the hurdles get tougher [9]. The barriers are kept up high throughout the hold period. But in the release phase, challenges are decreased. The minimum maintenance of the barriers at the end (relax) keeps the cells unpolarized. A QCA wire operates in the following manner: it works in separate clock phases as shown in Figure 5 and the inter-dot barrier is a partition within a clocking phase. The barriers separating the dots are slowly raised during the switch phase, and the cell in QCA stabilizes in one of its two possible polarization states, that depends on the polarization of the neighbouring cells [10]. The interdot barrier stays high in the hold phase, blocking electron tunnelling and maintaining the QCA cell's existing polarization state. In the 2nd and 3rd zone that is release and relaxation, respectively, the obstacles are reduced, enabling increased electron mobility. During these zones, the QCA cell remains unpolarized.

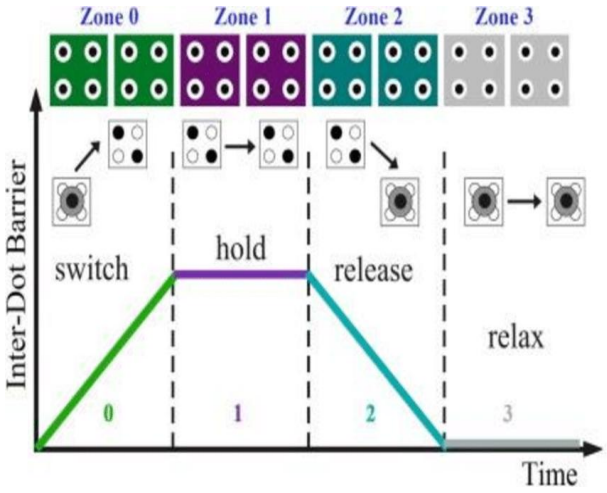


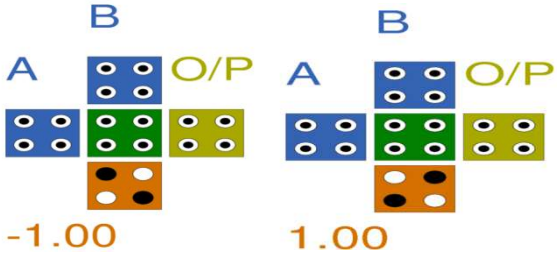
Figure 5. Four-phase QCA clocking mechanism showing switch, hold, release, and relax states for controlled information propagation.

The cell's polarization is determined during the switch zone, influenced by the polarization states of neighbouring cells that are in either the switch or hold zones. Unpolarized neighbours in the release and

relax phases do not affect the state of a QCA cell. Clock signals—generated by an induced electric field—can be created using CMOS wires positioned beneath the QCA layer.

A. BASIC LOGIC GATE DESIGN

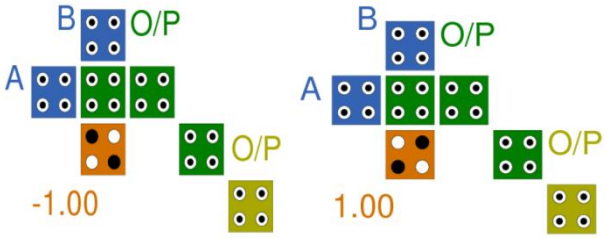
Two QCA cells can be positioned 45 degrees apart such that they interact inversely to implement the inverter or NOT gate using QCAD. The NOT gate is implemented by using the QCAD software tool [11]. In the majority gate illustrated in Figure 4a, an AND gate is formed by setting one input to zero (with a polarization of -1). The opposite is to set one input of the majority gate to one (+1 polarization) which is called an OR gate. To design a NAND gate by adding an inverter to the AND gate's output and NOR gate, which is implemented by adding an inverter at the output of the OR Gate [12]. AND Gate is shown in figure 6a and OR Gate is shown in figure 6b.



(a) **(b)**

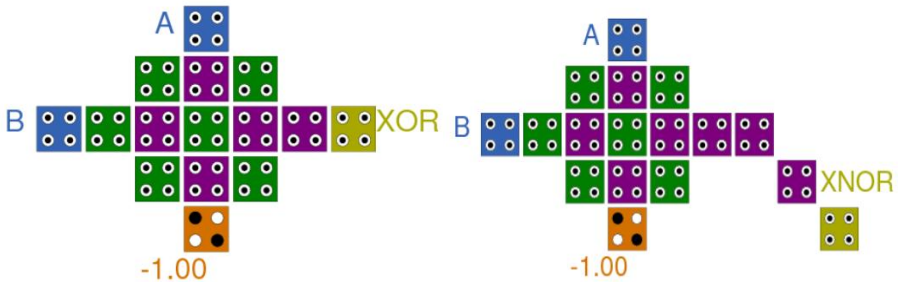
Figure 6. QCA implementation of basic combinational logic gates: (a) AND gate using majority logic and (b) OR gate using majority logic.

Figure 7a illustrates how to create a NAND gate by adding an inverter to the AND gate's output. Figure 7b shows a NOR gate, which is implemented by adding an inverter at the output of the OR Gate [13].



(a) **(b)**

Figure 7. QCA realization of universal logic gates: (a) NAND gate and (b) NOR gate using majority gate and inverter combinations.



(a) **(b)**

Figure 8. QCA-based exclusive logic circuits: (a) XOR gate and (b) XNOR gate implemented using compact cell arrangements.

For XOR gate design, no wire crossing is used, and it has only 14 cells. A majority gate, along with 2 clocking zones (Zone 0 & Zone 1), is used for the execution of the XOR gate. An XNOR gate can be executed by simply adding an inverter at the output of the XOR gate. Figure 8a shows the XOR Gate and Figure 8b shows the XNOR Gate [14]. When it comes to managing numerous circuits or memory units at once, a multiplexer is an extremely crucial component in the field of digital electronics in the design of an FPGA. A multiplexer is a combinational digital circuit that has multiple data inputs and one or more selection lines. The select inputs determine which one of the data inputs is connected to the output. Thus, only one input signal is chosen and transmitted to the output at a time. Typically, it has two input lines and select lines that are plugged in, from which one output is pulled. A digital logic circuit known as a 2:1 multiplexer is connected to two inputs and one select line, which is logic-set to choose the input line. As a result, the chosen line determines the output that is pulled from the specified logic circuit and calculated as shown in equation no.1. Two AND gates and one OR gate make up a simple 2:1 multiplexer architecture that satisfies the following logic [15]:

$$Output = a.S' + b.S \tag{1}$$

Here to design 2:1 Mux, a majority gate is used and achieved reduced cell count, smaller area using 9 cells as shown in Figure 9 [16].

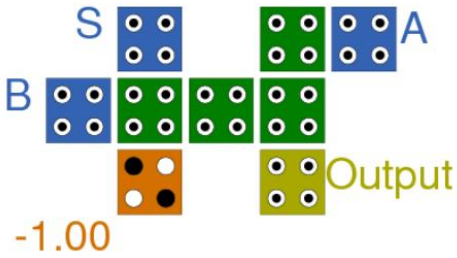


Figure 9. Compact 2:1 multiplexer implementation using QCA majority gate logic with reduced cell count and minimized layout area.

By using the cascaded combination of 2:1 Mux a 4:1 Mux is designed in Figure 10. The output is fully depends on select lines. For the given 4:1 Mux the clock zone is acting as a select lines. In your waveform simulation:

- When Clock 1 = 0 and Clock 0 = 0 → Output should follow A.
- When Clock 1 = 0 and Clock 0 = 1 → Output should follow B.
- When Clock 1 = 1 and Clock 0 = 0 → Output should follow C.
- When Clock 1 = 1 and Clock 0 = 1 → Output should follow D.

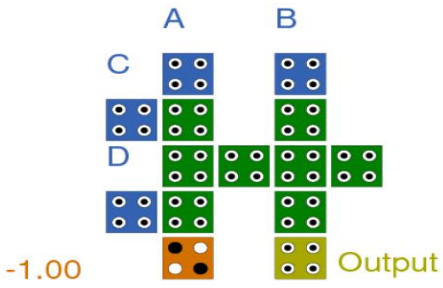
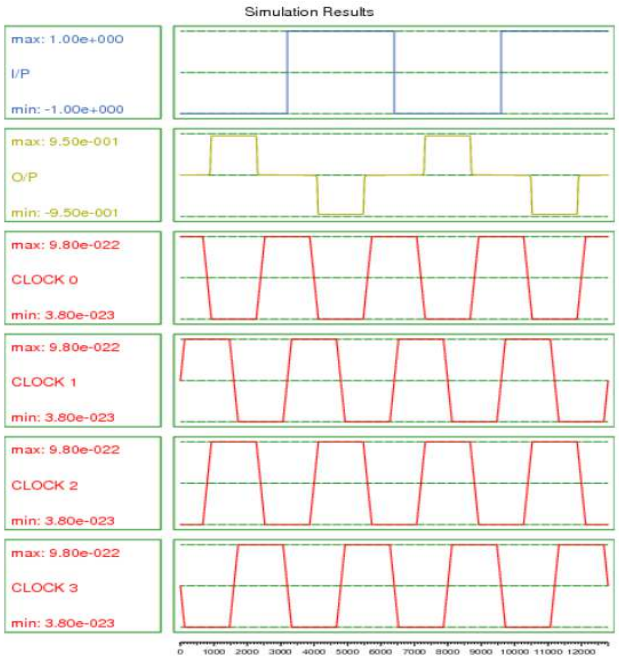


Figure 10. QCA-based 4:1 multiplexer architecture constructed using cascaded 2:1 multiplexer modules

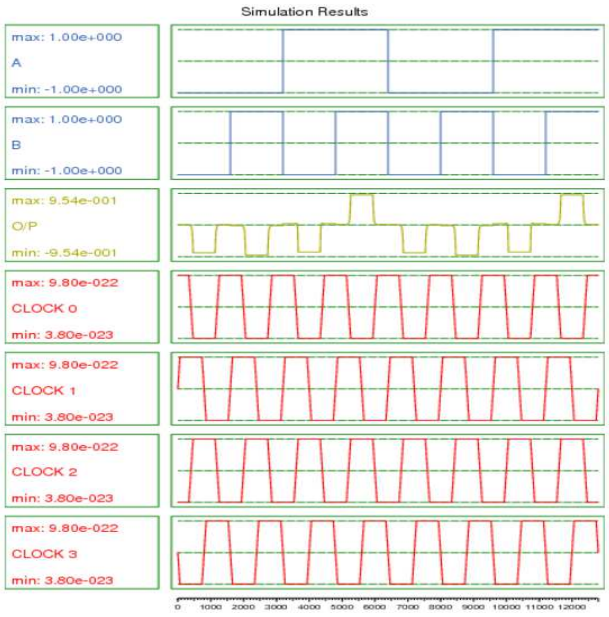
In all combinational circuit output depends on the present input, with no need of memeory cell, which makes the combinational circuit faster and simple as compare to a sequential circuit. For a sequential circuit, the output depends on present as well as past input which are stored in a memory cell, so for a sequential circuit, memory plays a vital role.



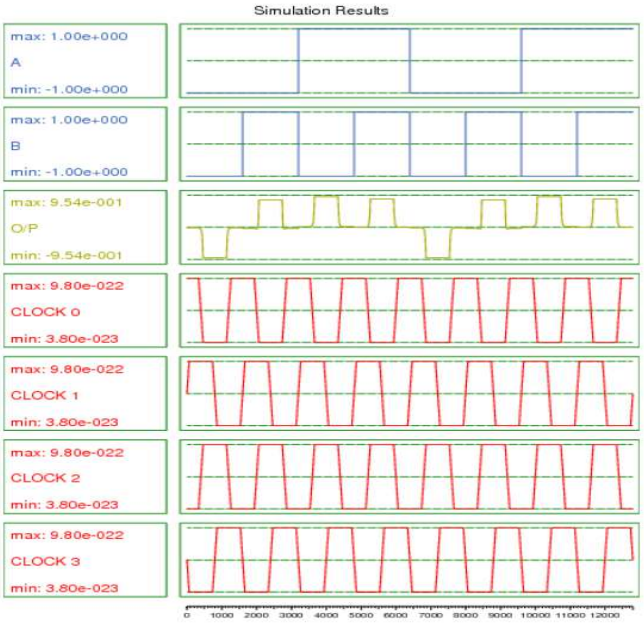
(a)



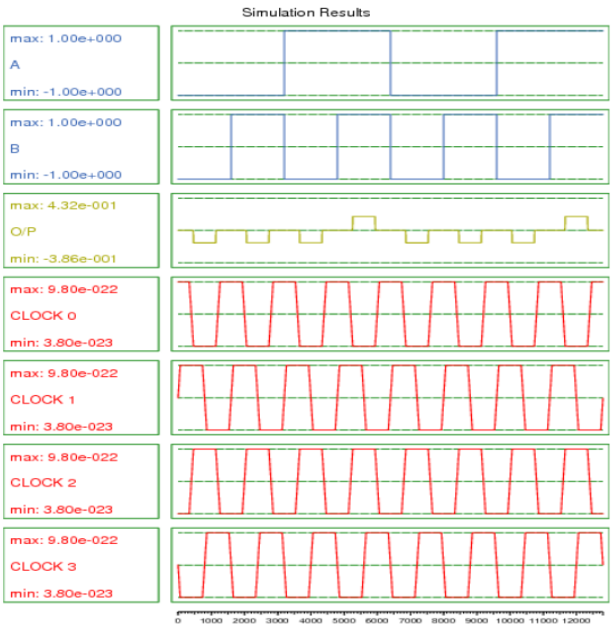
(b)



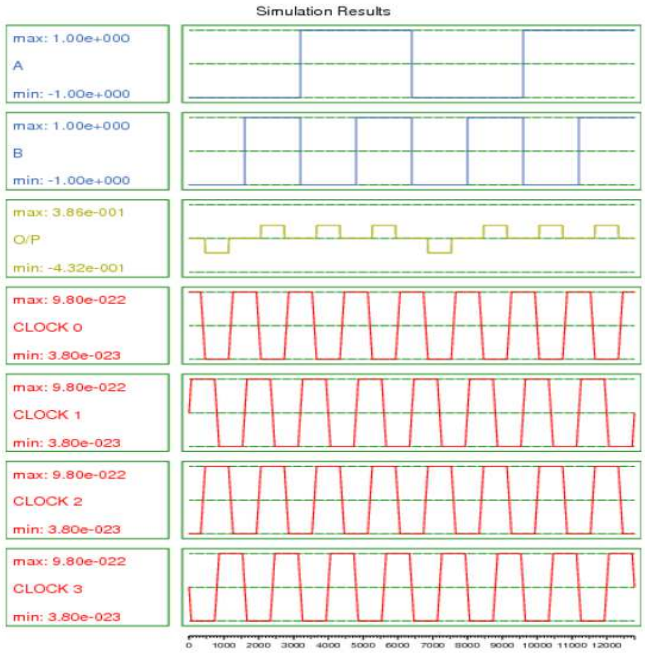
(c)



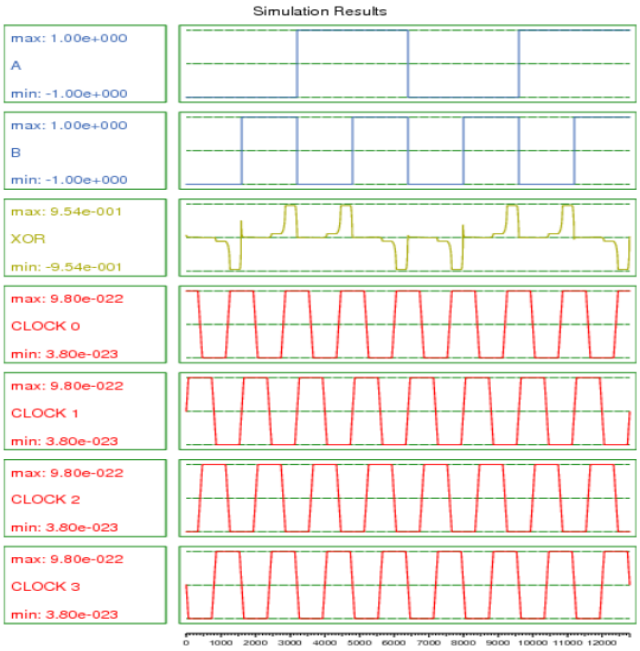
(d)


Simulation Results
max: 1.00e+000
A
min: -1.00e+000
max: 1.00e+000
B
min: -1.00e+000
max: 4.32e-001
O/P
min: -3.86e-001
max: 9.80e-022
CLOCK 0
min: 3.80e-023
max: 9.80e-022
CLOCK 1
min: 3.80e-023
max: 9.80e-022
CLOCK 2
min: 3.80e-023
max: 9.80e-022
CLOCK 3
min: 3.80e-023
0 1000 2000 3000 4000 5000 6000 7000 8000 9000 10000 11000 12000

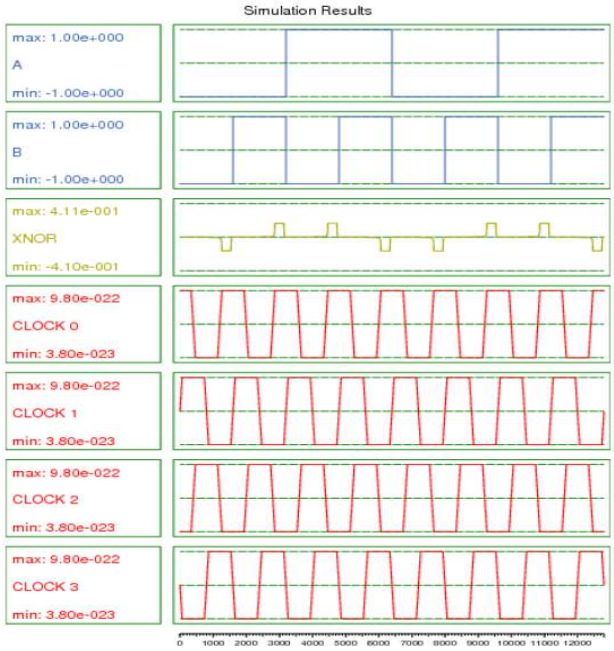
(e)


Simulation Results
max: 1.00e+000
A
min: -1.00e+000
max: 1.00e+000
B
min: -1.00e+000
max: 3.86e-001
O/P
min: -4.32e-001
max: 9.80e-022
CLOCK 0
min: 3.80e-023
max: 9.80e-022
CLOCK 1
min: 3.80e-023
max: 9.80e-022
CLOCK 2
min: 3.80e-023
max: 9.80e-022
CLOCK 3
min: 3.80e-023
0 1000 2000 3000 4000 5000 6000 7000 8000 9000 10000 11000 12000

(f)


Simulation Results
max: 1.00e+000
A
min: -1.00e+000
max: 1.00e+000
B
min: -1.00e+000
max: 9.54e-001
XOR
min: -9.54e-001
max: 9.80e-022
CLOCK 0
min: 3.80e-023
max: 9.80e-022
CLOCK 1
min: 3.80e-023
max: 9.80e-022
CLOCK 2
min: 3.80e-023
max: 9.80e-022
CLOCK 3
min: 3.80e-023
0 1000 2000 3000 4000 5000 6000 7000 8000 9000 10000 11000 12000

(g)


Simulation Results
max: 1.00e+000
A
min: -1.00e+000
max: 1.00e+000
B
min: -1.00e+000
max: 4.11e-001
XNOR
min: -4.10e-001
max: 9.80e-022
CLOCK 0
min: 3.80e-023
max: 9.80e-022
CLOCK 1
min: 3.80e-023
max: 9.80e-022
CLOCK 2
min: 3.80e-023
max: 9.80e-022
CLOCK 3
min: 3.80e-023
0 1000 2000 3000 4000 5000 6000 7000 8000 9000 10000 11000 12000

(h)



(i) **(j)**

Figure 11. Simulation waveforms of QCA logic circuits: (a) majority gate, (b) inverter, (c) AND gate, (d) OR gate, (e) NAND gate, (f) NOR gate, (g) XOR gate, (h) XNOR gate, (i) 2:1 multiplexer, and (j) 4:1 multiplexer.

Figure 11 presents the simulation waveforms and functional verification results of the implemented QCA combinational logic circuits, including majority gate, inverter, AND, OR, NAND, NOR, XOR, XNOR, 2:1 multiplexer, and 4:1 multiplexer. The obtained waveforms confirm correct logic propagation, signal synchronization, and accurate operation of the proposed QCA-based circuit designs. Table 2 shows the comparative analysis of area based on QCA and CMOS of gates NOT, AND, OR, NAND, NOR, XNOR and XOR. The graphical representation of the comparison of QCA and traditional CMOS technology, depending on their gate area, is shown in Figure 12, which illustrates the significant physical footprint reduction made possible by QCA technology. The comparison shows that QCA gates routinely take up 97–99% less space than their CMOS equivalents: NOT gate: 97.2% decrease, AND/OR gates: reduction of 98.9%, NAND gate: reduction of 98.0%, NOR gate: reduction of 98.1%, XOR gate: reduction of 97.4%, XNOR gate: reduction of 97.1%.To calculate the area in μm^2 for each gate requires the total number of cells used to design that particular gate and the area per cell [17]. The formula shown in Equation (2) is used to calculate the area in μm^2.

$$Area\ gate = No.of\ Cells \times Area\ per\ Cell \tag{2}$$

Table 2: Comparative analysis of Gate Area

Parameter	NOT	AND	OR	NAND	NOR	XNOR	XOR
No. of Cells in QCA	4	5	5	8	8	16	14
Area(um^2) Area per Cell=0.04µm2	0.16	0.20	0.20	0.32	0.32	0.64	0.56
Area in CMOS (90nm)	5.8	17.7	17.9	16.3	16.5	21.7	21.6

Across all fundamental logic gates, QCA typically achieves area savings of about 98%. The potential of QCA for ultra-dense circuit integration, lower interconnect complexity, and scalable memory design is highlighted by its exceptional compactness. The figure unequivocally shows that QCA technology is an excellent option for post-CMOS nanoelectronics architectures since it can provide an area efficiency improvement of orders of magnitude when compared to traditional CMOS.

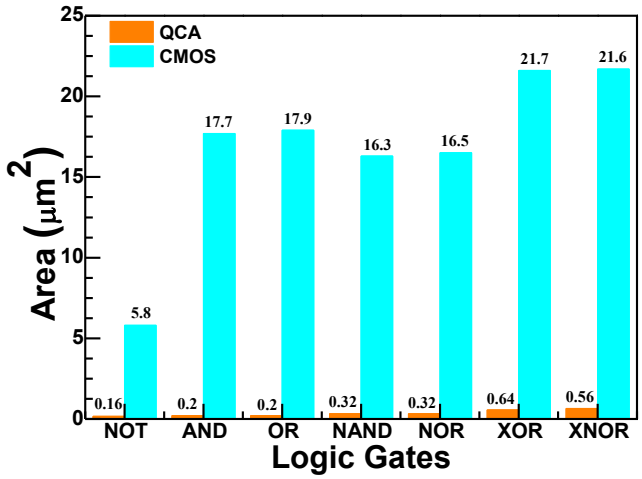


Figure 12. Comparative analysis of circuit area occupied by QCA and CMOS logic gates demonstrating significant area reduction achieved using QCA technology.

QCA Memory Cell Architecture:

In the case of QCA technology memory implementation, the memory is to be in constant motion. The memory cells are linked in a circle; the memory is expected to flow in a continuous motion between these cells. The loop is separated into all four clock zones to store information presented in Figure 13. A serial or parallel process can be utilized as a memory architecture [18]. In QCA technology, memory design to maintain memory in motion has two architectural methods, namely line-based and loop-based, illustrated in Figure 13. It is reviewed that how data flow is preserved, clocking used and several memory cells operated based on line in Figure 13a and loop-based architectural style in Figure 13b.

Line Based Approch:

Within Quantum-dot Cellular Automata (QCA), memory circuits may be built based on several architectures one being In Quantum-dot Cellular Automata (QCA), the line-based memory approach is an alternate method of storing data in memory circuits [19]. In this technique, the data is saved in a linear chain (line) of QCA cells as opposed to a feedback loop. The data stored is preserved by regulating the clocking areas of the QCA cells that ensure that the polarization of the cells remains constant over a given duration of time. In a line based memory, the data being fed in passes through a sequence of QCA cells lying in a straight line. In a state with the write signal enabled, the value of the input (0 or 1) is transmitted and stored along the line. The polarization that is stored is replicated to the output during the read operation using the same cell line but it does not alter the stored value. The clocking mechanism makes sure that the data does not change until some other value is written in the memory cell. The benefits of the line-based strategy are easier layout, the ability to scale, as well as circuit complexity is less than that of loop-based memory designs. Nevertheless, the stored data might be less stable in the

long-term periods, and clock zone synchronization becomes a concern in order to have a good functioning. The line characteristics have led to the application of line-based memory in simple QCA memory structures and small memory blocks.

Loop-Based Approach:

In Quantum-dot Cellular Automata (QCA), memory circuits might be realized through various architectures, one of which is the loop-based memory approach. In this technique, the data is stored by connecting a feedback of QCA cells in a way that the circuit output is fed back into the circuit input. This feedback loop ensures that the polarisation state of the QCA cells is maintained, so that the circuit is capable of retaining the binary value (0 or 1) stored within it even in the absence of any new input. Majority gates, inverters or multiplexers are some of the components that are usually employed in a loop-based memory cell in order to regulate the flow of information. As the write signal is turned on, the value of the input is stored in the loop [20]. When the read signal is actuated, the stored value is sent to the output, leaving no change in the stored data. The feedback loop is used to guarantee that the stored information flows inside the QCA cells and stabilises because of the electrostatic forces between the adjacent cells. The key benefits of the loop-based memory model are straightforward design, consistent data storage, and straightforward implementation of single-bit memory cells. Nonetheless, it might need additional clock steps, and the number of cells and this aspect may complicate the circuit design of smaller memory arrays. Consequently, this is why scholars tend to investigate the optimal loop designs to enhance the area efficiency, latency, and power consumption of QCA memory circuits.

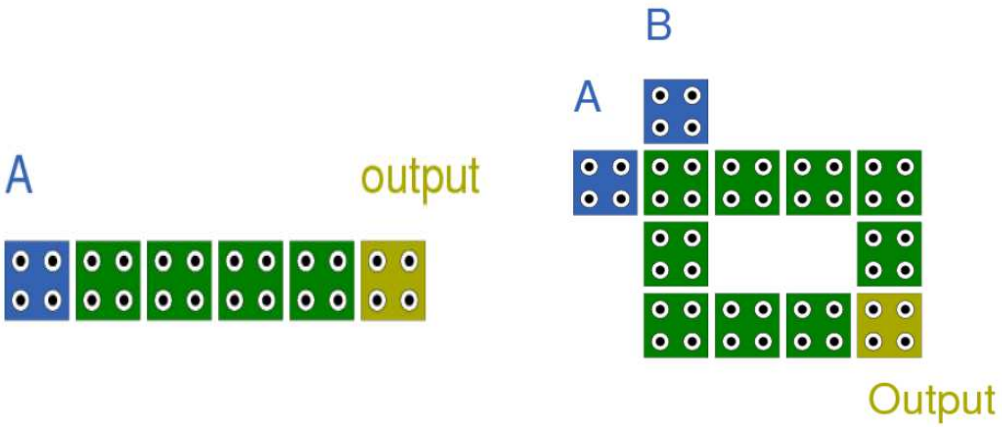


Figure 13. QCA memory architectures: (a) line-based memory structure and (b) loop-based memory structure for data storage applications.

QCA Layout Factors:

1. Cell Count: The overall number of QCA cells utilized for the implementation of a logic circuit is called the cell count. A minimum cell count is required to represent any circuit for a simple fabrication process [21].

2. Cell size: The physical dimensions of a single QCA cell are called cell size. It is typically measured in nanometers (nm), representing the distance between outermost quantum dots in a cell.

3. Total area: The total area depends on cell size, distance between adjacent cells, total cells and how the cells are arranged. A lower total area means a more compact, efficient, and cost-effective QCA design [22].

4. Latency: The total time delay experienced by a signal to travel from the input to the output of a QCA device. It depends on the number of clock zones the signal passes through and the clock frequency.
5. QCA cost: A combined performance metric that evaluates the overall efficiency of the QCA circuit in terms of its area, latency and cell count. QCA cost provides a single Figure of Merit (FOM) that reflects the trade-off between area, latency and cell count [23].

6. Energy Dissipation: Total amount of energy lost or consumed when QCA cells switch their polarization states during information transfer is called as energy dissipation.

7. Kink Energy: The electrostatic interaction energy between two adjacent QCA cells when their polarizations are opposite [24].

Table 3 shows the default simulation parameters of the QCAD software tool for better understanding. The QCAD designer tool is used for simulation analysis of basic Boolean functions of logic gates [25].

Table 3: Default Simulation Parameters of QCAD

Parameter	Values
Clock High	9.800000e-022 J
Clock Amplitude Factor	2.000000
Clock Low	3.8000000e-023 J
Clock Shift	0
Radius of Effect	65.000000nm
Layer Separation	11.500000
Cell Size	18 nm
Number of Samples	50.000
Relative Permittivity	12.900000
Convergence tolerance	0.0000100
Maximum Iterations per sample	100

It is a vital tool for QCA research, aiding the development of low-power, high-speed, nano-electronic circuits. QCAD is the result of a continuous initiative aimed at developing a quick and precise simulation and layout technique for quantum-dot cellular automata (QCA). QCAD software can simulate intricate QCA circuits on a majority of standard platforms. It is user-friendly interface for placing QCA cells and designing logic circuits and implements clock zones for accurate timing analysis.

III. PROPOSED DESIGN OF D LATCH:

The basic device used to store temporary information in digital systems is called a data latch or a level-triggered system. By using this storage device, one can implement other digital circuits [26]. This circuit is used to store and manage binary data. By using this storage device, one can implement various complex digital circuits and a memory unit. In the existing QCA Data-Latch designs, which are based on multiplexer structures implemented with the help of multiple majority gates and inverters, the proposed design uses a single 3-input majority gate and an inverter, making the circuit simple and compact in size. This study removes the complex multiplexer and makes a 14-cell requirement for this implementation, reducing the area, delay and QCA cost, and the structure is made more suitable for guaranteed QCA implementations.

Previously published QCA designs are more expensive and difficult to execute due to a number of issues, such as a bigger cell count, a very large circuit layout, a longer clock cycle delay, and more sophisticated gates. The Data latch circuit presented in [27] utilizes 35 cells, and it is designed using 3-input majority gates and an inverter. The total area occupied by this device is 0.04μm² and uses all four clock zones. The

Data latch circuit used in [28] uses 19 cells, and it is a combination of a majority gate, a multiplexer and an inverter. This device occupies an area of 0.01µm² and uses three clock zones. The Data latch device shown in [29] utilizes 18 cells, and it is designed using a 2:1 Mux. The total area of this device is 0.01µm² and uses two clock zones.

On the other hand, a more effective and compact solution is provided by the optimized QCA Data latch design that is suggested in the current research, which shows notable advancement in terms of decreased cells, minimal clock latency, smaller circuit area, and lower total QCA cost. The proposed Data Latch device implemented by utilizing a majority gate and an inverter is presented in Figure 14.

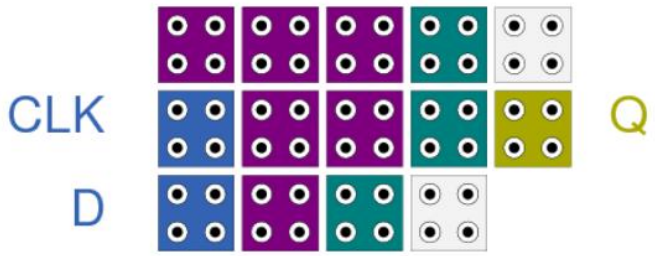


Figure 14. Proposed compact single-layer QCA D-latch architecture implemented using majority gate and inverter logic.

The proposed Data latch design is implemented by using Majority gates and an inverter. The total cell count required is 14 cells with a 0.0074 μm^2 layout area and 0.4 clock delay. The Data Latch is a level-triggered device: when CLK is high (1), Q follows the value of D; when CLK is low (0), Q holds the previous value of D. Table 4 shows the functionality of the Data Latch [30].

Table 4: Functionality of Data Latch

CLK	D	Q	Comment
0	X (don't care)	Q holds the previous value	Hold Condition
1	0	0	Transparent Condition
1	1	1	

When the clock is high (CLK=1), the input value is transferred to the output, i.e., Output Q shows the value of input (D). When the clock is low (CLK=0), the output holds the previous value of the input. Table 5 shows a comparison between the existing Data Latch and the Proposed Data Latch design.

Table 5: The Comparison of The Prior and Newly Designed Data Latch Device

Data latch	Cell count	Total area (A) (µm²)	Clock delay (T)	QCA cost	MG	NM	LT
[27]	35	0.04	1.00	5.00	NA	4	Single
[28]	19	0.01	0.75	1.50	3	NA	Single
[29]	18	0.01	0.50	1.00	1	1	Single
Proposed D Latch	**14**	**0.007**	**0.5**	**0.001**	**1**	**NA**	**Single**

Please note: MG-Majority Gate, NM- Number of Mux and LT- Layer Type

IV. Performance Evaluation and Result:

The advanced Data latch is recreated with the help of QCA Designer version 2.0.3. The simulation parameters and conditions of the QCA Designer tool. The predetermined values are used for configuring the system. Table 1 of this study reports the simulation parameters used. A single QCA cell has fixed dimensions of 18 × 18 nm^2, two electrons that are free to move according to the Coulomb repulsion force, and quantum dots with a diameter of 5 nm [31]. A Data latch circuit is made up of the data (D), clock (CLK) and one output (OUT) value. The output value is the same as the prior value if the clock (CLK) is logic 0, and if the output cell receives the logic state of data (D), and the clock (CLK) is logic 1. The functionality of the suggested QCA Data latch device and existing current QCA Data latch circuits are compared in Table 3. We take into account the crucial comparative metrics, including the layout area, clock latency, QCA cell counts, and QCA cost. These elements are essential for making an informed choice and guaranteeing the benefit of our research. The proposed Data latch circuit shows greater efficiency with respect to the prior Data latch circuit design. The proposed Data latch circuit uses 14 cells having 0.007μm² layout area. The proposed design has a 0.75 clock cycle. To calculate the QCA cost, the following Equation (3) is used

$$QCA\ Cost = (Mk + I + Cl) * Tp \tag{3}$$

where M stands for the majority logic gate, I for the inverter, C for the layer, and T for the clock delay. Exponential powers are k, l, and p. The proposed D-latch circuit's QCA cost is 0.001.

A. Simulation Results of D Latch:

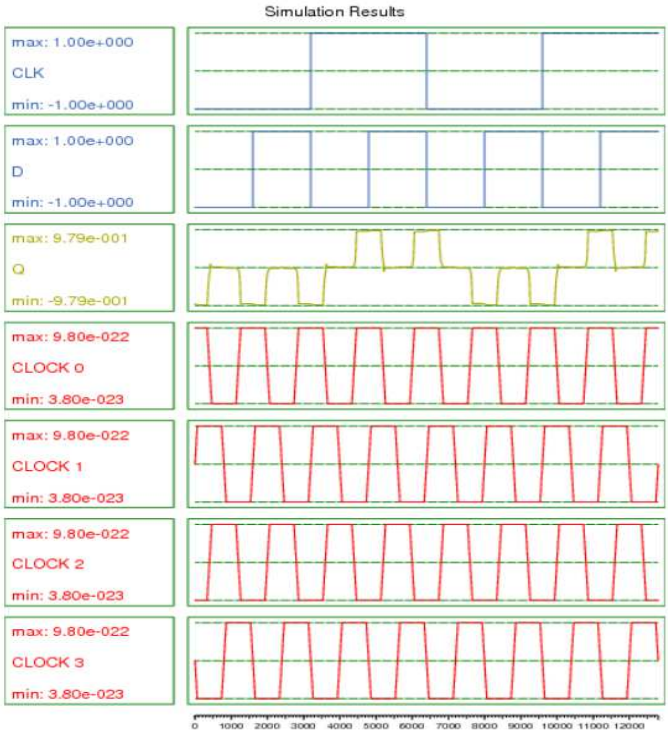


Figure 15. Simulation waveform of the proposed 14-cell QCA D-latch showing transparent and hold operating conditions.

The simulation waveform of the 14-cell Data latch circuit is shown in the Figure 15, satisfies all the conditions of the proposed Data latch circuit truth table. When the CLK is 0, output Q holds the previous

value, which means the hold condition. When CLK is 1, then output Q follows the value of D. This is called the transparent condition [32].

Proposed Data latch with Set- Reset Inputs:

The Figure 16 and Figure 17 show the proposed Data latch with Set- Reset inputs and its simulation waveform, respectively. The newly designed Data latch is implemented with the help of a 5-input majority gate, which allows integration of SET and RESET signals directly into the latch logic. The circuit uses 3 clocking zones (0-3) to propagate the signal sequentially. When Set=0 and Reset=0, then Q follows D on the active clock edge. When Set=1, Q is forced to 1 regardless of D. When Reset=1, Q is forced to 0 regardless of D. When Clk is low, Q retains its previous value. This proposed QCA Data latch with Set Reset abilities is compact, fast and fault-tolerant [33]. It reduces the area and cell count significantly, while providing direct control over the stored state. An arrangement of QCA cells has been used to come up with a more compact structure that simulates SET and RESET control inputs. The circuit relies on the Coulombic interaction of neighbouring quantum cells, instead of current flow, to represent binary information through cell polarization. This design accepts CLK/D, SET and RESET signal lines as inputs and generates the output Q by means of signal propagation in a controlled manner through multiple QCA cells arranged into controlled clocked zones. The design includes about 15 QCA cells occupying an area of $0.0048\ \mu m^2$ (Assuming a conventional size of $18\ nm * 18\ nm$ for each QCA cell). Sequential behaviour is realized efficiently through basic QCA primitives such as majority gates and signal wires.

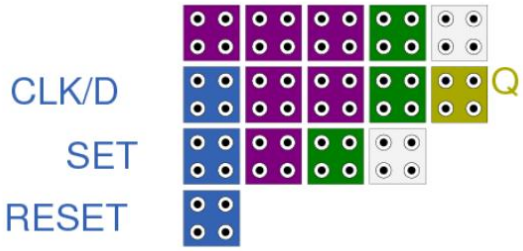


Figure 16. Proposed QCA-based D-latch architecture with integrated SET and RESET control inputs for enhanced memory functionality.

The operation is clocked by the four-phase QCA clocking scheme and spans 4 clock zones, resulting in a latency of 1 clock cycle. The presence of asynchronous SET and RESET inputs allows direct forcing of the output state independent of the data input, enhancing control and reliability of the memory element. Based on the cell count and latency, the estimated QCA cost of the design is 15, indicating a compact and efficient implementation suitable for nanoscale sequential circuits.

Simulation Waveform of Proposed Data latch with SET/RESET Capability:



Figure 17. Simulation waveform of the proposed QCA D-latch with SET and RESET functionality under different operating conditions.

Static Random Access Memory:

SRAM (Static Random Access Memory) is a volatile high-speed digital electronics memory that stores binary data by storing bistable flip-flops in the form of a 6-transistor (6T) cell [34]. Contrary to DRAM, SRAM requires no refreshing periodically, and data is stored as long as power is maintained. Random access Static random is the most important high-speed memory used in random access memories (RAMs). access memory (SRAM). SRAM is nimble and strong, but faces challenges in design below nanoscales. Complementary metal oxide semiconductors (CMOS), leakage current, area, and stability. Various technologies which can be used as an alternative to deal with the shortfalls of traditional. Quantum-dot Cellular Automata (QCA) is SRAM. A basic CMOS SRAM (Static Random Access Memory) cell consists of p-n junctions (complementary, PMOS and NMOS) and creates a bistable latch which stores a single data bit. The most typical one is the 6-transistor (6T) cell, which has two cross-coupled inverters (constituting a stable storage latch), two access transistors operated by a word line (WL) to allow a read/write access using bit lines (BL, BLB). The cell contains data when WL is low, and it is possible to read or write the stored value when WL is high. The advantage of this design is that it has low static power and a high noise margin of CMOS; however, at high nano nodes, scaling becomes difficult because of leakage and stability difficulties. Another emerging nanotechnology in the area of digital circuits is called QCA (Quantum-Dot

Cellular Automata), and it does not utilize transistor-like devices. It instead represents binary data with electron positions and polarization in arrays of quantum dots (small islands of semiconductor), with the presence of electrons in specific dots encoding logic 0 and logic 1. QCA has potential due to its very low power consumption, very small area, and possibly very high speeds - it is more effective than conventional CMOS at the nanoscale. Majority gates and inverters assemble logic into a circuit, and the flow of information is via electron interaction as opposed to flowing current as in CMOS.

Existing work of SRAM in QCA:

The SRAM memory cell is designed using a line-based approach using 39 cells in ref. [35]. This is a very complex structure with higher latency. The SRAM is showcased in ref. [36] used a loop-based approach with a 53-cell count, although it is compact in size, it required more power and a latency of 1.5 cycles. The multiplexer-based SRAM designed in ref. [37] uses 2:1 Mux and 3-input and 5-input majority gates having 109 cells. The total number of cells is more, but the SRAM shows better latency compared to other existing SRAM designs. The SRAM cell is designed using D- latch and a multiplexer using 26 cells, having a latency of 0.75 cycles and is highly compact in size. The SRAM cell designed in ref. shown in Figure 18, using a loop-based approach with a 3-input majority gate and an inverter having 25 cell count.

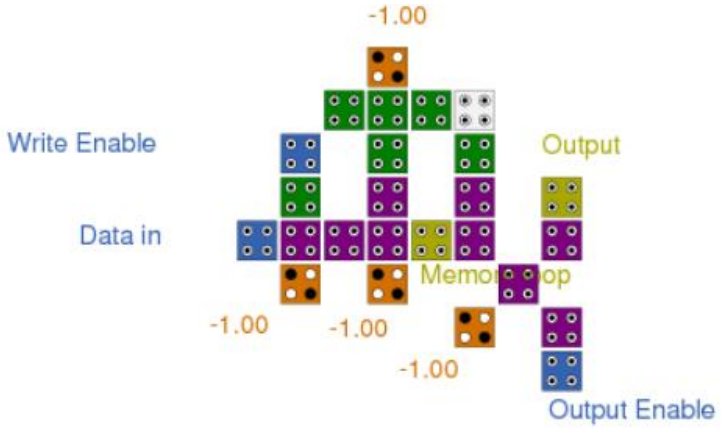


Figure 18. Existing QCA-based SRAM cell architecture implemented using a loop-based memory structure with 25 QCA cells.

QCA-based SRAM cells take up an area that is radically smaller than that of traditional CMOS SRAM cells. Whilst the QCA designs have cell sizes of approximately 0.02-0.03 mm^2, the CMOS SRAM cell in modern nodes ($65nm - 130nm$) usually measures between 0.5 mm^2 and approximately 0.08 mm^2, depending on transistor scaling. This demonstrates that QCA provides an order of magnitude decrease in the area. Table 6 shows the comparison of QCA-based and CMOS-based SRAM memory cells.

Table 6: The Comparison of the QCA-Based and CMOS-Based SRAM Cell [36]

Design	Paper No.	Cell/ Transistor Count	SRAM Cell area (μm^2)	Latency
QCA SRAM	[35]	25 Cells	0.02	0.5 cycles
QCA SRAM	[36]	26 Cells	0.02	0.75 cycles
QCA SRAM	[37]	109 Cells	0.13	1.75 cycles
CMOS 6T SRAM (45 nm)	[38]	6T	~0.5–0.8	~128–222 ps
CMOS 6T SRAM (22 nm)	[38]	6T	~0.08–0.12	~147 ps

CMOS 12T SRAM (45 nm)	[39]	12T	~1.2–1.4	~20 ns
CMOS 14T SRAM (45 nm)	[39]	14T	~1.4	~20 ns

The comparative analysis of QCA-based SRAM and CMOS-based SRAM highlights the remarkable area efficiency achieved by quantum-dot cellular automata. As shown in the table V, conventional CMOS SRAM cells, even at advanced nodes such as $22\,nm$, occupy between $0.08 - 0.12\,\mu m^2$ per cell, while radiation-hardened 12T and 14T CMOS designs at 45 nm reach up to 1.4 μm². In contrast, QCA-based SRAM architectures demonstrate a drastic reduction in occupied area, ranging from $0.046 - 0.13\,\mu m^2$ in earlier line-based and multiplexer-based designs down to only 0.02 μm² in the most compact loop-based majority-gate implementations. This corresponds to a 90–99% reduction in area compared to the 45 nm CMOS baseline. Furthermore, the proposed 25-cell QCA SRAM achieves the lowest footprint (0.02 μm²) with a latency of just 0.5 clock cycles, outperforming both traditional CMOS and earlier QCA designs. These results confirm that QCA technology not only surpasses CMOS in terms of density but also offers superior speed and cost efficiency, positioning it as a promising candidate for next-generation ultra-compact memory systems.

A conventional SRAM cell is essentially a latch that stores one bit of Data. It must support the Write and Read operations. The proposed Data latch with Set-Reset ability works as a traditional SRAM where D input will perform a data write operation, Q output will be used to store the data, SET/RESET will perform initialisation and override, ensuring reliable startup and fault recovery. Thus, the proposed Data latch is treated as a QCA SRAM cell with built-in SET/RESET capability [40]. The table shows the truth table mapping of the proposed data latch with QCA SRAM. The proposed QCA circuit can operate as a single-bit static random-access memory (SRAM) cell because it satisfies the essential functional requirements of static memory in Quantum-dot Cellular Automata technology. The design is based on a clock-controlled D-type storage structure, which inherently provides bistable behaviour necessary for data storage. When the clock signal is active, the input data is written to the memory node, while during the inactive clock phase, the circuit maintains the previously stored value due to the polarization stability of the QCA cells. This enables static data retention without the need for continuous refreshing, which is a defining characteristic of SRAM architectures. Additionally, the stored data is directly available at the output node Q, allowing non-destructive read operations. The inclusion of SET and RESET control inputs further enhances the functionality by enabling deterministic initialization and forced state control. Since the circuit provides write capability, stable data storage, direct read access, and clock-controlled operation, it fulfils the operational characteristics of a single-bit QCA SRAM cell [41]. Therefore, the proposed design can be effectively utilized as a basic memory element for QCA-based SRAM arrays and nanoscale sequential circuits. The proposed circuit behaves as a single-bit QCA SRAM memory cell implemented using a clock-controlled D-type storage structure. The design provides bistable data storage, write capability during the active clock phase, and stable data retention during the hold phase, thereby satisfying the functional requirements of static memory. Table 7 shows the mapping of the proposed Data latch with QCA SRAM.

Table 7: Truth Table Mapping of Proposed Data Latch and QCA SRAM

CLK	D	SET	RESET	Q (SRAM Output)
0	X	X	X	Hold (Q Previous Value)
1	0	0	0	Write (0)
1	1	0	0	Write (1)
X	X	1	X	Force 1 (SET)
X	X	X	1	Force 0 (RESET)

The table describes the operational behaviour of the proposed QCA memory cell, which functions as a clock-controlled data latch with additional SET and RESET control inputs. This structure allows the circuit to behave as a single-bit static memory element, similar to a QCA SRAM cell [42]. When the clock signal is low, the circuit does not accept new input data. Instead, the output Q maintains the previously stored value. This behaviour is characteristic of a data latch, where the stored state is preserved until the clock enables a new write operation. In QCA technology, this occurs during the hold phase of the clock, where the cells' polarization remains stable, ensuring static data retention. This property is essential for SRAM operation because the memory must retain data without continuous refreshing. When CLK = 1, the circuit becomes transparent to the input D, and the value of D is written into the memory node Q. If D = 0, the output becomes 0, and if D = 1, the output becomes 1. This behaviour corresponds to the write operation of an SRAM cell, where the input data is stored in the memory node. The clock signal, therefore, serves as the write enable signal, enabling controlled updates to the stored data. When the SET signal is active, the output Q is forced to logic '1', regardless of the values of the clock or data input. This feature allows direct initialization of the memory cell, which is useful during system start-up or reset operations [58]. In memory systems, such control inputs help establish a known state before normal operation begins. When the RESET signal is activated, the output Q is forced to logic '0', independent of other inputs. Similar to the SET function, this ensures reliable initialization and control of the memory element. Therefore, the proposed QCA circuit acts as a single-bit SRAM memory element, with the data latch serving as the core storage mechanism. The additional SET and RESET inputs enhance the controllability of the memory cell, enabling reliable initialization and improved operational flexibility.

Energy Dissipation of Proposed Data Latch and Data Latch with SET/RESET Capability:
The energy dissipation performance of the conventional QCA data latch (14 cells) and the proposed QCA data latch with Set/Reset capability (15 cells) is illustrated in Figure 19. The graph shows the variation of energy dissipation with respect to simulation time across the four QCA clock phases (Clock 0–Clock 3).

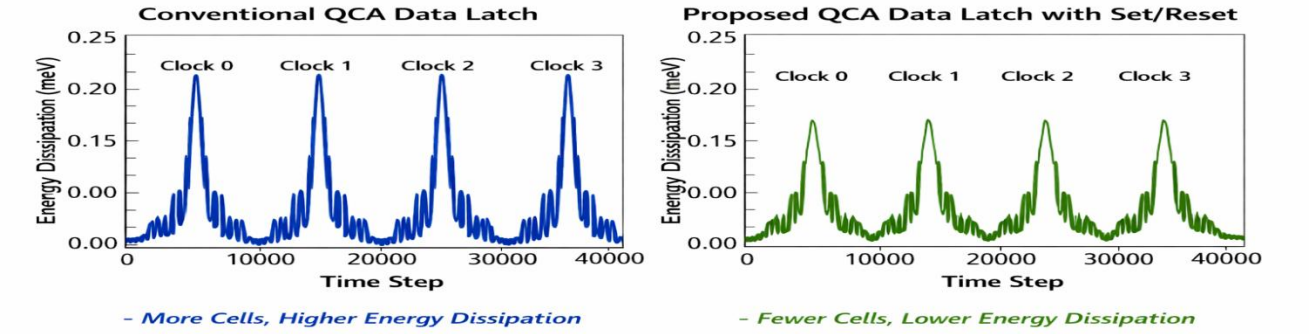


Figure 19. Comparative energy dissipation analysis of the conventional QCA D-latch and the proposed D-latch with SET/RESET capability across different clock phases.

In the conventional data latch, the energy dissipation peaks reach approximately 0.22 meV during clock transitions due to higher switching activity among the cells [43]. As the clock propagates through different phases, the repeated polarization and depolarization of the QCA cells lead to increased energy consumption. In contrast, the proposed data latch with Set/Reset functionality exhibits lower energy dissipation, with peak values around 0.17 meV. Although the proposed design uses one additional cell, the optimized cell arrangement and controlled signal propagation reduce unnecessary polarization switching.

The presence of Set and Reset control signals also improves the operational efficiency of the latch by enabling direct forcing of logic states when required, thereby minimizing switching overhead. As a result, the proposed 15-cell data latch demonstrates reduced energy dissipation and improved energy efficiency compared to the conventional 14-cell design, making it more suitable for low-power QCA-based memory and sequential circuit applications.

V. CONCLUSIONS:

The design and analysis of compact Quantum-dot Cellular Automata (QCA)-based combinational and sequential circuits for next generation nanoelectronic memory applications were presented in this chapter. The efficient sequential circuit realization was established, by implementing and analysing basic QCA logic gates and multiplexer structures. The QCA D-latch was designed, and it's able to be fabricated in a single layer architecture using only 14 cells with a layout area of 0.007 μm^2 and a clock latency of 0.5 cycles. Compared to existing latches, the results of the comparative analysis showed the achieved reduction in occupied area of around 21%, the improvement in operational speed of 20%, and significant reduction in QCA cost. Moreover, an improved QCA D latch has been designed to operate the memory with SRAM. The proposed memory structure had an area of 0.0048 μm^2, and had low energy dissipation and stable memory retention properties. It was found that the logic propagation, transparent, and hold-state operation to simulate the events were correct and the sequential functionality was reliable with various clock conditions. Results obtained prove the efficiency of the proposed QCA architectures with respect to the conventional CMOS and existing QCA memory architectures in terms of printability, low power consumption, less complexity of implementation and scalability. Thus, it is believed that the proposed designs can be useful as efficient building blocks for future ultra-dense nanoelectronic memory devices, quantum computing hardware, and low power high speed digital architectures. The potential future research directions include the development of fault tolerant QCA memories, multilayer implementations, analysis of thermal stability and integration of large-scale SRAMs for practical applications at the nanoscale level in computing systems.

Declaration

Ethics and Consent to Participate declarations: Not applicable

Consent for publication: Not Applicable

Availability of Data and Materials: Data sharing is not applicable to this article as no datasets were generated or analysed during the current study.

Competing Interest: The authors declare that they have no competing interests

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Author Contribution Declaration: PW conceptualized the study, literature review, and statistical analysis, and led the manuscript drafting. SK contributed to the design of the methodology and theoretical framework and supervised the technical validation. Both authors reviewed and approved the final manuscript.

Clinical trial number: not applicable**.**

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