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Voltage regulation control for V2G bidirectional interleaved converters based on a cascaded extended state observer

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Abstract When two-phase interleaved bidirectional direct current converters in vehicle-to-grid on-board chargers face time-varying disturbances, traditional linear active disturbance rejection control encounters limitations in balancing high-frequency noise amplification and steady-state tracking errors. To address this, an improved controller utilizing a cascaded extended state observer is proposed. A two-layer, third-order nested architecture is constructed to compensate for internal and external disturbances, facilitating disturbance reconstruction in high-frequency noise environments. Furthermore, a cross-layer mapping and feedforward mechanism is integrated to improve error feedback and reduce steady-state errors. A second-order affine control model is derived, and its mechanism for alleviating bandwidth constraints is theoretically evaluated through frequency domain responses. Simulation results indicate that the proposed strategy improves dynamic tracking and disturbance rejection compared to traditional proportional-integral and linear active disturbance rejection control methods during broadband noise injection and sudden load variations. Additionally, it demonstrates stable transition capabilities and steady-state robustness during vehicle-to-grid charge and discharge mode switching.

Keywords Vehicle-to-Grid, Two-phase interleaved converter, Active disturbance rejection control, Cascaded extended state observer, Disturbance compensation

1 Introduction

With the acceleration of the global energy transition and the electrification of transportation, the population of electric vehicles (EVs) has experienced rapid growth. The unregulated charging and discharging of large-scale EVs reduce the equivalent inertia of the grid, posing challenges to the frequency and voltage stability of distribution networks. Consequently, Vehicle-to-Grid (V2G) technology has gained significant attention[1]. This technology enables bidirectional power flow, allowing EVs to serve as distributed energy storage units that provide dynamic support for low-inertia grids, such as peak shaving and frequency/voltage regulation.

In V2G systems, the on-board charger (OBC) serves as the energy conversion hub, employing a two-phase interleaved bidirectional converter to regulate battery voltage and current. This topology is utilized to reduce current ripple, decrease component size, and improve power density. However,

transient grid fluctuations and load variations affect its voltage stability and recovery time. To improve system robustness, linear active disturbance rejection control (LADRC) integrating an extended state observer is employed. This strategy estimates and compensates for total disturbances in real-time, improving the converter's disturbance rejection capability[2-5].

Nevertheless, in practical high-frequency switching environments, the standard ESO is susceptible to measurement noise. When addressing the high non-linearity and parameter perturbations of interleaved systems, traditional LADRC faces a trade-off in parameter tuning: increasing the observation bandwidth to reduce low-frequency tracking errors versus decreasing it to suppress high-frequency switching noise[6-7]. To address these challenges, several control strategies have been proposed recently, including high-gain decoupling control, adaptive sliding mode control, model predictive control, and modified ADRC based on generalized proportional-integral observers[8-13]。. Meanwhile, intelligent algorithms such as neural network prediction and fuzzy inference have been applied to optimize steady-state performance[14-19]。. In the fields of microgrid inverters and V2G systems, coordinated ADRC designs have improved steady-state operation quality to some extent[20-21]. However, further research is needed to address the initial inverse dip in non-minimum phase systems and the issues of state estimation delay and steady-state error under continuous ramp disturbances[22].

Targeting high-frequency nonlinear features in two-phase interleaved bidirectional converters, this paper proposes an improved active disturbance rejection control strategy based on a cascaded extended state observer(CESO-ADRC). By reconstructing the observer topology through cross-layer mapping and feedforward compensation, the method addresses internal and external disturbances in high-frequency noise environments. Theoretical analysis indicates that this mechanism relaxes bandwidth constraints and reduces steady-state errors for continuous time-varying disturbances. Evaluated via MATLAB and Simulink, the proposed strategy improves upon traditional PID and linear active disturbance rejection control under load mutations, broadband noise, and vehicle-to-grid mode transitions. Consequently, it improves dynamic tracking, noise suppression, and steady-state robustness while maintaining parameter design simplicity.

2.Modeling and affine nonlinear reconstruction of two-phase interleaved bidirectional converters

To analyze nonlinear coupling and establish a theoretical basis for cascaded extended state observer (CESO) design, this section derives the continuous-time average signal model. Using the Boost mode as a representative case, the model is restructured into a standard second-order ADRC affine control form.

2.1Large-signal average state-space modeling in continuous conduction mode

In the two-phase interleaved bidirectional Buck/Boost converter structure, let U_{bat} denote the output voltage at the low-voltage battery terminal and U_{dc} represent the regulated output voltage at the high-voltage DC bus. The filter inductors are designed symmetrically as $L_1 = L_2 = L$, the high-frequency DC filter capacitor is $C_{f1} = C$, and R is the equivalent DC load impedance on the grid-tied inverter side. The power switches in both phases operate with a 180° phase shift under a duty cycle d.

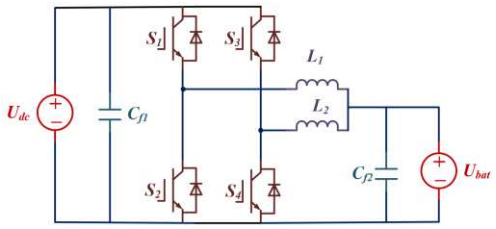


Fig. 1 Topology of the two-phase interleaved bidirectional Buck/Boost converter

When the converter operates in continuous conduction mode, the total input inductor current flowing into the high-voltage side is defined as $i_\Sigma = i_{L1} + i_{L2}$. Based on Kirchhoff's voltage and current laws, the reduced-order large-signal average state-space nonlinear equations can be established:

$$\begin{cases} \dfrac{L}{2}\dfrac{di_\Sigma}{dt} = V_{bat} - (1-d)u_c \\ C\dfrac{du_c}{dt} = (1-d)i_\Sigma - \dfrac{u_c}{R} \end{cases} \tag{1}$$

To extract the nominal parameters required for controller design, the nonlinear differential equations containing the product terms $(1-d)u_c$ and $(1-d)i_\Sigma$ must be linearized at the steady-state operating point (U_c, I_Σ, D). By introducing small-signal perturbations $u_c = U_c + \Delta u_c$, $d = D + \Delta d$, and $i_\Sigma = I_\Sigma + \Delta i_\Sigma$ into (1) and neglecting second-order bias terms, the Laplace transform is applied. Through algebraic elimination in the complex frequency domain, the core transfer function $G_{vd}(s)$ from the control input (duty cycle perturbation $\Delta d(s)$) to the controlled output (voltage perturbation $\Delta u_c(s)$) is derived:

$$G_{vd}(s) = \frac{\Delta u_c(s)}{\Delta d(s)} = \frac{V_{in}}{LCs^2 + \dfrac{L}{R}s + 1} \tag{2}$$

In (2), V_{in} represents the equivalent input voltage gain near the operating point. The pole distribution of this small-signal transfer function indicates that the two-phase interleaved converter exhibits the characteristics of a second-order underdamped system with non-minimum phase features near its steady-state equilibrium.

2.2System dimension reduction, decoupling, and disturbance lumped-parameterization for ADRC

Linear ADRC treats internal uncertainties and external perturbations as a total lumped disturbance. By defining the output bus voltage as $y = u_c$ and the input duty cycle as $u = d$, time-domain mapping yields the corresponding second-order linear constant-coefficient differential equation:

$$LC\ddot{y} + \frac{L}{R}\dot{y} + y = V_{in}u + n(t) \tag{3}$$

In (3), $n(t)$ represents the unknown external lumped disturbances induced by the dead-time effect of power devices, parasitic losses, time-varying battery internal resistance, and circulating current imbalances between the interleaved phases.

To extract the standard control gain, (2) is divided by the energy storage network inertia coefficient LC for restructuring:

$$\ddot{y} = b_{real}u + d_{ext}(t) \tag{4}$$

In (4), $b_{real} = \dfrac{V_{in}}{LC}$ is defined as the actual physical control gain, and the dynamic external disturbance term $d_{ext}(t)$ is defined as:

$$d_{ext}(t) = -\frac{1}{RC}\dot{y} - \frac{1}{LC}y + \frac{n(t)}{LC} \tag{5}$$

Under prolonged operation involving high-frequency switching and power exchange, the core magnetic components of the converter are prone to magnetic saturation, and the filter capacitance may drift with temperature. Consequently, the actual physical gain b_{real} is difficult to determine precisely. Therefore, a nominal control gain $b_0 = \frac{V_{in,nom}}{L_{nom}C_{nom}}$ is introduced as a prior design reference.

By unifying the unmodeled high-frequency dynamics within the converter, state drifts caused by parameter perturbations, and all external mutation interferences, the generalized total disturbance of the system $f(t)$ is defined:

$$f(t) = d_{ext}(t) + (b_{real} - b_0)u = -\frac{1}{RC}\dot{y} - \frac{1}{LC}y + \frac{n(t)}{LC} + (b_{real} - b_0)u \tag{6}$$

Finally, the coupled nonlinear voltage dynamic model of the two-phase interleaved bidirectional converter is effectively decoupled and reconstructed as a standard second-order ADRC affine controlled equation:

$$\ddot{y} = f(t) + b_0 u \tag{7}$$

3. Design of improved cascaded extended state observer and control law synthesis

To address traditional LADRC limitations, this paper introduces a restructured cascaded observer for second-order converters. Its dual-layer nested mechanism and cross-layer mapping optimize the error polynomial while suppressing high-frequency noise.

3.1Analysis of limitations in traditional single extended state observers

For the reconstructed second-order system described in (7), standard LADRC typically employs a single third-order linear ESO to simultaneously estimate the system states and the total disturbance. With the actual output voltage and control input duty cycle defined as inputs, the continuous-time state-space equations before discretization are expressed as:

$$\begin{cases} e_1 = y - z_1 \\ \dot{z}_1 = z_2 + 3\omega_o e_1 \\ \dot{z}_2 = z_3 + 3\omega_o^2 e_1 + b_0 u \\ \dot{z}_3 = \omega_o^3 e_1 \end{cases} \tag{8}$$

In (8), z_1 and z_2 represent the estimates of the output voltage and its first-order derivative, respectively, while z_3 denotes the estimate of the total disturbance $f(t)$.

The parameter ω_o signifies the observer bandwidth. However, a single-observer structure faces significant challenges in simultaneously attenuating high-frequency switching noise and minimizing low-frequency tracking errors. This conflict often results in mutual performance constraints during practical parameter tuning.

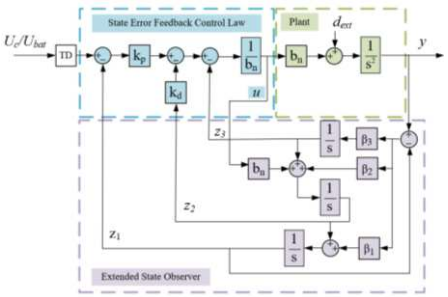


Fig. 2 Control structure of the traditional third-order linear extended state observer

3.2Structural design of the dual-layer cascaded extended state observe

To mitigate the trade-off between observation bandwidth and high-frequency noise suppression characteristic of traditional LADRC, this work develops a dual-layer cascaded ESO topology. This architecture nests a primary state observer with a secondary cooperative observer, coupled through state feedforward signals.

3.2.1Primary state extraction and feedforward disturbance observer design

The first-layer observer processes the DC bus voltage and duty cycle. To regulate dynamic response, its characteristic poles are configured with a high-frequency bandwidth parameter ω_{o1}. The corresponding state-space equations are:

$$\begin{cases} e_{11} = y - z_{11} \\ \dot{z}_{11} = z_{12} + 3\omega_{o1} e_{11} \\ \dot{z}_{12} = z_{13} + 3\omega_{o1}^2 e_{11} + b_0 u \\ \dot{z}_{13} = \omega_{o1}^3 e_{11} \end{cases} \tag{9}$$

To implement feedforward compensation, the disturbance estimate $\hat{f}_1$ integrates the integral state variable z_{13} with a proportional error response channel:

$$\hat{f}_1 = 3\omega_{o1}^2 e_{11} + z_{13} \tag{10}$$

When the bus voltage experiences an initial dip under complex operating conditions, this proportional channel facilitates a rapid response, thereby providing a feedforward compensation signal of sufficient magnitude from the first layer.

3.2.2Disturbance residual tracking and cooperative compensation observer design

The second-layer ESO incorporates the feedforward estimate $\hat{f}_1$ as a coupling term. It is configured with a lower observation bandwidth ω_{o2} to filter high-frequency noise and improve steady-state estimation. The state-space equations are expressed as:

$$\begin{cases} e_{21} = y - z_{21} \\ \dot{z}_{21} = z_{22} + 3\omega_{o2} e_{21} \\ \dot{z}_{22} = z_{23} + 3\omega_{o2}^2 e_{21} + b_0 u + \hat{f}_1 \\ \dot{z}_{23} = \omega_{o2}^3 e_{21} \end{cases} \tag{11}$$

Through the feedforward injection of $\hat{f}_1$, the plant model is transformed from $y = f(t) + b_0 u$ to $y = \Delta f(t) + (b_0 u + \hat{f}_1)$. The second layer subsequently tracks the low-frequency residual disturbance, outputting this estimate via a pure integral channel:

$$\hat{f}_2 = z_{23} \tag{12}$$

3.3Cross-layer state synthesis and feedback control parameter configuration

Based on the aforementioned restructuring logic, the proposed CESO architecture utilizes a cross-layer mapping mechanism for global signal synthesis, which is subsequently fed into the state error feedback control law:

$$\begin{cases} \hat{y} = z_{21} \\ \hat{y} = z_{22} \\ \hat{f}_{total} = \hat{f}_1 + \hat{f}_2 = (3\omega_{01}^2 e_{11} + z_{13}) + z_{23} \end{cases} \tag{13}$$

Using this compensation signal, the control law is designed through a linear error feedback structure. For a given DC bus voltage reference y^*, a proportional-derivative control action is formulated:

$$u_0 = k_p(y^* - z_{21}) + k_d(\dot{y}^* - z_{22}) \tag{14}$$

Finally, by integrating the feedback control action with the disturbance compensation signal, a global control law is established to generate the duty cycle control signal for the interleaved DC-DC converter:

$$u = \frac{u_0 - \hat{f}_{total}}{b_0} = \frac{k_p(y^* - z_{11}) + k_d(\dot{y}^* - z_{12}) - (3\omega_{o1}^2 e_{11} + z_{13} + z_{23})}{b_0} \tag{15}$$

This mechanism of coordinated extraction and compensation alleviates the structural coupling effects of the closed-loop error transfer function. Without significantly magnifying the high-frequency noise gain, this strategy effectively enhances the steady-state tracking performance for continuous, time-varying disturbances.

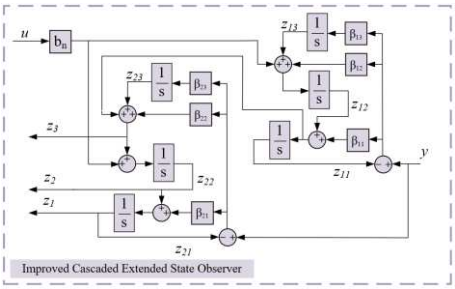


Fig. 3 Control structure of the improved dual-layer cascaded extended state observer

4Analysis of stability and frequency-domain disturbance rejection of the improved CESO structure

Traditional LADRC is sensitive to high-frequency noise and continuous disturbances. The proposed CESO mitigates these issues through dual-layer asymmetric mapping and feedforward coupling. This section mathematically evaluates its closed-loop convergence stability and disturbance rejection performance.

4.1Proof of observer convergence and closed-loop system stability

For the primary state observer in the first layer, the characteristic polynomial $\Delta_1(s)$ is determined by the pole placement:

$$\Delta_1(s) = s^3 + \beta_{11}s^2 + \beta_{12}s + \beta_{13} = (s + \omega_{o1})^3 \tag{16}$$

Similarly, the characteristic polynomial $\Delta_2(s)$ for the cooperative state observer in the second layer is:

$$\Delta_2(s) = s^3 + \beta_{21}s^2 + \beta_{22}s + \beta_{23} = (s + \omega_{o2})^3 \tag{17}$$

Setting $\omega_{o1} > 0$ and $\omega_{o2} > 0$ places all characteristic roots in the left-half complex plane, ensuring the state estimation errors $E_1(s)$ and $E_2(s)$ converge asymptotically.

For a reference voltage y^*, the proportional-derivative control law is defined as

$u_0 = k_p(y^* - z_{21}) + k_d(\dot{y}^* - z_{22})$. Incorporating disturbance cancellation, the duty cycle is given by $u = (u_0 - f_{ceso})/b_0$. Substituting this into the system model (8) yields:

$$\ddot{y} = f(t) + b_0\left[\frac{k_p(y^* - z_{21}) + k_d(\dot{y}^* - z_{22}) - f_{ceso}}{b_0}\right] \tag{18}$$

Given the asymptotic convergence of CESO, the estimated states approach their actual values near steady state: $z_{21} \approx y$, $z_{22} \approx \dot{y}$, and $f_{ceso} \approx f(t)$. Total disturbances are compensated, reducing the closed-loop dynamics to a linear constant-coefficient differential equation:

$$\ddot{y} + k_d\dot{y} + k_p y = k_p y^* + k_d \dot{y}^* \tag{19}$$

The closed-loop characteristic equation is $s^2 + k_d s + k_p = 0$. Through pole placement, setting $k_p = \omega_c^2$ and $k_d = 2\omega_c$ ensures system stability for any controller bandwidth $\omega_c > 0$. Consequently, the converter under CESO-ADRC achieves bounded-input bounded-output stability.

4.2Analysis of disturbance estimation error transfer function and frequency-domain response

Assuming zero initial conditions, applying the Laplace transform to the first-layer state-space equation allows for the derivation of the preliminary tracking observation error transfer function $E_1(s)$ for the total disturbance $F(s)$:

$$E_1(s) = Y(s) - Z_{11}(s) = \frac{s}{\Delta_1(s)}F(s) \tag{20}$$

Simultaneously, leveraging the full-dimensional direct-through mechanism of internal variables, the primary feedforward estimate $F_{to1}(s)$ of the total disturbance from the first layer is:

$$F_{to1}(s) = \frac{\beta_{11}s^2 + \beta_{12}s + \beta_{13}}{\Delta_1(s)}F(s) \tag{21}$$

Combining (20) and (21), the real physical residual $E_{f1}(s)$ that the first layer fails to cover and leaves to the second layer is:

$$E_{f1}(s) = F(s) - F_{to1}(s) = \frac{s^3}{\Delta_1(s)}F(s) \tag{22}$$

The second layer adopts $E_{f1}(s)$ as its sole tracking target. The secondary residual disturbance estimate $F_{to2}(s)$ output from this layer to the overall system is in pure integral form:

$$F_{to2}(s) = \frac{\beta_{23}}{\Delta_2(s)}E_{f1}(s) \tag{23}$$

The final global disturbance estimation error $E_{total}(s)$ is:

$$E_{total}(s) = F(s) - F_{to1}(s) - F_{to2}(s) = E_{f1}(s)\left(1 - \frac{\beta_{23}}{\Delta_2(s)}\right) \tag{24}$$

Substituting the expression for $E_{f1}(s)$ and the polynomial $\Delta_2(s)$ into (24), algebraic simplification yields the high-order closed-loop transfer function relationship for the global disturbance estimation error:

$$E_{total}(s)=\frac{s^3}{\Delta_1(s)}F(s)\cdot\frac{s(s^2+\beta_{21}s+\beta_{22})}{\Delta_2(s)}=\frac{s^4(s^2+\beta_{21}s+\beta_{22})}{\Delta_1(s)\Delta_2(s)}F(s) \tag{25}$$

Integral compensation in the second-layer CESO expands the error transfer function's numerator polynomial. Under continuous time-varying disturbances such as load steps, the final value theorem yields the steady-state estimation error e_{fss} as:

$$e_{fss}=\lim_{s\to 0}sE_{total}(s)=0 \tag{26}$$

The result of this limit approaching zero indicates that the disturbance observation error in the steady state is effectively suppressed.

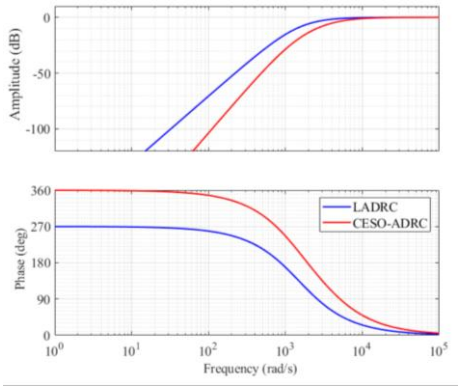


Fig. 4 Bode plot comparison of disturbance estimation error transfer functions for traditional and improved observers

Fig. 4 presents a frequency-domain Bode plot comparison of the disturbance estimation error transfer functions between traditional LADRC and the improved CESO-ADRC. From the magnitude response curves, it is evident that in the low-to-medium frequency range, CESO-ADRC exhibits a larger initial attenuation slope and a lower error magnitude gain at the same frequency compared to traditional LADRC. This further validates the effectiveness of the proposed structure in suppressing continuous time-varying disturbances from a frequency-domain perspective.

5. Simulation verification and result analysis

5.1Simulation model construction and core parameter configurations

To rigorously evaluate the dynamic performance and robustness of the proposed improved CESO-ADRC strategy under complex operating conditions, a simulation model of the two-phase interleaved bidirectional Buck/Boost converter was developed in MATLAB/Simulink. The core operating parameters of the system are detailed in Table 1.

Table 1 Core simulation parameters of the two-phase interleaved bidirectional converter

Parameter Name	Symbol	Value
Rated transmission power of converter	P_{nom}	70kW
High-voltage side nominal DC voltage	U_{dc}	700V
Low-voltage side nominal DC voltage	U_{bat}	400V
High-frequency switching frequency	f_{sw}	50kHz

Parameter Name	Symbol	Value
Interleaved filter inductors	L_1,L_2	120uH
High-voltage side DC filter capacitor	C_{f1}	1000uF
Low-voltage side DC filter capacitor	C_{f2}	300uF
PID control parameters	k_p,k_i,k_d	0.0015,0.7,0
Traditional LADRC bandwidth	ω_o	1500rad/s
CESO-ADRC bandwidths	ω_{o1},ω_{o2}	4500rad/s,1500rad/s

5.2Performance comparison under complex steady-state and transient conditions

Addressing the typical operating scenarios a V2G charger may encounter, this section compares the performance of PID, traditional LADRC, and the proposed CESO-ADRC strategies under Buck, Boost, and mode-switching conditions.

5.2.1Transient and steady-state disturbance rejection performance in Buck mode

During the Buck mode, control performance is assessed against sudden load steps and complex input perturbations. A load step mutation is introduced at t = 0.05 s.

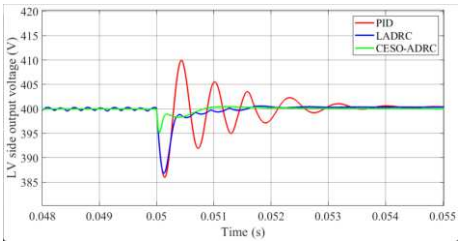


Fig. 5 Dynamic response of output voltage under load step change in Buck mode

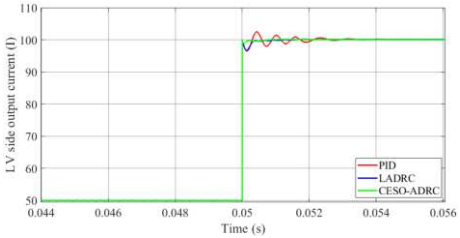


Fig. 6 Dynamic response of output current under load step change in Buck mode

Figures 5 and 6 illustrate the dynamic voltage and current responses to a load step. Traditional PID control exhibits oscillations, voltage dips, overshoots, and longer recovery times. While LADRC improves damping and eliminates overshoots, it still experiences initial voltage dips and current regulation delays. The proposed CESO-ADRC improves upon both baseline methods. By utilizing feedforward compensation, it restricts voltage and current fluctuations, avoids overshoots or undershoots, and achieves steady-state recovery with reduced tracking ripples.

To further gauge the system's resilience against continuous time-varying disturbances, random broadband noise and sinusoidal perturbations are injected into the converter's input terminal.

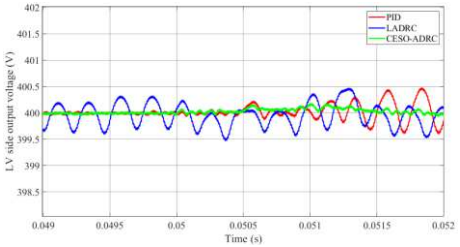


Fig. 7 Steady-state voltage response under broadband random input disturbance in Buck mode

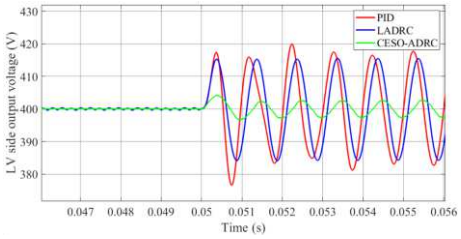


Fig. 8 Steady-state voltage response under sinusoidal time-varying input disturbance in Buck mode

Figures 7 and 8 evaluate the system's robustness against continuous input disturbances. Under a 100 V random broadband disturbance, both PID and LADRC experience tracking oscillations, while CESO-ADRC anchors the output near the 400 V baseline, demonstrating improved high-frequency noise suppression. Furthermore, when subjected to a 40 V sinusoidal disturbance, PID and LADRC exhibit periodic voltage fluctuations, reaching ranges of 376 V to 420 V and 384 V to 416 V, respectively. Relying on its dual-layer compensation, CESO-ADRC narrows this fluctuation range to between 397 V and 404 V, mitigating steady-state tracking errors.

5.2.2Transient and steady-state disturbance rejection performance in Boost mode

In the Boost mode, where the power battery feeds energy back to the grid, the comprehensive performance of the system facing similar disturbances is further investigated.

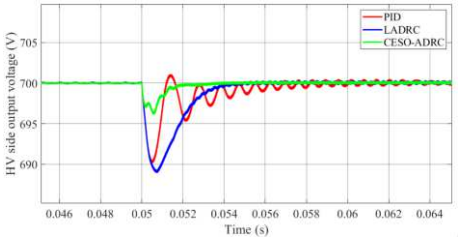


Fig. 9 Dynamic response of output voltage under load step change in Boost mode

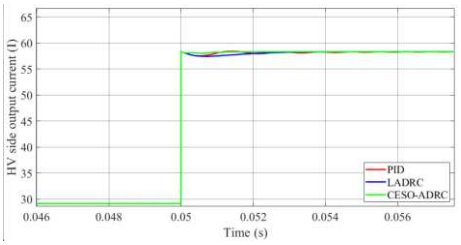


Fig. 10 Dynamic response of output current under load step change in Boost mode

Figures 9 and 10 illustrate the dynamic voltage and current responses following a load step. Traditional PID control presents voltage dips, oscillations, and slower current regulation. LADRC similarly exhibits a slower voltage recovery ramp and current tracking delays. The proposed CESO-ADRC addresses these issues by reducing the initial reverse voltage drop, restricting undershoot, and achieving a faster current tracking trajectory, ensuring restoration to the steady-state target.

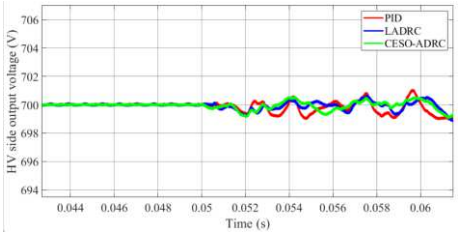


Fig. 11 Steady-state voltage response under broadband random input disturbance in Boost mode

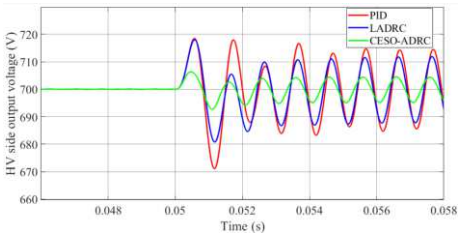


Fig. 12 Steady-state voltage response under sinusoidal time-varying input disturbance in Boost mode

External grid-side disturbance rejection is documented in Fig. 11 and Fig. 12, which record voltage responses under superimposed random broadband and sinusoidal disturbances. Under the 100 V random disturbance, CESO-ADRC yields a smaller voltage fluctuation amplitude compared to PID and LADRC, converging along the 700 V central axis. During the 40 V sinusoidal disturbance, PID and LADRC voltage fluctuations reach 671 V to 718 V and 681 V to 718 V, respectively. In comparison, CESO-ADRC confines the fluctuation to a 692 V to 706 V range, maintaining stable voltage regulation capability.

5.2.3Smooth switching response test for V2G bidirectional charge and discharge modes

he V2G application environment requires the converter to transition between Buck and Boost modes. This section conducts a comparative analysis focusing on the startup voltage establishment process and transient impacts during bidirectional mode switching.

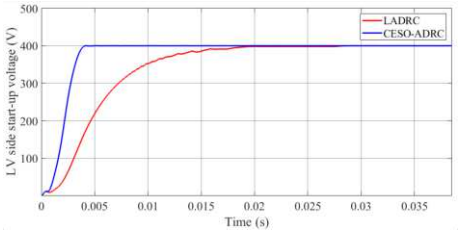


Fig. 13 Low-voltage side voltage establishment response during smooth transition from Buck to Boost mode

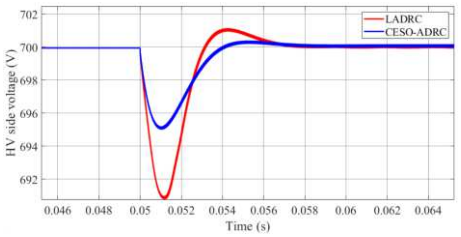


Fig. 14 High-voltage side transient anti-impact response during smooth transition from Buck to Boost mode

Figures 13 and 14 illustrate the dynamic responses during the transition from Buck to Boost mode. During the low-voltage startup to 400 V, traditional LADRC requires 18 ms to establish a steady state due to integral lag. CESO-ADRC achieves this plateau in 4 ms without overshoot. Regarding the energy reversal impact on the high-voltage side, LADRC experiences a 9.2 V transient drop and an 8 ms settling time. CESO-ADRC mitigates this impact by reducing the voltage drop to 5 V and the settling time to 5 ms, facilitating a smoother transition.

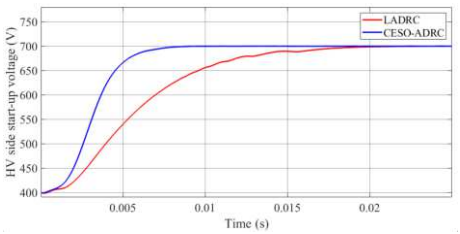


Fig. 15 High-voltage side voltage establishment response during smooth transition from Boost to Buck mode

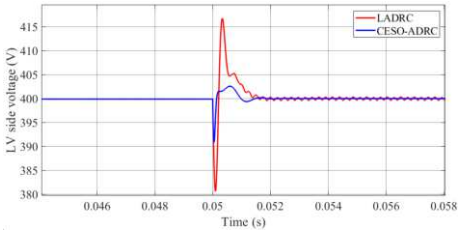


Fig. 16 Low-voltage side transient anti-impact response during smooth switching from Boost to Buck mode

Figures 15 and 16 illustrate the system dynamics during the Boost to Buck mode transition. On the high-voltage side, traditional LADRC exhibits response lag, requiring 18 ms to climb from 400 V to 700 V, whereas CESO-ADRC establishes steady state in 7 ms. Concurrently, the low-voltage side under LADRC experiences transient fluctuations, including a 19.5 V undershoot and a 16.5 V overshoot. By utilizing dynamic compensation, CESO-ADRC damps these impacts, limiting the initial voltage drop to approximately 9 V and achieving faster steady-state convergence.

6. Conclusion

To address nonlinear disturbances in two-phase interleaved bidirectional converters for V2G chargers, an improved cascaded active disturbance rejection control strategy is proposed.

A dual-layer, third-order extended state observer nested coupling mechanism is introduced to address the limitations of traditional linear methods. By optimizing the disturbance estimation error structure through feedforward compensation, this architecture suppresses steady-state errors from continuous time-varying disturbances and relaxes the observer's bandwidth constraints.

Performance validations indicate that the proposed strategy improves upon traditional proportional-integral and linear active disturbance rejection control methods. It mitigates transient voltage fluctuations during load steps and external disturbances while suppressing high-frequency ripples. Furthermore, it stabilizes transitions during bidirectional charge and discharge mode switching by reducing the initial inverse voltage dip inherent to non-minimum phase systems.

Consequently, this strategy demonstrates practical applicability, offering a reference for voltage regulation in vehicle-grid interactions, distributed energy storage, and microgrid applications.

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Declarations

Competinginterests The authors declare no competing interests

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