Research Square

Preprints are preliminary reports that have not undergone peer review.
They should not be considered conclusive, used to inform clinical practice,
or referenced by the media as validated information.

Mass-Manufacturable Germanium Photodetectors for Beyond-448-Gbps-Class Operation on a Monolithic Silicon Photonics Platform

Yusheng Bian

yushengbian@gmail.com

GlobalFoundries https://orcid.org/0000-0003-1163-5231

Sujith Chandran
Globalfoundries

Qidi Liu
Globalfoundries

Abdelsalam Aboketaf
Globalfoundries

Won Suk Lee
Globalfoundries

Teodor Stanev
Globalfoundries

Hanyi Ding
Globalfoundries

Brian Popielarski
Globalfoundries

Madhuchhanda Brahma
Globalfoundries

Michelle Zhang
Globalfoundries

James Garofolo
GlobalFoundries

Shaun Benjamin
GlobalFoundries

Crystal Hedges
GlobalFoundries

Jason Kim
GlobalFoundries

Zahidur Chowdhury

GlobalFoundries
Koushik Ramachandran
GlobalFoundries
Massimo Sorbara
GlobalFoundries
Shantanu Pal
GlobalFoundries
Takako Hirokawa
GlobalFoundries
Judson Holt
GlobalFoundries
Michal Rakowski
GlobalFoundries
Ming Gong
GlobalFoundries https://orcid.org/0000-0003-1665-0406
Kevin Dezfulian
GlobalFoundries
Mrunal Shah
GlobalFoundries
Helen Wong
GlobalFoundries
Paul Diglio
GlobalFoundries
Ben Cadieux
GlobalFoundries
Daniel Smith
GlobalFoundries
Javier Ayala
GlobalFoundries
Asli Sahin
GlobalFoundries
Eric Snow
GlobalFoundries
Ken Giewont
GlobalFoundries
Bob Mulfinger
GlobalFoundries
Ryan Sporer
GlobalFoundries

Lukas Chrostowski
Department of Electrical & Computer Engineering, University of British Columbia, 2332 Main Mall, Vancouver V6T1Z4 BC, Canada
Graham Reed
University of Southampton https://orcid.org/0009-0002-5314-6604
Keren Bergman
Columbia University https://orcid.org/0000-0001-8580-1728
John Bowers
Department of Electrical and Computer Engineering, University of California, Santa Barbara
https://orcid.org/0000-0003-4270-8296

Physical Sciences - Article

Keywords:

Posted Date: June 1st, 2026

DOI: https://doi.org/10.21203/rs.3.rs-9682597/v1

License: This work is licensed under a Creative Commons Attribution 4.0 International License.
Read Full License

Additional Declarations: There is **NO** Competing Interest.

Abstract

The explosive growth of artificial intelligence (AI) and high-performance computing (HPC) workloads is placing increasingly stringent demands on optical interconnects for fast, reliable, and mass-manufacturable photonic receivers 1–3. Germanium (Ge)-on-silicon (Si) photodetectors have demonstrated impressive bandwidth and responsivity, yet large-signal operation beyond 400 Gbps per wavelength has remained largely inaccessible in foundry-compatible platforms 4–6. Here we show that a mass-manufacturable 300 mm monolithic complementary metal-oxide-semiconductor (CMOS) silicon photonics (SiPh) platform can overcome this limitation. An O-band Ge-on-Si lateral photodetector achieves large-signal data rates exceeding 448 Gbps per wavelength with four-level pulse-amplitude modulation (PAM4) and 520 Gbps with six-level pulse-amplitude modulation (PAM6) at a photocurrent of ~2 mA. This performance is enabled by an optoelectronic bandwidth of up to ~215 GHz, near-unity quantum efficiency, and a record bandwidth-responsivity product exceeding ~217 GHz·A W^{-1} - more than 2 times higher than the previous best of 108 GHz·A W^{-1} for waveguide-coupled Ge photodiodes - while sustaining optical input powers up to 2.8 mW and maintaining sub-38 nA dark current at -1 V bias. Crucially, these metrics are attained without inductive peaking, avalanche gain, or transimpedance-amplifier (TIA) integration, with uniform high-speed characteristics across a full 300 mm wafer, underscoring production-level reproducibility. The same platform supports high speed depletion mode, travelling wave Si Mach-Zehnder modulators (MZMs) capable of ≥400 Gbps per wavelength operation without digital signal processing (DSP), precision silicon nitride (SiN) wavelength division multiplexing (WDM) filters with sub 1.5 nanometre channel stability, low loss detachable fibre-chip input-output (I/O) (~1 dB per facet), co integrated CMOS circuits using ≥350 GHz class ft transistors, and advanced wafer level packaging features. To the best of our knowledge, this is the first monolithic CMOS silicon photonics foundry platform uniting ≥400 Gbps-class transmitter and receiver functions on a single substrate, providing a scalable foundation for next-generation pluggable, near- and co-packaged (NPO/CPO) optical interconnects in AI/HPC systems.

Introduction

The continued growth of AI, cloud computing, and HPC has transformed optical-interconnect bandwidth into a primary system-level constraint, driven by the need for ever-higher per-lane data rates to sustain aggregate throughput[1–3]. Optical interconnect roadmaps have therefore converged on aggressive per-lane scaling - from 100 Gbps to 200 Gbps and now toward 400 Gbps and beyond - to enable 1.6 Tbps and 3.2 Tbps optical modules[1,2,7]. At these data rates, incremental component-level improvements are no longer sufficient. In practice, achieving a 400 Gbps per lane requires operation at ~448 Gbps when forward-error correction overhead is included, placing particularly stringent demands on receiver bandwidth and large-signal performance. Scalable deployment instead requires production-ready platform solutions that jointly address bandwidth, power handling, foundry-compatible manufacturability, packaging-aware system integration, and end-to-end scalability[3,8].

Silicon photonics (SiPh) offers a compelling foundation for this transition by combining dense photonic integration with mature CMOS manufacturing[8–11]. Large-scale deployment of Si modulators[12,13], coarse and dense WDM components[14], and optical I/O interfaces[15] have established wafer-scale photonics as a viable technology for datacenter applications. However, as per-lane data rates approach and exceed 400 Gbps, both the transmitter and receiver increasingly limit system scaling. On the transmitter side, heterogeneous and hybrid approaches based on lithium niobate ($LiNbO_3$)[16–21], lithium tantalate ($LiTaO_3$)[22–24], electro-optic polymers[25,26], and plasmonic device concepts[27,28] have demonstrated 400 Gbps-class modulation capability. However, these approaches typically rely on non-standard materials or process flows that are not fully compatible with CMOS foundry manufacturing, and a pure-Si, production-ready platform integrating matched ≥400 Gbps-class transmit and receive functions on a single substrate - without reliance on extensive DSP - remains unavailable. On the receiver side, III-V photodetectors can provide very high bandwidth[29,30] but most of them are implemented as discrete receive modules, while Si-integrated implementations commonly require heterogeneous integration[31–37], which can complicate wafer-fab manufacturing flows and present challenges to CMOS compatibility and integration density. By contrast, conventional Ge-on-Si photodetectors have struggled to simultaneously achieve the bandwidth, responsivity, large-signal linearity, and yield required for extreme speed operation within foundry-compatible process windows[4,5].

Previous work has reported impressive optoelectronic bandwidths in Ge p-intrinsic-n (PIN) photodiodes, including isolated demonstrations of >100 GHz small-signal bandwidth enabled primarily through aggressive geometry scaling[5,38] and electrical optimization such as inductive peaking[39–41]. For example, C-band Ge-fin waveguide photodiodes have demonstrated optoelectronic 3-dB bandwidths up to 265 GHz[5]; however, these devices exhibit relatively modest internal responsivities (~0.3 A W^{-1}), dark currents on the order of 100 - 200 nA, and have been characterized only under small-signal conditions. The associated fabrication complexity and deeply scaled Ge feature sizes (e.g. < 100 nm) further raise challenges for scalable manufacturing. In a complementary approach, C-band ultra-thin Ge photodetectors on a 300-mm SiPh platform have achieved ~100 GHz bandwidth with responsivities up to 1.05 A W^{-1} and dark currents below 20 nA, although the performance relies sensitively on aggressive thickness control and process tuning[42]. A compact C-band lateral-junction Ge photodiode employing butt-coupling and on-chip gain peaking has also demonstrated a bandwidth of 136 GHz, but with reduced responsivity (0.66 A W^{-1}) and elevated dark current (309.2 nA at -1 V)[41]. Avalanche photodetectors, by contrast, have largely emphasized sensitivity enhancement rather than extreme speed[6], as avalanche build-up dynamics fundamentally constrain bandwidth. Recent demonstrations include a separated-absorption-charge-cliff-multiplication (SACCM) Ge/Si avalanche photodetector achieving 105 GHz bandwidth with a gain-bandwidth product of ~4,800 GHz and 260 Gbps PAM4 reception[43], albeit with dark current reaching up to 19 μA. As a result, despite substantial progress in device physics, many demonstrations prioritize small-signal metrics, receiver-only operation, or concepts relying on aggressive electrical compensation, or avalanche multiplication that can complicate scalable SiPh manufacturing and product-level yield. Consequently, a production-ready 300-mm SiPh platform

capable of supporting ≥400 Gbps-class reception together with matched, pure-Si electro-optic modulation - without reliance on extensive digital signal processing - has remained elusive.

Here we address this gap by demonstrating a monolithically integrated CMOS SiPh foundry platform centered on an ultra-fast Ge-on-Si photodetector, exhibiting up to 215 GHz bandwidth and near-unity quantum efficiency, enabling record bandwidth-responsivity product and large-signal reception beyond 448 Gbps per wavelength. On the same 300-mm CMOS SiPh platform, we integrate pure-Si transmit-side building blocks, including high-speed electro-optic modulators and detachable optical I/O, together with precision wavelength-division multiplexers and advanced packaging features within a unified photonic stack, thereby facilitating co-integration of transmit- and receive-side functionalities on a single platform. This monolithic, CMOS-compatible architecture eliminates the need for module-level assembly of discrete transmit and receive chips, while supporting both fully integrated and standalone photonic deployment across pluggable and co-packaged optical interconnects.

Results

Architecture of a monolithic silicon photonics platform

The ultrafast photodetector demonstrated here is realized on a foundry-qualified 300-mm SiPh platform designed for CMOS compatibility, wafer-scale uniformity, seamless integration, and high-volume manufacturing[44–46]. Figures 1a and 1b show full-wafer and die-level optical images of a 300-mm silicon-on-insulator (SOI) substrate densely populated with photonic and CMOS components, establishing high-volume manufacturability as a design boundary condition rather than an afterthought. Scanning transmission electron micrograph (STEM) images (Fig. 1c–e) further confirm high-fidelity pattern transfer across the photonic layer stack, with the Ge photodetector serving as a representative example elucidating the structural integrity and alignment of the integrated junction, surrounding photonic layers, and backend interconnect stack.

All active and passive photonic components - including the Ge photodetector, pure-Si modulators such as MZMs and micro-ring modulators (MRMs), WDMs, and optical I/Os optimized for O-band datacom and C-band telecom applications - are fabricated without heterogeneous bonding, III-V materials, or exotic add-on layers such as lithium niobate or electro-optic polymers. As shown in the system-level schematic in Fig. 1g, photonic and electronic building blocks are co-integrated on a single Si substrate and interconnected through a shared, yet locally optimized, backend interconnect stack. This architecture contrasts with conventional pluggable transceivers, which typically assemble discrete transmitter and receiver photonic-integrated circuits - often based on different material systems - at the module level rather than integrating both functions on a unified Si platform.

The backend infrastructure features nine levels of metallization jointly optimized for logic density and high-frequency signal integrity, supporting both standalone photonic integrated circuit (PIC) operation and optional monolithic co-integration of electronic integrated circuits (EICs). In addition, the platform

incorporates advanced packaging features, including cavities for flip-chip attachment of lasers[47] and semiconductor optical amplifiers (SOAs), detachable micro-optic couplers, and support for through-silicon vias (TSVs), copper pillars, and optimized copper receive pads, providing a scalable pathway toward 2.5D and 3D integration. These capabilities enable flexible EIC-PIC stacking, allowing the PIC to be coupled to advanced-node CMOS electronics through heterogeneous integration as system requirements evolve (see Supplementary Section Fig.1 for additional details).

For the present ultrafast Ge photodetector demonstrations, the full CMOS-integrated platform and backend interconnect stack are retained, while specific electronic functions (for example, TIAs) are intentionally not exercised to isolate intrinsic photonic device performance. This approach preserves compatibility with advanced electronic-photonic co-integration, while ensuring that the performance reported here does not rely on co-designed electronics and remains portable across a broad range of system architectures.

Ge photodetector architecture and operating regime

The ultrafast Ge photodetector is realized as a lateral Ge-on-Si PIN junction embedded within a crystalline Si waveguide, in which epitaxial Ge is selectively grown in a shallow, waveguide-defined recess to form a compact and lithographically controlled active region. As shown in the STEM cross-section (Fig. 1d-e) and the three-dimensional schematic (Fig. 1f), the absorbing Ge region is laterally confined and optically isolated from the surrounding doped Si, while carefully engineered contact regions enable low-resistance electrical access through silicided Si interfaces and vertically integrated tungsten and copper interconnects, with contacts positioned away from the optical mode. This architecture enables simultaneous realization of ultra-high bandwidth, high responsivity, and robust power handling - an operating regime that has proven difficult to achieve in conventional Ge-on-Si PIN photodetectors. Rather than extending prior ultrahigh-speed approaches that rely primarily on aggressive Ge scaling to improve small-signal bandwidth, this work adopts a device-platform co-optimization strategy that targets system-relevant large-signal operation together with wafer-scale uniformity compatible with high-volume manufacturing.

The Ge active region is engineered to balance optical absorption, junction capacitance, series resistance, and carrier transit time within the monolithic platform. A nominal Ge length of 10 μm and a width of 350 nm are selected to provide sufficient absorption while maintaining operation in a transit-time-limited (rather than RC-limited) regime. This geometry also enables defect-free selective epitaxial growth within Si trenches, avoiding excessive lateral overgrowth that would otherwise compromise crystalline quality and wafer-scale yield. Optical mode overlap with the Ge absorber is maximized through co-designed Si input couplers, while dopant implants are displaced from the Ge region to suppress free-carrier absorption, reduce junction capacitance, and prevent implant-induced defects, enabling near-unity quantum efficiency despite the reduced Ge width. This geometry shortens the effective carrier transit path to support high-speed operation without incurring the responsivity penalties associated with excessively narrow absorbers. The surrounding Si is moderately doped to lower series resistance and

establish a strong electric field across the intrinsic region, which is essential for sustaining bandwidth and suppressing carrier screening at high photocurrent.

DC, small-signal AC characteristics and wafer-scale uniformity

Figure 2 summarizes the wafer-scale electrical and optoelectronic characteristics of the Ge photodetector, measured using a dedicated set of in-line optical test system (ILOTS) macros incorporating ground-signal-ground (GSG) pads for both direct-current (DC) and radio-frequency (RF) characterization at wafer level. This measurement strategy enables high-throughput statistical evaluation directly on 300-mm wafers, providing statistically relevant insight into device uniformity and process control, as detailed in Methods and Supplementary Fig.2-3.

Representative dark current-voltage characteristics (Fig. 2a) exhibit consistently low leakage across the operating reverse-bias range. Full-wafer measurements yield an average dark current of 16 nA (minimum 12 nA, maximum 38 nA) at −1 V) and 52 nA (minimum 32 nA, maximum 107 nA) at −2 V, values that are competitive with state-of-the-art foundry-compatible Ge photodiodes at comparable bandwidth. The corresponding wafer-scale dark-current map (Fig. 2b, Supplementary Fig.4(a)) confirms that low leakage is a reproducible, process-level feature rather than a localized “hero-device” result. Continued optimisation of the Ge module indicates a clear path to reducing the median dark current below 10 nA while further tightening the distribution, addressing increasingly stringent requirements for high-volume receivers targeting pluggable, NPO, and CPO architectures.

To connect DC performance with receiver-relevant operation, Fig. 2c presents bias-dependent photocurrent responses measured at 1310 nm under controlled optical power sweeps, illustrating stable and efficient carrier collection across the relevant bias window. Because responsivity extraction depends critically on accurate calibration of optical power delivered to the photodetector through the grating coupler, multiple mitigation strategies are adopted to minimise systematic uncertainty, as detailed in Supplementary Section S2. Under these measurement and calibration conditions, the device exhibits high responsivity with weak bias dependence. The wafer-scale responsivity map at -2 V (Fig. 2d) shows a median responsivity exceeding 1.01 A W^{-1} across the 300-mm wafer, with peak values approaching ~1.05 A W^{-1}, demonstrating near-unity quantum efficiency. Responsivity values marginally exceeding the theoretical limit arise from residual uncertainties in optical-power calibration and reference normalisation rather than intrinsic gain.

Figure 2e extends this analysis into the high-optical-power regime by plotting responsivity as a function of incident power, demonstrating that conversion efficiency is largely preserved up to 2.8 mW. This behaviour is essential for large-signal reception, where space-charge effects can otherwise distort linearity. Notably, this power-handling capability can be readily doubled to 5.6 mW using a dual-input photodetector architecture, without compromising bandwidth, responsivity, or other key figures of merit. At low optical powers, photocurrent shows minimal dependence on reverse bias, indicating efficient carrier extraction even near zero bias. At higher powers, a finite reverse bias is required to maintain constant responsivity, consistent with field-assisted carrier sweep-out in the Ge PIN junction.

Figures 2f-i quantify the resistance-capacitance (RC) landscape, extracted from independent resistance and capacitance measurements, that determines whether high bandwidth can be preserved at extreme responsivity at manufacturing scale. The series resistance wafer map, determined from forward-biased current-voltage characteristics (Fig. 2a), demonstrates tight control of resistance across the wafer (Fig. 2f). Capacitance derived from S-parameter measurements (Supplementary Fig. 5) remains stable over frequency (Fig. 2g), enabling a consistent parasitic model, while capacitance versus bias (Fig. 2h) shows the expected monotonic reduction with increasing depletion. The capacitance wafer map (Fig. 2i) confirms that these low-capacitance conditions are achieved uniformly across dies, establishing the RC environment required for ultrahigh-speed operation. For the optimized devices, the measured junction capacitance and resistance are approximately 5.7 fF and 48 Ω, corresponding to an RC-limited 3-dB cutoff frequency of ~582 GHz - well above the estimated carrier transit-time limit of ~180-210 GHz - confirming that device operation is firmly transit-time dominated (Supplementary Table 1).

Small-signal frequency-response measurements (Fig. 2j), performed using a 110 GHz lightwave component analyser (Methods and Supplementary Fig.3), show a smooth optoelectronic S21 roll-off without pronounced peaking or resonant artefacts, consistent with an intrinsically bandwidth-limited response rather than circuit-induced extension. Minor oscillations observed at the highest measured frequencies indicate operation approaching the limits of the test system. Bandwidth values exceeding the 110 GHz instrument limit are obtained by fitting the measured S21 response to a physically motivated model, yielding extracted 3-dB bandwidths well beyond the direct measurement range. The corresponding bandwidth wafer map (Fig. 2k) demonstrates that high bandwidth is achieved broadly across the 300-mm SOI substrate, with minimum values exceeding 140 GHz and peak bandwidths reaching 215 GHz at -2V, rather than being confined to individual devices. Figure 2l further shows that bandwidth remains robust as optical input power is increased and degrades only gradually at the highest tested powers. Owing to tester limitations, bandwidth measurements were performed up to ~0.7 mW incident on the photodetector; this operating regime can be naturally extended to 1.4 mW using a dual-input photodetector architecture to accommodate higher optical loading, while preserving other intrinsic device-level performance metrics.

Taken together, Fig. 2 establishes that the photodetector exhibits low dark current, near-unity quantum efficiency, controlled resistance and capacitance, and high intrinsic bandwidth, achieved uniformly at wafer scale on a 300-mm CMOS SiPh platform. These results provide a manufacturable, statistically validated foundation for extreme-speed operation, enabling the large-signal and platform-level demonstrations presented next. In addition to the DC and AC device characteristics discussed here, universal optical return loss (ORL) reduction methodologies have been implemented as detailed in Supplementary Fig.6, enabling back-reflection levels below -35 dB for both the ultra-high-speed photodetectors presented here and lower-speed monitoring photodetectors, thereby exceeding IEEE requirements for pluggable, NPO and CPO interconnect systems[48].

Large-signal operation beyond 448 Gbps

While small-signal optoelectronic bandwidth provides a useful indicator of intrinsic device speed, large-signal performance ultimately determines system-level relevance. Figure 3 summarizes a calibrated set of large-signal eye-diagram measurements spanning modulation formats and data rates, obtained using a measurement framework based on a 224-GBaud arbitrary waveform generator (AWG) driving an external reference modulator (Fig. 3a). The resulting optical waveform is detected by the photodetector under test and analysed using a sampling oscilloscope with explicitly defined electrical drive and photodetector output reference planes. This calibration strategy ensures that the measured eye openings reflect the intrinsic large-signal response of the photodetector rather than artefacts arising from instrumentation, interconnects, or reference-plane ambiguity. Full details of the waveform generation, calibration, and measurement procedures are provided in Methods and Supplementary Section S2.

At lower modulation complexity, clean non-return-to-zero (NRZ) eye openings at 200 Gbps and 224 Gbps (Fig. 3b,c) indicate low-jitter operation at moderate symbol rates. Transitioning to multilevel modulation, PAM4 eye diagrams at 400 Gbps and 448 Gbps (Fig. 3d,e) establish direct compatibility with contemporary ≥400- Gbps -per-lane system targets, achieved without reliance on avalanche gain[49] or inductive peaking[39–41]. At higher modulation orders, the photodetector continues to demonstrate robust signal integrity at high data rates. Figures 3f-j show PAM6 and PAM8 operation extending beyond 448 Gb s^{-1} per wavelength, illustrating that the underlying detector architecture sustains large-signal operation at symbol rates exceeding those implied by small-signal bandwidth alone. All eye diagrams were acquired at elevated optical power conditions corresponding to photocurrents of ~2 mA, representing a regime broadly consistent with IEEE-relevant receiver operating conditions under high-power scenarios[48]. These measurements highlight the available performance headroom of the device under large-signal excitation, while maintaining clear eye separation under higher-order modulation formats. To the best of our knowledge, this constitutes the highest demonstrated ≥448-Gbps-class large-signal reception in a Ge-on-Si photodetector realised within a 300-mm monolithic SiPh foundry platform, advancing beyond prior reports that primarily emphasise small-signal bandwidth or substantially lower-rate large-signal operation.

All large-signal data reported here are obtained from direct photodetector measurements performed without TIA, thereby probing the intrinsic optoelectronic response of the Ge photodetector under large-signal conditions - an experimental configuration rarely explored at these data rates. While the present results already demonstrate robust large-signal operation at and beyond 448 Gbps per wavelength using external instrumentation, further improvements in signal margin and system robustness are expected through optimised electrical interfaces and dedicated TIA co-integration within the same platform.

Benchmarking and system-level relevance

Figures 4a and 4b present a consolidated benchmarking of the Ge-on-Si photodetector against representative state-of-the-art photodetectors based on III-V, germanium, plasmonic and graphene

materials integrated with silicon waveguide platforms[5,34,37,38–42,50–53]. Rather than highlighting isolated performance metrics, this comparison evaluates a system-relevant set of figures of merit - including large-signal data rate, bandwidth, responsivity, bandwidth-responsivity product, and dark current - considered collectively. Within this framework, prior ultrafast Ge photodiodes report bandwidth–responsivity products of ~108 GHz·A W^{-1} for a 265 GHz Ge fin device and ~105 GHz·A W^{-1} for a recent 100 GHz ultrathin Ge photodetector, whereas the present device exceeds 217 GHz·A W^{-1}, representing an approximately twofold improvement over previous state-of-the-art demonstrations.

Viewed in aggregate, the device delivers leading large-signal performance together with state-of-the-art bandwidth and high responsivity, while maintaining low dark current. Notably, these attributes are achieved on a 300-mm monolithic, CMOS-compatible silicon photonics platform, with the reported performance reflecting wafer-scale statistics rather than selected laboratory devices - highlighting a level of manufacturability and integration maturity not typically demonstrated in prior high-performance reports.

The normalized radar plot in Fig. 4b further reinforces this multi-metric balance: the present photodetector extends toward the outer boundary across all axes, enclosing the largest area among the compared devices and indicating a consistently high level of performance across the key figures of merit. This contrasts with prior approaches - based on aggressive Ge scaling, plasmonic confinement, avalanche gain or resonant enhancement - which often trade responsivity, linearity, dark current, or stability for peak performance in a single dimension.

Monolithic Integration of Transmit and Receive Functions

Building on the demonstrated wafer-scale manufacturability and system-relevant performance of the Ge photodetector, we examine how this receiver capability is leveraged within the SiPh platform to realize closely matched transmit, receive, wavelength routing, and optical interfacing functions. As per-lane data rates scale toward and beyond 400 Gbps across pluggable modules (DR and FR), as well as NPO and CPO, achieving balanced transmitter and receiver performance within a foundry-compatible photonics stack becomes increasingly challenging. Here we address this challenge through monolithic integration of high-speed modulators, scalable cWDM, and packaging-ready optical interfaces.

High-speed all-silicon Mach-Zehnder modulators

MZMs are widely deployed in commercial pluggable transceivers owing to their linearity and robustness; however, scaling toward ≥400 Gbps becomes increasingly difficult due to RC loading and stringent drive requirements, particularly in contrast to compact, Q-factor-limited resonant modulators. Figures 5a and 5b show high-speed, all-silicon MZMs employing S-type junction engineering co-integrated with the Ge photodetector. As shown in Fig. 5c, a 400 Gbps PAM4 eye diagram demonstrates ≥400 Gbps-class transmit-side operation, establishing transmitter capability commensurate with the demonstrated receiver performance.

Scalable WDM with tight wavelength control

System-level scaling is further supported by passive cWDM components implemented using high-quality PECVD SiN. As shown in Figs. 5d-f, optimized WDM structures exhibit <1.5 nm wafer-level channel variability - reduced from >10 nm through improved SiN film uniformity and critical-dimension control - while compact path-length merging in bend regions reduces footprint. Together, these features enable bandwidth scaling through WDM while maintaining tighter system guardbands and high manufacturing yield.

Packaging-ready broadband low-loss detachable optical I/O

Scalable optical interfacing is enabled by cavity-integrated, micro-optic-assisted surface coupling solutions, as shown in Figs. 5g–i. These detachable interfaces, developed in conjunction with advanced micro-optic technologies, provide broadband, low-loss coupling approaching ~1 dB per facet across the entire O-band while substantially relaxing lateral and angular alignment tolerances. Importantly, the cavity-assisted architecture enables wafer-level optical testing prior to singulation, supporting early yield screening and simplified assembly flows for high-density optical I/O in both NPO and CPO. The robustness of this approach is further confirmed by insertion-loss measurements before and after permanent adhesive alignment (Supplementary Fig. 7), which show no measurable degradation, indicating stable optical coupling and readiness for final deployment in optical engine architectures.

Discussion and outlook

This work demonstrates that Ge-on-Si photodetectors, when co-optimized within a scalable SiPh platform, can simultaneously achieve best-in-class DC performance, ultrahigh small-signal bandwidth, and record-class large-signal operation while remaining compatible with high-volume manufacturing. Whereas prior Ge and Ge/Si photodetector studies have largely emphasized small-signal bandwidth as a device-physics benchmark, they have often not addressed the coupled requirements of large-signal operation, optical power handling, and wafer-scale uniformity that ultimately determine system-level viability.

By realizing high large-signal data rates together with strong responsivity and leading small-signal bandwidth in a CMOS-compatible, wafer-scale process, this work bridges the gap between research-laboratory demonstrations and deployable optical interconnect technologies. The results show that large-signal performance need not come at the expense of efficiency, bandwidth, or manufacturability, but can instead be achieved through device-platform co-optimization, marking a transition from isolated device scaling toward system-relevant performance.

Beyond the receiver itself, the demonstrated platform integrates high-speed transmit-side modulators, scalable wavelength-division multiplexing, and packaging-ready optical I/O. This level of integration shifts high-speed silicon photonics from a device-centric paradigm toward system readiness, in which receivers, transmitters, passives, and optical I/O are jointly engineered for scalability, yield, and

reproducibility. Demonstration in a 300-mm manufacturing environment underscores wafer-scale uniformity as a first-order constraint at extreme data rates and establishes a credible path from laboratory prototypes to high-volume deployment.

At the system level, the demonstrated ≥400 Gbps-class per-lane receiver performance provides a direct route to multi-terabit aggregate bandwidth through wavelength-multiplexed architectures, encompassing both coarse and dense WDM. When combined with cWDM and dWDM techniques, such per-lane data rates naturally scale to 3.2 Tbps, 6.4 Tbps, and beyond, without requiring fundamental changes to the underlying device or platform technology.

Looking forward, the demonstrated receiver headroom beyond 448 Gbps provides margin for higher-order modulation formats, increased wavelength counts, and tighter electronic-photonic co-design, while preserving compatibility with scalable manufacturing. Near-term opportunities include monolithic TIA integration and joint device-circuit optimization, together with extended reliability and environmental qualification. More broadly, the scalable device-platform co-optimization principles established here provide a foundation for future photodetector architectures that combine large-signal system performance with high-volume SiPh manufacturability.

Methods

Design and fabrication

The ultra-fast photodetector and other photonic device simulations were performed using ANSYS Lumerical tools and Sentaurus TCAD benchdeck, whereas the testing circuit followed a design flow using Cadence Virtuoso. The finalized design was verified against foundry design rules using Calibre. The demonstrated integrated photodetector was fabricated using GlobalFoundries' 45SPCLO 300-mm silicon photonics platform, which enables monolithic integration of photonic devices with 45-nm silicon-on-insulator RF CMOS electronics. Most of the photonic devices in the test chips were based on the foundry's standard process design kit, with ultra-fast photodetector design-of-experiments included in ILOTs packages for systematic characterization of small- and large-signal, DC and AC performance metrics reported in the paper. No additional process masks or steps were introduced to form the ultra-fast photodetector. Photodetector, modulator, and cWDM devices were measured at wafer level via grating couplers, while detachable I/O measurements were performed at module level with micro-optics units attached to a cavity formed during the wafer fabrication.

DC measurement

Dark current and photocurrent measurements were performed at wafer level using the in-line optical test system (ILOTs) with GSG probe pads, under reverse bias conditions of -1 V and -2 V. Responsivity was calibrated using multiple independent approaches to account for grating coupler insertion loss variability (see Supplementary S2 (Fig.2) for full calibration methodology).

Small-signal RF measurement

The devices were equipped with ground-signal-ground (GSG) pads (90 μm by 60 μm) with pitches of 100 μm to match the requirements of the respective radio-frequency probes in the lightwave component analyser (LCA) and eye diagram measurement setups. Small-signal optoelectronic S-parameters were measured using a Keysight N5227B vector network analyser with an integrated 110 GHz lightwave component analyser (N4372E). A three-step electrical calibration procedure was applied: (i) open-short-load cable/LCA calibration, (ii) precision calibration substrate for RF probe de-embedding, and (iii) on-chip open/shorted pad-set de-embedding of the metal stack and dielectric environment. The 3-dB optoelectronic bandwidth was extracted from the measured |S21| response under -2 V and -1V DC bias (see Supplementary S2 (Fig.3) for full setup details).Two-port S-parameter measurements were used to extract the device capacitance; details are provided in Supplementary Section S3 (Fig.5).

Large-signal RF measurement

Large-signal eye diagram measurements were performed at -2 V reverse bias. NRZ and PAM4 data at 200-448 Gbps were generated using a Keysight 120 GBaud pattern generator/reference transmitter and captured with a high-speed sampling oscilloscope. For higher-order modulation (PAM6, PAM8, up to 520 Gbps), a 224 GBaud arbitrary waveform generator (Keysight M8199A) was used to generate the test signals, with digital pre-emphasis applied to compensate transmitter bandwidth limitations. The photodetector output was acquired through a calibrated reference receiver, with all eye diagrams representing averages of 32 pattern repeats from which outer modulation amplitude and signal quality statistics were extracted**.**

Declarations

Acknowledgements

We acknowledge Kevin Soukup, Rick Carter, Thomas Barber, Vikas Gupta, Radhika Arora, Patrick Lo, Gregg Bartlett, Ted Letavic and the rest of the GlobalFoundries engineering team for discussions and contributions to silicon photonics technologies. We extend special thanks to the Fab 9 test team and modeling lab for comprehensive measurement support. We also would like to thank Senko Advanced Components for the great partnership and Fabrinet for the measurement support for detachable I/O. Last but not least, we want to thank Prof. Kimerling, Prof. Michel from MIT and Prof. Shujie Yang from University of Pennsylvania for useful discussions on the manuscript.

Author contributions

Y.B. initiated and supervised the project. Y.B., S.C., W.S.L, Q.L. and A.A. designed the photodetectors and created layouts for the devices and test structures. Y.B., S.C. and M.B. performed Lumerical and TCAD modeling of the devices. M.Z., H.L.W, J.H., J.A., A.S., and R.S. fabricated the devices. B. P. collected photos, SEM and TEM images for the photodetectors. T.S., H.D., J.G., Q.L., A.A., S.B. C.H. E.S. performed

extensive electrical, optical, and optoelectrical characterization of the photodetectors. S.C., Q.L., A.A., Y.B. , W.S.L, S.P. and M.S. analyzed the DC and AC results. M.R., S.C., W.S.L, Y.B. J.G., B.M. and M.S. designed and analyzed the nitride passives and cWDM. M.G., K. D., S.C., Q.L., A.A., W.S.L., Y.B., B.M. and M.S. designed and analyzed modulator performance. Y.B., T. H. and K.D. designed the I/O spot size converter and cavity. Z.C., K.R., J.K. and K. G. contributed to the assembly and collected insertion loss data for detachable I/O. All authors including L.C., G.R., K.B. and J.E.B. contributed significantly to the writing and discussion of the manuscript.

Competing interests statement

L.C. cofounded Dream Photonics. K.B. cofounded Xscape Photonics. J.E.B. cofounded Nexus Photonics and Quintessent.

References

1. Shastri, B. J. *et al.* Photonics for artificial intelligence and neuromorphic computing. *Nat. Photonics* **15**, 102–114 (2021).
2. Khani, M. *et al.* SiP-ML: high-bandwidth optical network interconnects for machine learning training. in *Proceedings of the 2021 ACM SIGCOMM 2021 Conference* 657–675 (Association for Computing Machinery, New York, NY, USA, 2021). doi:10.1145/3452296.3472900.
3. Margalit, N. *et al.* Perspective on the future of silicon photonics and electronics. *Appl. Phys. Lett.* **118**, 220501 (2021).
4. Michel, J., Liu, J. & Kimerling, L. C. High-performance Ge-on-Si photodetectors. *Nat. Photonics* **4**, 527–534 (2010).
5. Lischke, S. *et al.* Ultra-fast germanium photodiode with 3-dB bandwidth of 265 GHz. *Nat. Photonics* **15**, 925–931 (2021).
6. Shi, Y. *et al.* Avalanche photodiode with ultrahigh gain–bandwidth product of 1,033 GHz. *Nat. Photonics* **18**, 610–616 (2024).
7. Zhou, X., Lam, C. F., Urata, R. & Liu, H. State-of-the-Art 800G/1.6T Datacom Interconnects and Outlook for 3.2T. in *Optical Fiber Communication Conference (OFC) 2023 (2023), paper W3D.1* W3D.1 (Optica Publishing Group, 2023). doi:10.1364/OFC.2023.W3D.1.
8. Soref, R. The Past, Present, and Future of Silicon Photonics. *IEEE J. Sel. Top. Quantum Electron.* **12**, 1678–1687 (2006).
9. Rickman, A. The commercialization of silicon photonics. *Nat. Photonics* **8**, 579–582 (2014).
10. Thomson, D. *et al.* Roadmap on silicon photonics. *J. Opt.* **18**, 073003 (2016).
11. Shekhar, S. *et al.* Roadmapping the next generation of silicon photonics. *Nat. Commun.* **15**, 751 (2024).
12. Reed, G. T., Mashanovich, G., Gardes, F. Y. & Thomson, D. J. Silicon optical modulators. *Nat. Photonics* **4**, 518–526 (2010).

13. Rahim, A. *et al.* Taking silicon photonics modulators to a higher performance level: state-of-the-art and a review of new technologies. *Adv. Photonics* **3**, 024003 (2021).
14. Wade, M. *et al.* An Error-free 1 Tbps WDM Optical I/O Chiplet and Multi-wavelength Multi-port Laser. in *Optical Fiber Communication Conference (OFC) 2021* F3C.6 (Optica Publishing Group, Washington, DC, 2021). doi:10.1364/OFC.2021.F3C.6.
15. Bian, Y. *et al.* Monolithically integrated self-aligned SiN edge coupler with <0.6/0.8 dB TE/TM insertion loss, <-39 dB back reflection and >520 mW high-power handling capability. in *Optical Fiber Communication Conference (OFC) 2023* M3C.3 (Optica Publishing Group, San Diego California, 2023). doi:10.1364/OFC.2023.M3C.3.
16. He, M. *et al.* High-performance hybrid silicon and lithium niobate Mach–Zehnder modulators for 100 Gbit s−1 and beyond. *Nat. Photonics* **13**, 359–364 (2019).
17. Wang, C. *et al.* Integrated lithium niobate electro-optic modulators operating at CMOS-compatible voltages. *Nature* **562**, 101–104 (2018).
18. Weigel, P. O. *et al.* Bonded thin film lithium niobate modulator on a silicon photonics platform exceeding 100 GHz 3-dB electrical modulation bandwidth. *Opt. Express* **26**, 23728–23739 (2018).
19. Berikaa, E., Alam, M. S. & Plant, D. V. Net 400-Gbps/λ IMDD transmission using a single-DAC DSP-free transmitter and a thin-film lithium niobate MZM. *Opt. Lett.* **47**, 6273–6276 (2022).
20. Rahman, A. *et al.* High-performance Hybrid Lithium Niobate Electro-optic Modulators Integrated with Low-loss Silicon Nitride Waveguides on a Wafer-scale Silicon Photonics Platform. Preprint at https://doi.org/10.48550/arXiv.2504.00311 (2025).
21. Shen, B. *et al.* Fully Integrated 1064 nm Transmitters With Widely Tunable GaAs Lasers and > 100-GHz Thin-Film LiNbO3 Modulators. in *Optical Fiber Communication Conference (OFC) 2026 (2026), paper Th4A.5* Th4A.5 (Optica Publishing Group, 2026).
22. Cai, J. *et al.* Heterogeneously integrated lithium tantalate-on-silicon nitride modulators for high-speed communications. *Nat. Commun.* **17**, 3314 (2026).
23. Wang, C. *et al.* Lithium tantalate photonic integrated circuits for volume manufacturing. *Nature* **629**, 784–790 (2024).
24. Xu, M., Lan, Y., Che, D., Shi, J. & Liang, D. C-Band 110-GHz-Bandwidth Thin-Film Lithium Tantalate Modulator Enabling 768 (536) Gbit/s Line (Net) Data Rates. in *Optical Fiber Communication Conference (OFC) 2026 (2026), paper Th4A.3* Th4A.3 (Optica Publishing Group).
25. Taghavi, I. *et al.* Polymer modulators in silicon photonics: review and projections. *Nanophotonics* **11**, 3855–3871 (2022).
26. Schwarzenberger, A. *et al.* Silicon-Organic Hybrid (SOH) Mach–Zehnder Modulators (MZM) for Single-Carrier IM/DD Line Rates of 500 Gbit/s and Beyond. *J. Light. Technol.* **44**, 1030–1046 (2026).
27. Ummethala, S. *et al.* THz-to-optical conversion in wireless communications using an ultra-broadband plasmonic modulator. *Nat. Photonics* **13**, 519–524 (2019).

28. Eppenberger, M. *et al.* Resonant plasmonic micro-racetrack modulators with high bandwidth and high temperature tolerance. *Nat. Photonics* **17**, 360–367 (2023).
29. Giboney, K. S. *et al.* Travelling-wave photodetectors with 172-GHz bandwidth and 76-GHz bandwidth-efficiency product. *IEEE Photonics Technol. Lett.* **7**, 412–414 (1995).
30. Li, L. *et al.* Modified uni-travelling-carrier photodiodes with 206 GHz bandwidth and 0.81 A W−1 external responsivity. *Nat. Photonics* **19**, 1301–1308 (2025).
31. Qin, S. *et al.* Micro-transfer printing of O-band InGaAs/InP photodiodes on a silicon nitride photonic platform. *Opt. Express* **33**, 34153–34169 (2025).
32. Muthuganesan, H. *et al.* 100 Gbps PAM4 ultra-thin photodetectors integrated on SOI platform by micro transfer printing. *Opt. Express* **31**, 36273–36280 (2023).
33. Guo, X. *et al.* Heterogeneous integration of GaInAsSb–GaSb photodiodes on SOI photonic integrated circuits for SWIR applications. *Opt. Lett.* **50**, 89–92 (2025).
34. Wen, P. *et al.* Waveguide coupled III-V photodiodes monolithically integrated on Si. *Nat. Commun.* **13**, 909 (2022).
35. Mauthe, S. *et al.* High-speed III-V nanowire photodetector monolithically integrated on Si. *Nat. Commun.* **11**, 4565 (2020).
36. Xue, Y. *et al.* High-performance III-V photodetectors on a monolithic InP/SOI platform. *Optica* **8**, 1204–1209 (2021).
37. Xue, Y. *et al.* High-speed and low dark current silicon-waveguide-coupled III-V photodetectors selectively grown on SOI. *Optica* **9**, 1219–1226 (2022).
38. Shahin, A. *et al.* Beyond 100 GHz, High Responsivity, Waveguide-Coupled Deeply Recessed Germanium on Silicon Photodiode. in *2025 30th OptoElectronics and Communications Conference (OECC) and 2025 International Conference on Photonics in Switching and Computing (PSC)* 1–3 (2025). doi:10.23919/OECC/PSC62146.2025.11111517.
39. Shi, Y., Li, X., Zou, M., Yu, Y. & Zhang, X. 103 GHz germanium-on-silicon photodiode enabled by an optimized U-shaped electrode. *Photonics Res.* **12**, 1–6 (2024).
40. Chen, W. *et al.* High-performance compact vertical germanium photodiodes enabled by silicon corner reflectors. *Photonics Res.* **12**, 2983–2988 (2024).
41. Zou, M., Shi, Y., Li, Z., Yu, Y. & Zhang, X. Ultra-Compact Lateral Junction Germanium Photodiode with a Bandwidth of 136 GHz. *ACS Photonics* **12**, 6698–6704 (2025).
42. Wang, X. *et al.* 100 GHz bandwidth ultra-thin germanium photodetectors with high responsivity on a 300 mm silicon photonics process. *Optica* **13**, 67–73 (2026).
43. Shi, Y., Zou, M., Li, Z., Yu, Y. & Zhang, X. Ultrafast avalanche photodiode exceeding 100 GHz bandwidth. *Nat. Commun.* **16**, 11058 (2025).
44. Stojanović, V. *et al.* Monolithic silicon-photonic platforms in state-of-the-art CMOS SOI processes [Invited]. *Opt. Express* **26**, 13106–13121 (2018).

45. Giewont, K. *et al.* 300-mm Monolithic Silicon Photonics Foundry Technology. *IEEE J. Sel. Top. Quantum Electron.* **25**, 1–11 (2019).
46. Bian, Y. *et al.* 300-mm monolithic CMOS silicon photonics foundry technology [Invited]. in *CLEO 2024 (2024), paper ATu3H.1* ATu3H.1 (Optica Publishing Group, 2024). doi:10.1364/CLEO_AT.2024.ATu3H.1.
47. Bian, Y. *et al.* 3D Integrated Laser Attach Technology on a 300-mm Monolithic CMOS Silicon Photonics Platform. *IEEE J. Sel. Top. Quantum Electron.* 1–19 (2023) doi:10.1109/JSTQE.2023.3238290.
48. IEEE Standard for Ethernet - Amendment 3: Media Access Control Parameters for 50 Gb/s and Physical Layers and Management Parameters for 50 Gb/s, 100 Gb/s, and 200 Gb/s Operation. *IEEE Std 8023cd-2018 Amend. IEEE Std 8023-2018 Amend. IEEE Std 8023cb-2018 IEEE Std 8023bt-2018* 1–401 (2019) doi:10.1109/IEEESTD.2019.8649797.
49. Xiang, Y., Cao, H., Liu, C., Guo, J. & Dai, D. High-speed waveguide Ge/Si avalanche photodiode with a gain-bandwidth product of 615 GHz. *Optica* **9**, 762–769 (2022).
50. Chen, H. *et al.* −1 V bias 67 GHz bandwidth Si-contacted germanium waveguide p-i-n photodetector for optical links at 56 Gbps and beyond. *Opt. Express* **24**, 4622–4631 (2016).
51. Wang, X. *et al.* Silicon Nitride Waveguide-Integrated Ge Photodetector with >110 GHz Bandwidth under 1 mA Operation in the O-Band. *ACS Photonics* https://doi.org/10.1021/acsphotonics.5c02939 (2026) doi:10.1021/acsphotonics.5c02939.
52. Salamin, Y. *et al.* 100 GHz Plasmonic Photodetector. *ACS Photonics* **5**, 3291–3297 (2018).
53. Ma, P. *et al.* Plasmonically Enhanced Graphene Photodetector Featuring 100 Gbit/s Data Reception, High Responsivity, and Compact Size. *ACS Photonics***6**, 154–161 (2019).

Figures

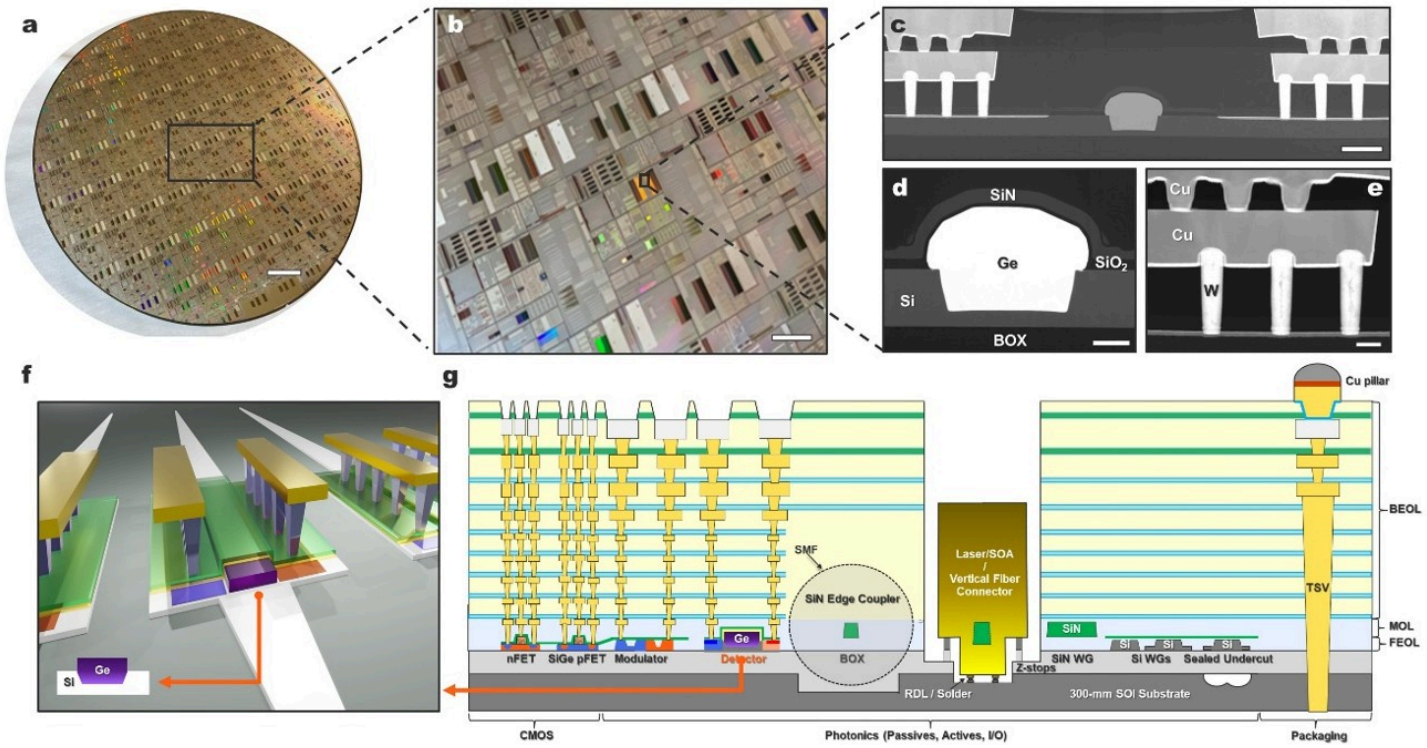


Figure 1

Wafer-scale monolithic integration of ultrahigh-speed Ge-on-Si photodetectors on a CMOS silicon photonics platform.

a, Photograph of a fabricated 300-mm silicon-on-insulator wafer, illustrating wafer-scale integration of Ge photodetectors with dense passive and active silicon photonic components, as well as advanced CMOS devices across the full substrate. **b,** Optical micrograph of representative silicon photonics and CMOS dies. **c,** Cross-sectional scanning transmission electron micrograph (STEM) of a complete Ge photodetector, showing the Ge-on-Si junction, lateral PIN structure and electrical contacts extending through the interconnect stack up to the M2 metallization level. **d,** Higher-magnification STEM image of the Ge active region partially embedded within the silicon waveguide, revealing the laterally confined Ge absorption region, surrounding silicon, and dielectric encapsulation. **e,** Higher-magnification STEM image of the electrical contact region, highlighting tungsten contacts and copper interconnects that provide vertical routing for high-frequency electrical access. **f,** Three-dimensional schematic of the lateral Ge-on-Si PIN photodetector, illustrating the optical input taper, intrinsic absorption region and electrical contacts (schematic not to scale). **g,** Cross-sectional schematic of the monolithic CMOS-compatible silicon photonics platform, showing single-substrate integration of Ge photodetectors with CMOS electronics, modulators, passive photonic components, optical I/O structures and advanced packaging features, including through-silicon vias (TSVs), copper pillars, laser and fiber attach as well as detachable I/Os, enabling both standalone photonic integrated circuits and electronic-photonic co-integration (schematic not to scale). **Scale bars:** 3 cm (a); 1 cm (b); 300 nm (c); 100 nm (d); 100 nm (e).

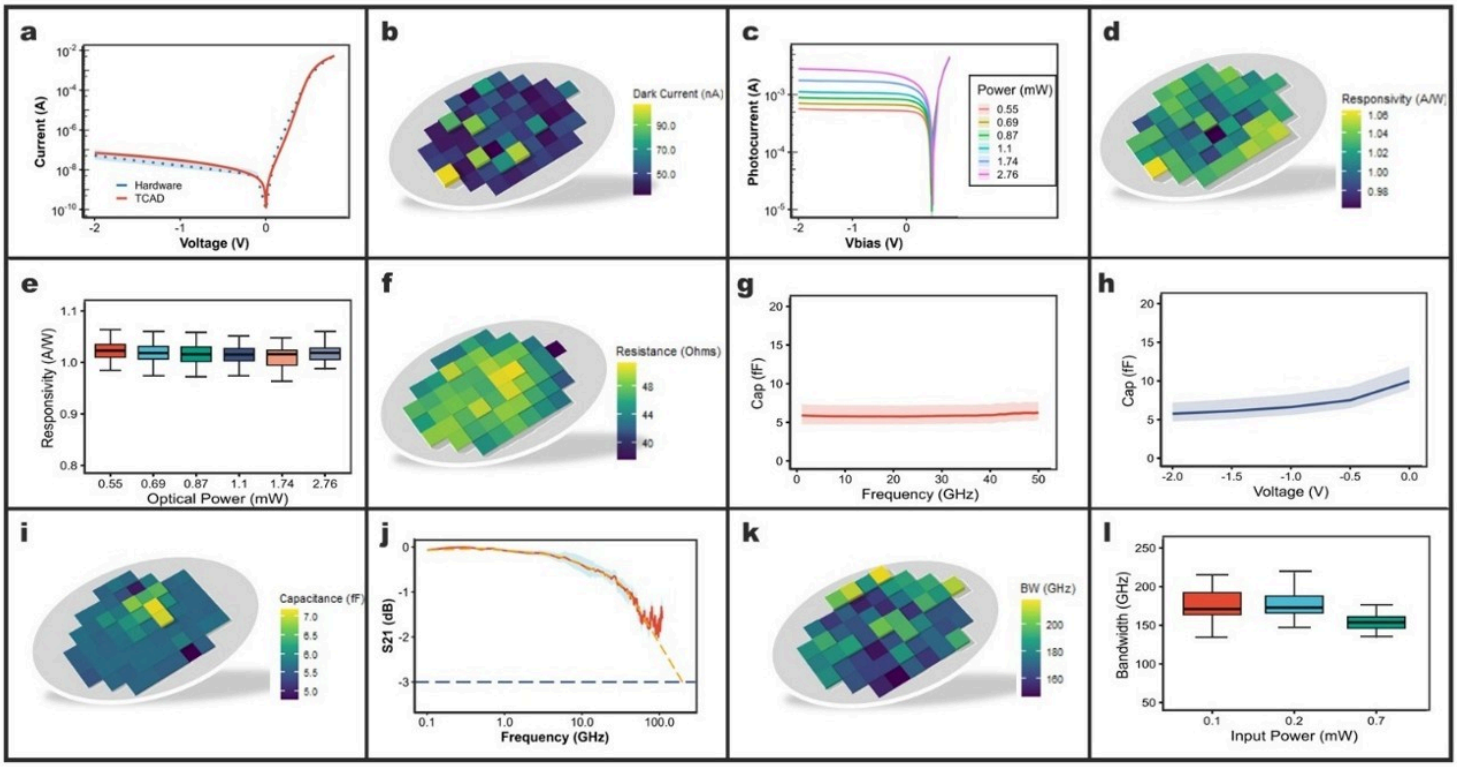


Figure 2

Wafer-scale electrical and optoelectronic performance of ultrafast Ge-on-Si lateral PIN photodetectors.

a, Dark-current-voltage (I-V) characteristics of representative Ge photodetectors measured across the reverse-bias range, with TCAD simulations overlaid using a trap-assisted generation-recombination model calibrated to the measured leakage. b, Wafer map of dark current across the 300 mm SOI substrate, showing low leakage and tight wafer-scale uniformity. c, Bias-dependent photocurrent measured under multiple input optical powers, demonstrating stable carrier collection across the operating bias range. d, Wafer map of responsivity at the target bias and wavelength, showing median values exceeding ~1.01 A W^{-1} across the wafer. e, Responsivity as a function of optical input power, indicating stable operation up to ~2.8 mW without abrupt saturation. f, Wafer map of extracted series resistance from forward-biased dark current I-V curve, confirming well-controlled electrical resistance across dies. g, Capacitance as a function of frequency, exhibiting stable values over the measurement band. h, Capacitance as a function of reverse bias, showing the expected depletion-driven reduction. i, Wafer-scale capacitance map, confirming reproducible low-capacitance operation. j, Representative small-signal optoelectronic frequency response (S21), showing smooth roll-off without resonant peaking within the measurement bandwidth. k, Wafer map of extracted 3-dB optoelectronic bandwidth, demonstrating consistent high-speed performance across the 300 mm SOI wafer. l, Optoelectronic bandwidth as a function of input optical power, showing gradual roll-off at elevated photocurrent; measurements are limited by the available test range.

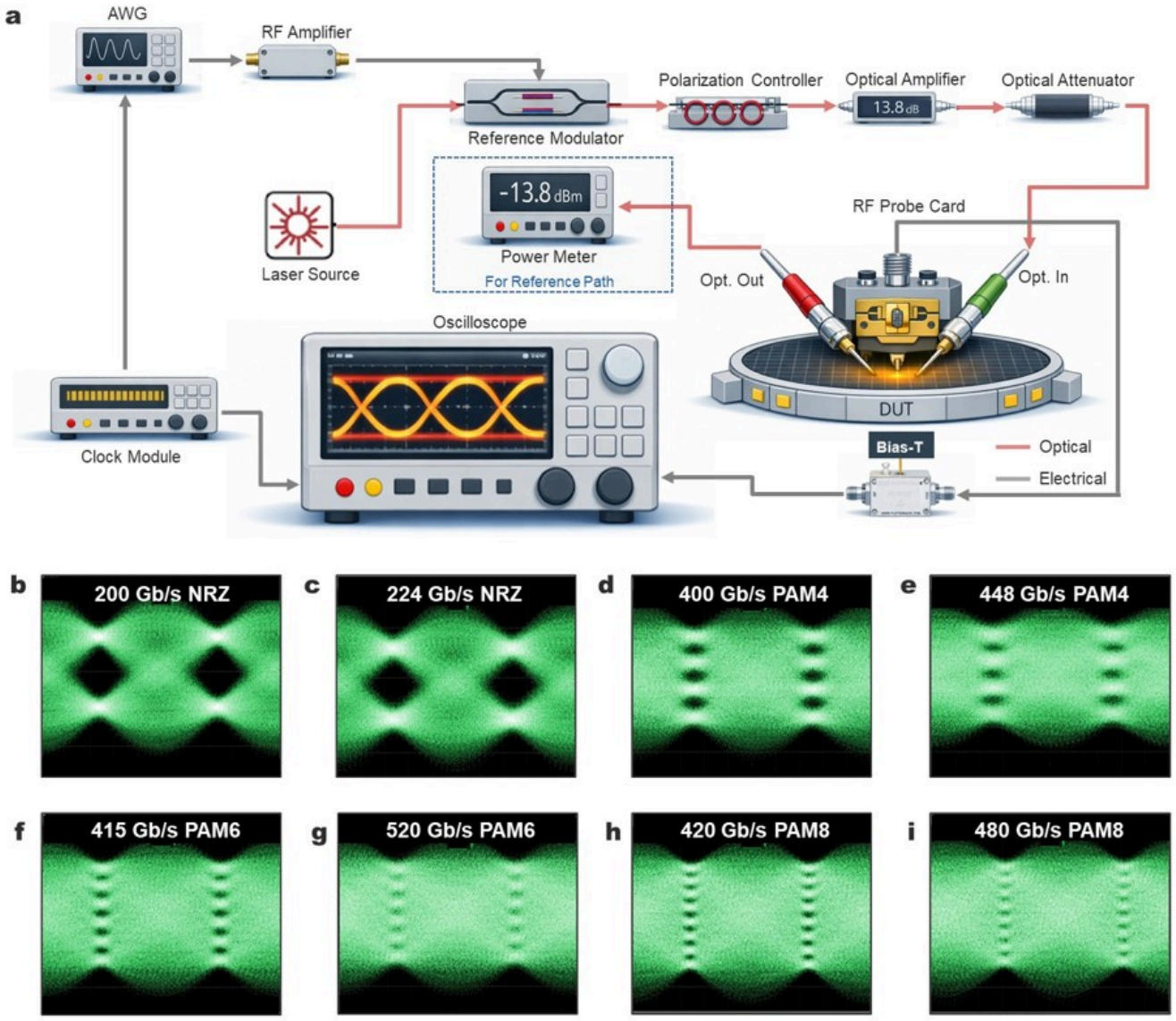
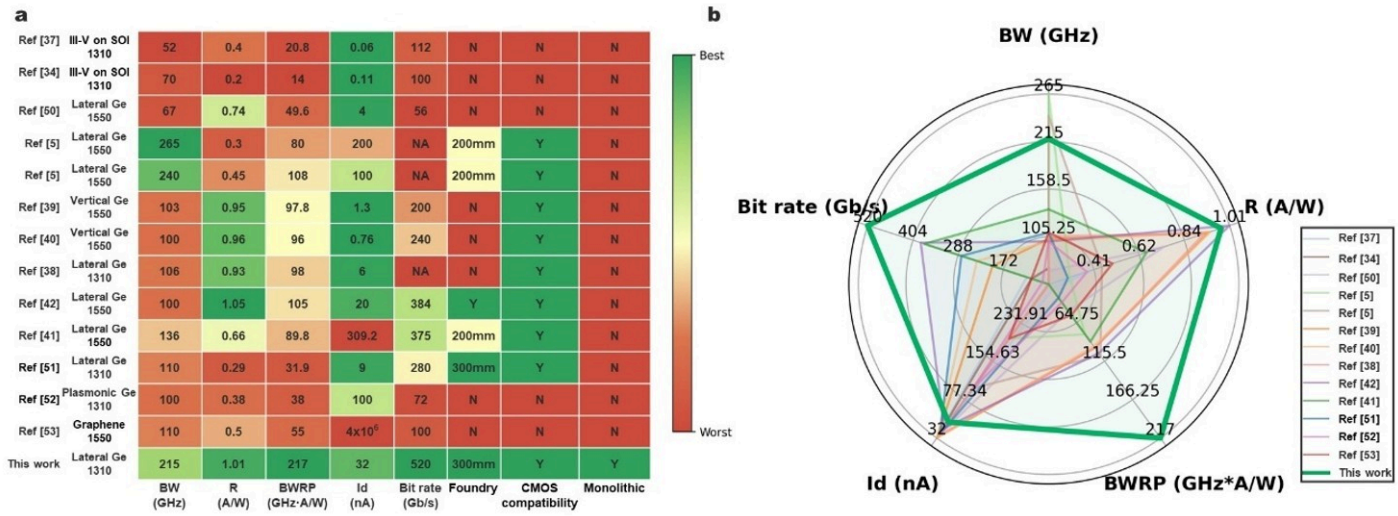


Figure 3

Large-signal receiver operation of Ge-on-Si lateral PIN photodetectors.

a, Schematic of the large-signal measurement configuration used to evaluate photodetector performance, including optical modulation, polarization control, amplification, attenuation, device biasing and electrical signal capture (schematic not to scale). b,c, Measured non-return-to-zero (NRZ) eye diagrams at 200 Gbps (b) and 224 Gbps (c), showing clear signal separation at moderate symbol rates. d,e, Measured PAM4 eye diagrams at 400 Gbps (d) and 448 Gbps (e), demonstrating ≥400 Gbps-class receiver operation consistent with system-relevant data rates. f,g, Measured PAM6 eye diagrams at 415 Gbps (f) and 520 Gbps (g), showing discernible multilevel modulation features at elevated data rates. h,i, Measured PAM8 eye diagrams at 420 Gbps (h) and 480 Gbps (i), illustrating continued signal structure under higher-order modulation. All eye diagrams are obtained using the integrated photodetector in a standalone photonic-integrated-circuit configuration, without avalanche gain or

transimpedance-amplifier (TIA) integration, reflecting intrinsic large-signal device performance under the specified measurement conditions (see Methods).



		BW (GHz)	R (A/W)	BWRP (GHz·A/W)	Id (nA)	Bit rate (Gb/s)	Foundry	CMOS compatibility	Monolithic
Ref [37]	III-V on SOI 1310	52	0.4	20.8	0.06	112	N	N	N
Ref [34]	III-V on SOI 1310	70	0.2	14	0.11	100	N	N	N
Ref [50]	Lateral Ge 1550	67	0.74	49.6	4	56	N	N	N
Ref [5]	Lateral Ge 1550	265	0.3	80	200	NA	200mm	Y	N
Ref [5]	Lateral Ge 1550	240	0.45	108	100	NA	200mm	Y	N
Ref [39]	Vertical Ge 1550	103	0.95	97.8	1.3	200	N	Y	N
Ref [40]	Vertical Ge 1550	100	0.96	96	0.76	240	N	Y	N
Ref [38]	Lateral Ge 1310	106	0.93	98	6	NA	N	Y	N
Ref [42]	Lateral Ge 1550	100	1.05	105	20	384	Y	Y	N
Ref [41]	Lateral Ge 1550	136	0.66	89.8	309.2	375	200mm	Y	N
Ref [51]	Lateral Ge 1310	110	0.29	31.9	9	280	300mm	Y	N
Ref [52]	Plasmonic Ge 1310	100	0.38	38	100	72	N	N	N
Ref [53]	Graphene 1550	110	0.5	55	$4x10^6$	100	N	N	N
This work	Lateral Ge 1310	215	1.01	217	32	520	300mm	Y	Y

Figure 4

Benchmarking of Ge-on-Si photodetectors against representative on-chip photodetectors.
a, Literature benchmarking of waveguide-integrated photodetectors across key figures of merit, including 3-dB optoelectronic bandwidth, optical responsivity, bandwidth-responsivity product, dark current and reported large-signal data rate, together with platform-level attributes such as foundry compatibility, CMOS integration and 300-mm manufacturing scale. Representative Ge, III-V, plasmonic and graphene photodetectors implemented for integrated receiver applications are included for comparison, alongside the device demonstrated in this work. Metrics are shown as reported in the respective publications. Absolute responsivity values are presented for completeness; however, direct comparison between O- and C-band operation should be interpreted with care, as for a given quantum efficiency the responsivity scales with wavelength and is therefore intrinsically higher at longer wavelengths. Within this context, the present device demonstrates among the highest reported effective quantum efficiency across the compared platforms. **b,**Radar plot comparing normalized photodetector performance across five metrics (bandwidth, responsivity, bandwidth–responsivity product, dark current and large-signal data rate), illustrating the balanced and simultaneous performance of the Ge-on-Si photodetector relative to representative on-chip photodetectors.

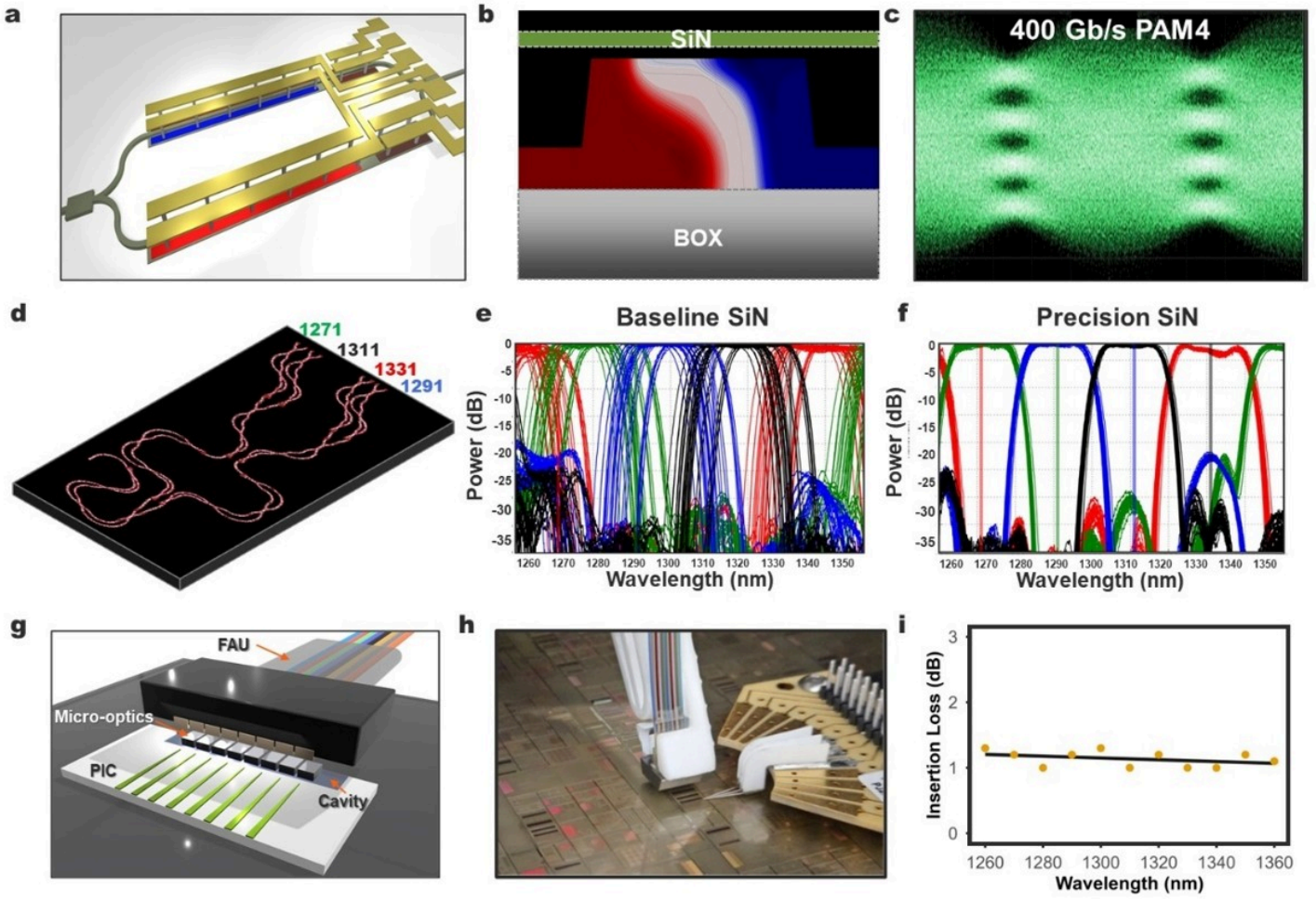


Figure 5

Monolithic silicon photonics platform capabilities, including modulators, wavelength-division multiplexing and detachable optical I/O.

a, Layout of a pure-silicon Mach-Zehnder modulator implemented on the monolithic CMOS SiPh platform, illustrating travelling-wave device geometry including p-n junction phase shifters and transmission line. b, Cross-sectional schematic of the silicon MZM, highlighting the S-type junction modulation region within the Si waveguide and the SiN overcladding (schematic not to scale). c, Measured PAM4 eye diagram obtained using the integrated MZM, demonstrating ≥400 Gbps-class modulation performance alongside the 448 Gbps receive functions. d, Layout of a SiN wavelength-division-multiplexing routing circuit. e,f, Measured WDM spectra for a baseline SiN implementation (e) and precision SiN film with optimal performance (f), showing improved channel alignment and reduced centre-wavelength variation (from ~10 nm to <1.5 nm). g, Schematic of a detachable optical I/O architecture based on cavity-integrated micro-optics and a multi-fiber array interface. h, Photograph of the detachable fibre-attach assembly integrated on a SiPh wafer, including micro-optics, a fiber-array unit (FAU) and auxiliary alignment fixtures. i, Measured through-band insertion loss, showing ~1 dB per facet coupling loss for the detachable optical interface in the O-band.

Supplementary Files

This is a list of supplementary files associated with this preprint. Click to download.

- NatureUltrahighspeedGePDGlobalFoundries2026SupplementaryRev2.docx