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Design and Performance Evaluation of a PV-Fed High-Gain DC–DC Converter Integrated with an 11-Level Reduced-Switch Multilevel Inverter Using Advanced PWM and Control Strategies

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Abstract: - This paper presents the design and performance evaluation of a photovoltaic (PV) based power conversion system integrated with a high-gain DC–DC converter and an 11-level multilevel inverter. The system employs a perturb and observe (P&O) maximum power point tracking method to ensure effective extraction of solar energy under varying environmental conditions. A reduced-switch asymmetric 11-level multilevel inverter is utilized to generate a stepped output voltage with improved waveform quality and lower harmonic distortion. Different carrier-based pulse width modulation techniques, including PD, POD, APOD, In-shift, and rotating trapezoidal PWM, are investigated. In addition, both proportional–integral (PI) and proportional–resonant (PR) controllers are implemented to regulate the inverter output. Simulation results demonstrate that the PR controller provides superior harmonic performance compared to the PI controller. Furthermore, the influence of modulation index on total harmonic distortion (THD) is analysed, showing that higher modulation index values lead to improved output quality. The PR-RTSPWM methodology outperforms the other modulation techniques in terms of harmonic performance, as confirmed by experimental validation using a digital signal controller (DSC).

Keywords: Photovoltaic (PV) System Reduces Switch Topology, High Gain DC-DC Converter, 11-Level Inverter, and Proportional Resonant (PR) Controller.

1. INTRODUCTION

Multilevel inverters (MLI) are becoming more and more used in industrial and renewable energy conversion systems because of their superior output waveform over the inverters with two levels. Multilevel inverters are appealing due to their near sinusoidal output waveform, reduced total harmonic distortion (THD), minimal dv/dt stress, and less power loss. The three primary varieties of traditional multilevel inverters are cascaded H-bridge (CHB), flying capacitor (FC), and neutral point clamped (NPC) [1]-[4]. Nevertheless, these traditional MLI have drawbacks, such as capacitor voltage balancing in FC and NPC. Among these inverters, the CHB MLI is unique, however it requires more separated DC sources. For these traditional MLI to achieve higher voltage levels, more switches are needed [5]-[8].

In light of the aforementioned problems with conventional MLI, researchers have made numerous attempts and created a large number of decreased device count MLI. Compared to the fundamental MLI topologies, these topologies require fewer switches and diodes to achieve the same number of levels [9]-[13]. Voltage boosting is not possible with the traditional and decreased device count MLI. Due to the low voltage produced by PV

panels and fuel cells, this voltage boosting will be crucial in renewable energy conversion systems [14]-[18].

The pursuit of renewable energy sources drives the sharp rise in fuel prices and greenhouse gas emissions [19], which over time leads to air pollution and climate change [20]. Among the many sustainable energy sources, solar energy is elegant and emits no emissions; the photovoltaic (PV) system makes the conversion of electricity simple [21]-[26]. Both residential and commercial customers started using it as a regular source of electricity [27]. This comprises a variety of solar electric car applications, vehicle charging stations, water pumping systems, and standalone systems for regions without dependable grid connectivity [28]-[30].

Photovoltaic power generation is composed of solar PV panels, and the output of a solar panel is fed into a DC connection via a DC-DC converter. The voltage is delivered to the DC-AC inverter and the load via a DC link [31]. The output of solar PV is not continuous; it varies depending on temperature and sun irradiation [32]-[37]. Therefore, it is crucial In order to extract PV module's power output, which is acknowledged to be greatest Power Point Tracking (MPPT) [38], for an efficient operation of a PV panel even under numerous climatic fluctuations in an annual computation [39]. The DC-DC converter is crucial to managing maximum power when the MPPT is present in a system because it works with the duty cycle change [40].

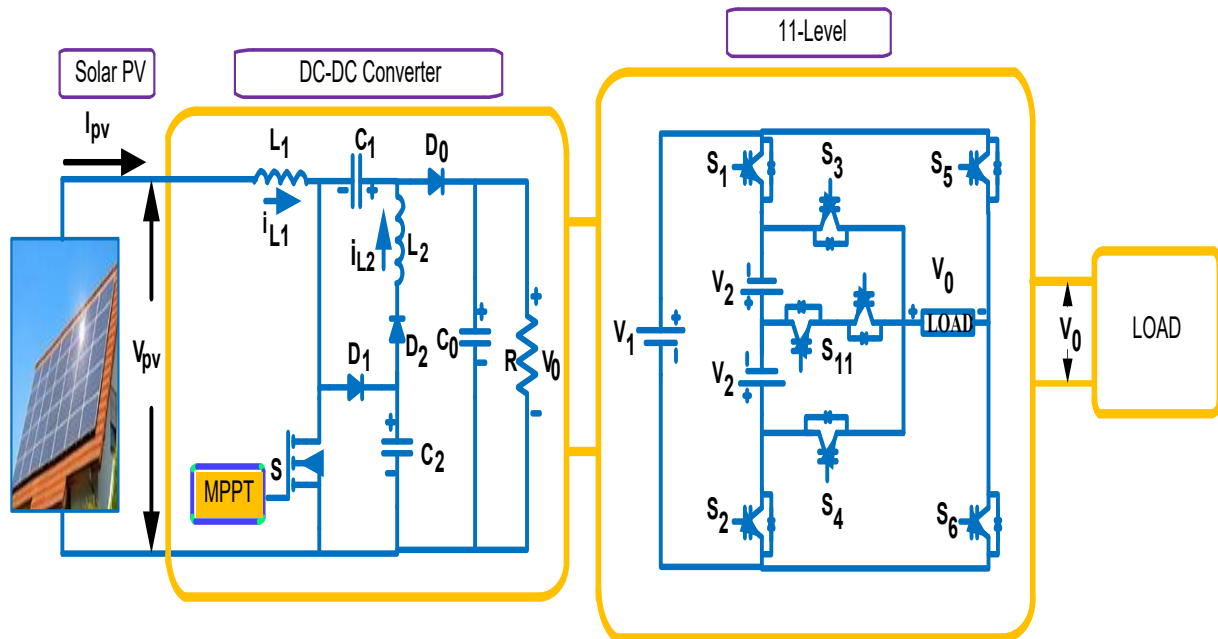


Figure 1: Block Diagram of PV-Fed Converter with Multilevel Inverter

In Figure 1, a stand-alone photovoltaic (PV) system is created with an 11-level multilevel inverter is combined with DC-DC boost converter. To ensure maximum energy extraction from the solar panels, the system uses a maximum power point tracking (MPPT) technique based on perturb and observe (P&O). First, the boost converter receives the DC output produced by the PV array. where it is stepped up to the required voltage level, and then delivered to the 11-level inverter. A thorough comparison of the outcomes is provided

after the inverter's performance is assessed using both PI and PR controllers in addition to different PWM approaches.

2. 11-LEVEL MULTILEVEL INVERTER

In order to produce multiple stepped output voltage levels, the circuit depicted in Figure 2 is an asymmetric multilevel inverter, specifically designed with a 1:2 voltage ratio between its DC sources [41]. It is made up of multiple power switches, S_1 through S_6 , and auxiliary switches, such as S_{11} , arranged so that various switch combinations result in varying output voltage levels. The main characteristic of asymmetry is the use of two DC sources, one of which has a voltage value of V and the other about $2V$. [42]-[44] The switches on the right side, which form an H-bridge structure, regulate the polarity of the output voltage applied to the load, while the switches on the left assist in choosing and combining these DC sources [45]. The circuit may create many voltage steps, such as V , $2V$, $3V$, $4V$, and $5V$, by turning on and off particular switches in the right order. This produces an enhanced staircase waveform that nearly approaches a sinusoidal output [46].

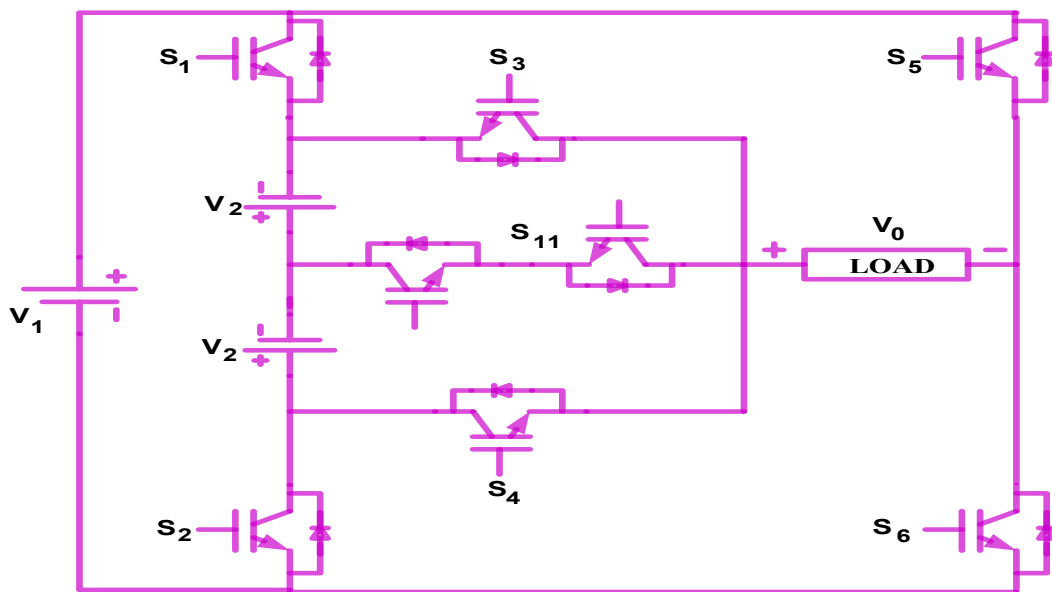


Figure 2: Reduced-Switch 11-Level Multilevel Inverter Configuration for AC Output Generation

To express how many switches the inverter needs overall is as follows:

$$N_{\text{Switch}} = 2K + 2 \quad (1)$$

where K is the quantity of DC voltage sources utilized.. For this configuration, $K=3$, resulting in a total of 8 switches.

$$V_{0,\text{max}} = V_1 + (K - 1) \quad (2)$$

The maximum output voltage is determined by combining the input DC sources and is given by:

$$V_{0,\text{max}} = V_1 + (K - 1)V_2 \quad (3)$$

This expression can also be related to the number of output voltage levels N as:

$$V_{0,\max} = \left(\frac{N-1}{2}\right) V_{dc} \quad (4)$$

Assuming the first source voltage V_1 is equal to the base DC voltage V_{dc} the equation becomes:

$$V_{dc} + (K-1)V_2 = \left(\frac{N-1}{2}\right) V_{dc} \quad (5)$$

3. ENHANCED SWITCHING SCHEME FOR AN 11-LEVEL MULTILEVEL INVERTER

Table 1: Switch Configuration Table for Basic and Modified 11-Level Inverter Topologies

Conventional switching sequence of 11-level inverter

Modified switching sequence of 11-level inverter

Mode	S_1	S_3	S_4	S_5	S_{11}	V_0
1	1	1	0	1	0	0
2	1	1	0	0	0	V_1
3	1	0	0	1	1	V_2
4	1	0	0	0	1	$V_1 + V_2$
5	1	0	1	1	0	$2V_2$
6	1	0	1	0	0	$V_1 + 2V_2$
7	0	0	1	0	0	0
8	0	0	1	1	0	$-V_1$
9	0	0	0	0	1	$-V_2$
10	0	0	0	1	1	$-(V_1 + V_2)$
11	0	1	0	0	0	$-2V_2$
12	0	1	0	1	0	$-(V_1 + 2V_2)$

Mode	S_1	S_3	S_4	S_5	S_{11}	V_0
1	1	1	0	0	0	V_1
2	1	0	0	1	1	V_2
3	1	0	0	0	1	$V_1 + V_2$
4	1	0	1	1	0	$2V_2$
5	1	0	1	0	0	$V_1 + 2V_2$
6	0	0	0	0	0	0
7	0	0	1	1	0	$-V_1$
8	0	0	0	0	1	$-V_2$
9	0	0	0	1	1	$-(V_1 + V_2)$
10	0	1	0	0	0	$-2V_2$
11	0	1	0	1	0	$-(V_1 + 2V_2)$

The Table 1 shows a comparison between conventional and modified switching patterns of an 11-level inverter. Both approaches produce the same voltage levels but differ in switching sequences. The sequence waveform is shown in Figure 4.

4. SWITCHING CONTROL METHOD

4.1 Phase Disposition Sinusoidal Pulse Width Modulation (PDSPWM)

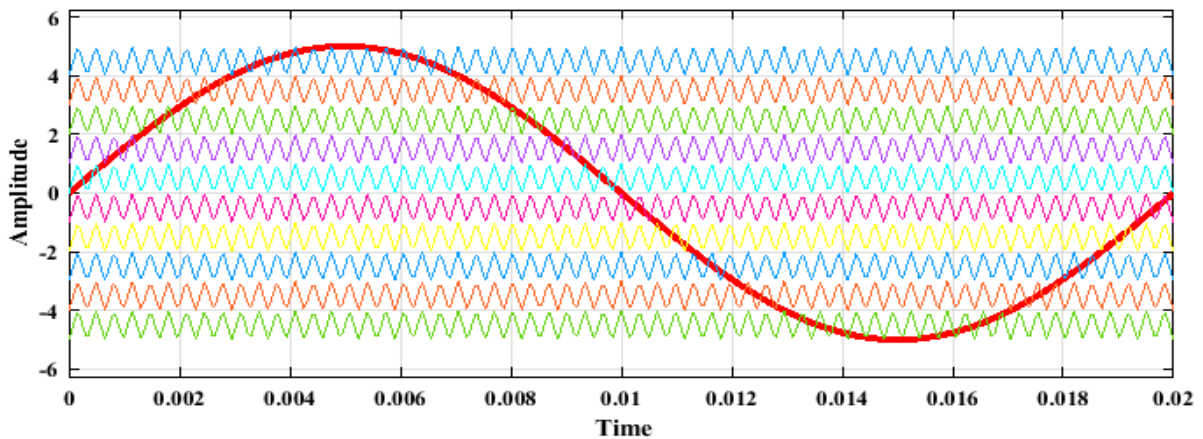


Figure 3: Aligned PDSPWM Carrier-Based PWM Scheme for Multilevel Inverter Control

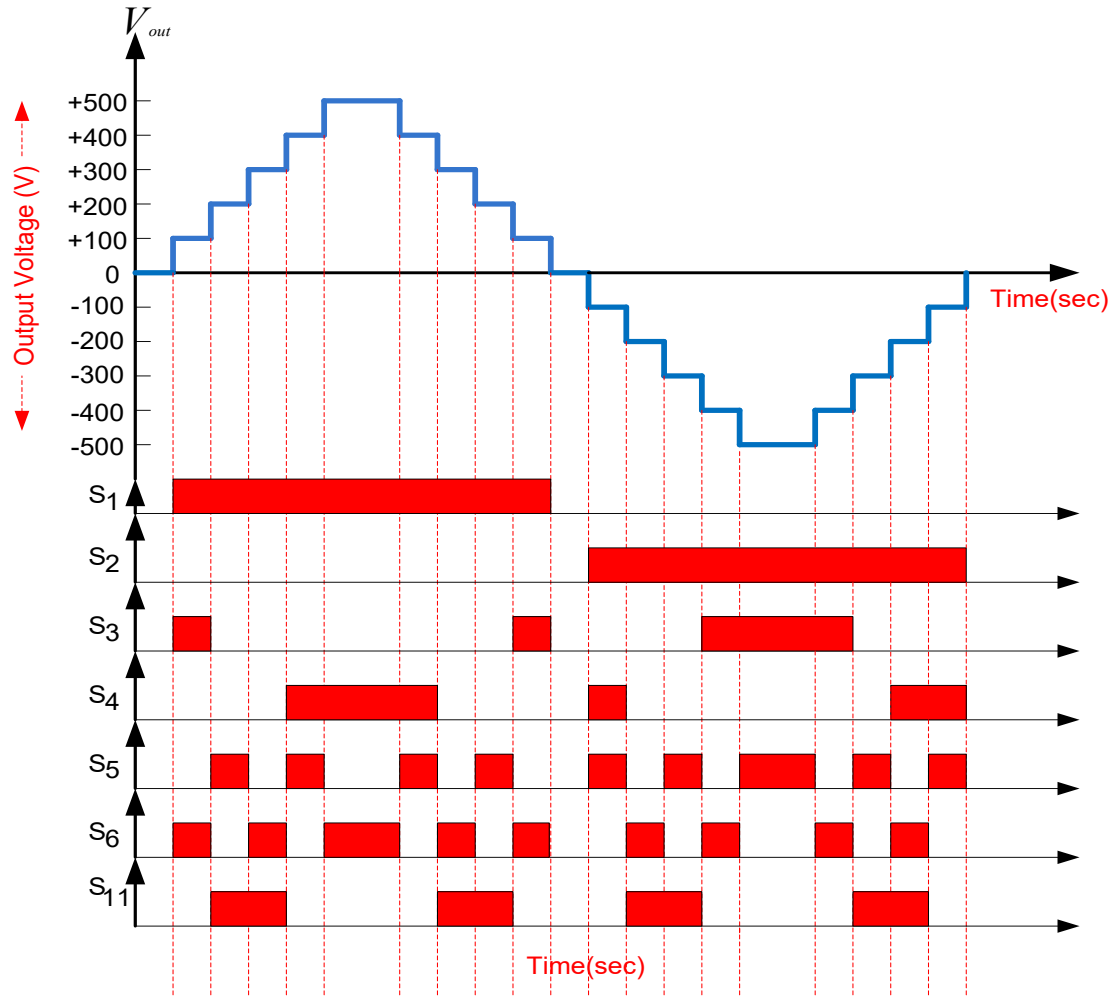


Figure 4: Gate Signal Sequence of an 11-Level Inverter

In PDSPWM [47] all carriers are in phase with each other as depicted in Figure 3. Table 2 below lists the triangular carriers' upper and lower values [48].

Table 2: Carrier Amplitude Limits for PDSPWM in Multilevel Inverter

Parameter	Value	Parameter	Value
Triangular 1 lower peak	-5	Triangular 1 upper peak	-4
Triangular 2 lower peak	-4	Triangular 2 upper peak	-3
Triangular 3 lower peak	-3	Triangular 3 upper peak	-2
Triangular 4 lower peak	-2	Triangular 4 upper peak	-1
Triangular 5 lower peak	-1	Triangular 5 upper peak	0
Triangular 6 lower peak	0	Triangular 6 upper peak	1
Triangular 7 lower peak	1	Triangular 7 upper peak	2
Triangular 8 lower peak	2	Triangular 8 upper peak	3
Triangular 9 lower peak	3	Triangular 9 upper peak	4
Triangular 10 lower peak	4	Triangular 10 upper peak	5

4.2 Phase Opposition Disposition Sinusoidal Pulse Width Modulation (PODSPWM)

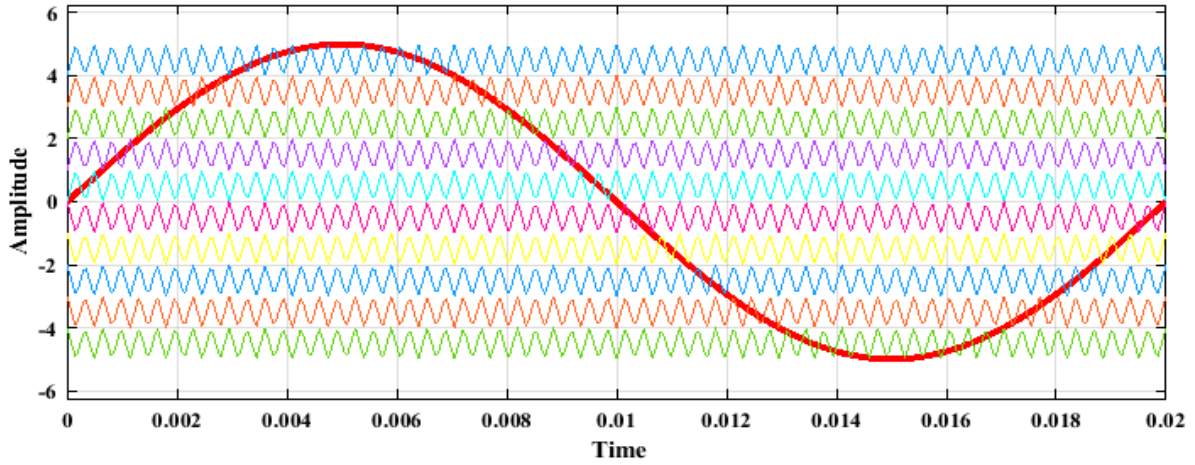


Figure 5: Aligned PODSPWM Carrier-Based PWM Scheme for Multilevel Inverter Control

In PODSPWM [49] every carrier is in phase if it is higher than zero, and is 180° out of phase with below the zero reference as depicted in Figure 5. Table 3 below lists the triangular carriers' upper and lower values [50].

Table 3: Carrier Amplitude Limits for PODSPWM in Multilevel Inverter

Parameter	Value	Parameter	Value
Triangular 1 lower peak	-4	Triangular 1 upper peak	-5
Triangular 2 lower peak	-3	Triangular 2 upper peak	-4
Triangular 3 lower peak	-2	Triangular 3 upper peak	-3
Triangular 4 lower peak	-1	Triangular 4 upper peak	-2
Triangular 5 lower peak	0	Triangular 5 upper peak	-1
Triangular 6 lower peak	0	Triangular 6 upper peak	1
Triangular 7 lower peak	1	Triangular 7 upper peak	2
Triangular 8 lower peak	2	Triangular 8 upper peak	3
Triangular 9 lower peak	3	Triangular 9 upper peak	4
Triangular 10 lower peak	4	Triangular 10 upper peak	5

4.3 Alternate Phase Opposition Disposition Sinusoidal Pulse Width Modulation (APODSPWM)

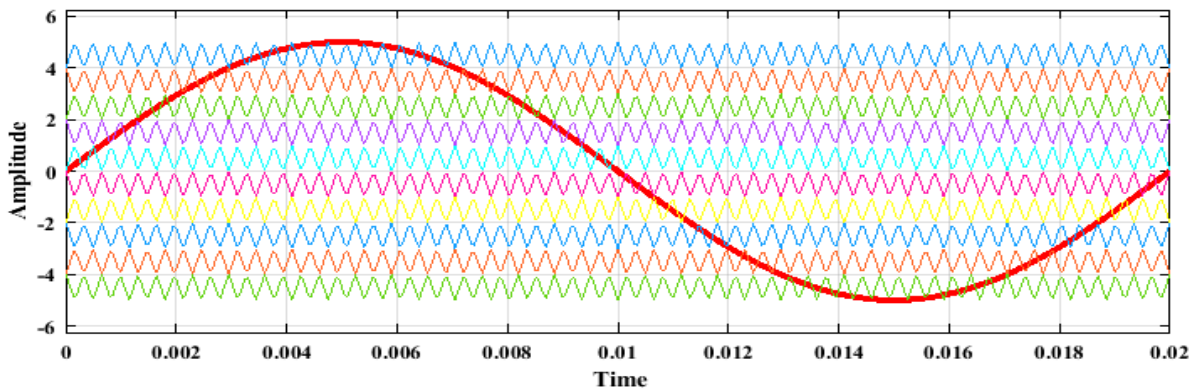


Figure 6: Aligned APODSPWM Carrier-Based PWM Scheme for Multilevel Inverter Control

In APODSPWM [51] every carrier and its neighbour carrier are out of phase with each other as depicted in Figure 6. Table 4 below lists the triangular carriers' upper and lower values [52]-[53].

Table 4: Carrier Amplitude Limits for APODSPWM in Multilevel Inverter

Parameter	Value	Parameter	Value
Triangular 1 lower peak	-4	Triangular 1 upper peak	-5
Triangular 2 lower peak	-4	Triangular 2 upper peak	-3
Triangular 3 lower peak	-2	Triangular 3 upper peak	-3
Triangular 4 lower peak	-2	Triangular 4 upper peak	-1
Triangular 5 lower peak	0	Triangular 5 upper peak	-1
Triangular 6 lower peak	0	Triangular 6 upper peak	1
Triangular 7 lower peak	2	Triangular 7 upper peak	1
Triangular 8 lower peak	2	Triangular 8 upper peak	3
Triangular 9 lower peak	4	Triangular 9 upper peak	3
Triangular 10 lower peak	4	Triangular 10 upper peak	5

4.4 In-Shift Sinusoidal Pulse Width Modulation (In-Shift SPWM)

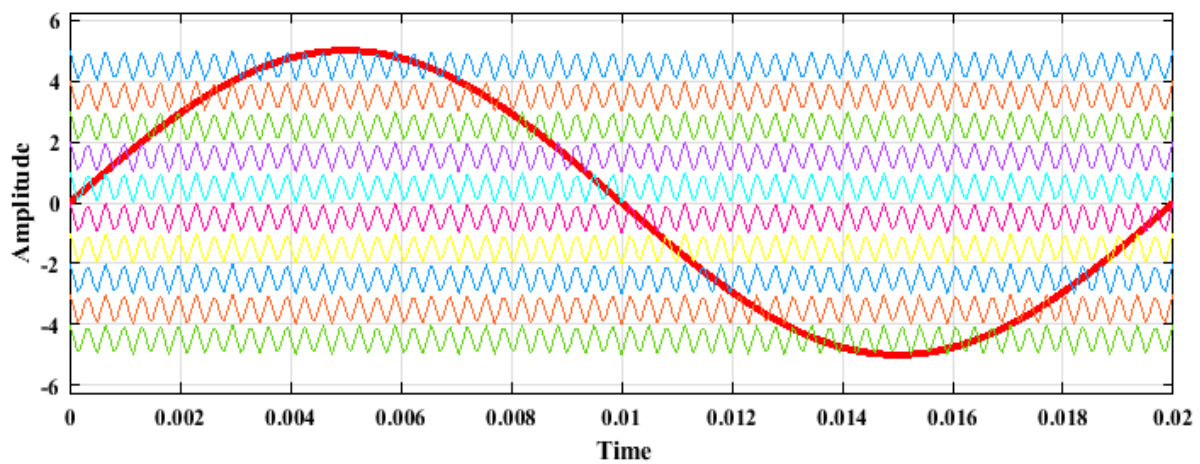


Figure 7: Aligned In-Shift SPWM Carrier-Based PWM Scheme for Multilevel Inverter Control

In In-Shift SPWM [54]-[55] all carriers are out of phase with each other as depicted in Figure 7. The upper and lower values of triangular carriers are mentioned in below Table 5 [56].

Table 5: Carrier Amplitude Limits for In-Shift SPWM in Multilevel Inverter

Parameter	Value	Parameter	Value
Triangular 1 lower peak	-4	Triangular 1 upper peak	-5
Triangular 2 lower peak	-3	Triangular 2 upper peak	-4
Triangular 3 lower peak	-2	Triangular 3 upper peak	-3
Triangular 4 lower peak	-1	Triangular 4 upper peak	-2
Triangular 5 lower peak	0	Triangular 5 upper peak	-1
Triangular 6 lower peak	1	Triangular 6 upper peak	0
Triangular 7 lower peak	2	Triangular 7 upper peak	1
Triangular 8 lower peak	3	Triangular 8 upper peak	2
Triangular 9 lower peak	4	Triangular 9 upper peak	3
Triangular 10 lower peak	5	Triangular 10 upper peak	4

4.5 Rotating Trapezoidal sinusoidal pulse width modulation (RTSPWM)

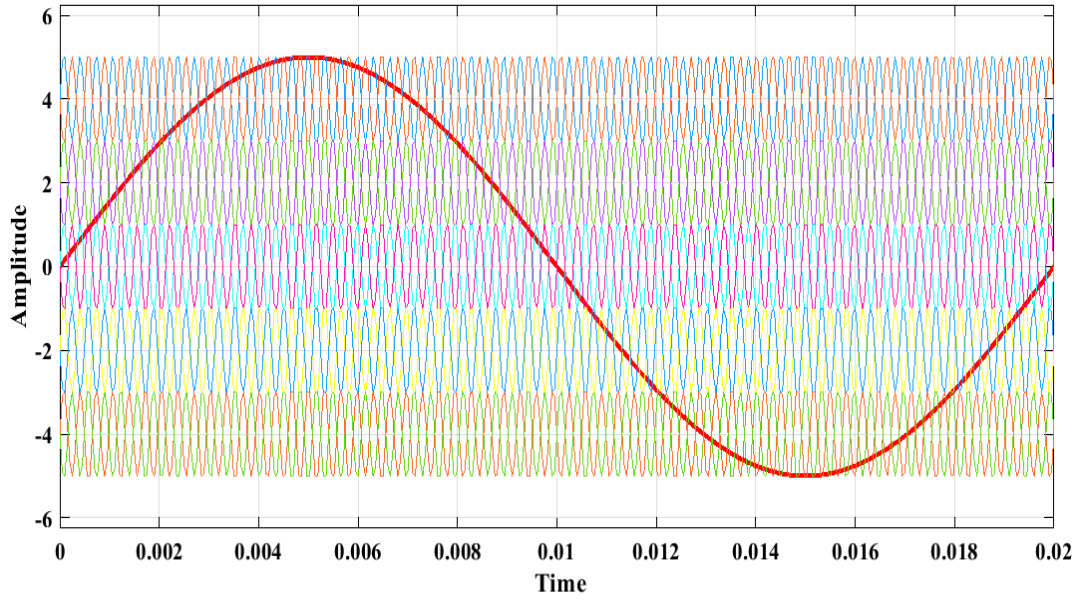


Figure 8: Aligned RTSPWM Carrier-Based PWM Scheme for Multilevel Inverter Control

In RTSPWM all Trapezoidal carriers are in phase with each other as shown in Figure 8.

Carriers are expressed as

$$C_i = E \left((-1)^{f(i)} y_c(w_c, \phi) + i - \frac{N}{2} \right) \quad (6)$$

E = Amplitude of trapezoidal carrier, w_c = frequency, $i = 1, 2, \dots (N-1)$

Normalized Trapezoidal carrier is

$$y_c(w_c, \phi) = (-1)^\alpha ((\alpha \bmod 2) - 1) + \frac{1}{2} \quad (7)$$

$$\alpha = \frac{w_c t + \phi}{\pi} \quad (8)$$

5. MODELLING OF HIGH GAIN DC-DC CONVERTER

When the switch S is activated, the inductors L_1 and L_2 receive energy from the input source, as shown in Figure 10 [57]-[59], allowing them to store energy in their magnetic fields. During this period, certain diodes are reverse-biased, and capacitors hold onto their stored charge. The inductors' stored energy is released and sent to the load and capacitors via the diodes when the switch is turned off. [60] By stacking or adding their voltages with the

input source, the capacitors (C_1 , C_2 and C_0) function as energy transfer and storage components, increasing the voltage.

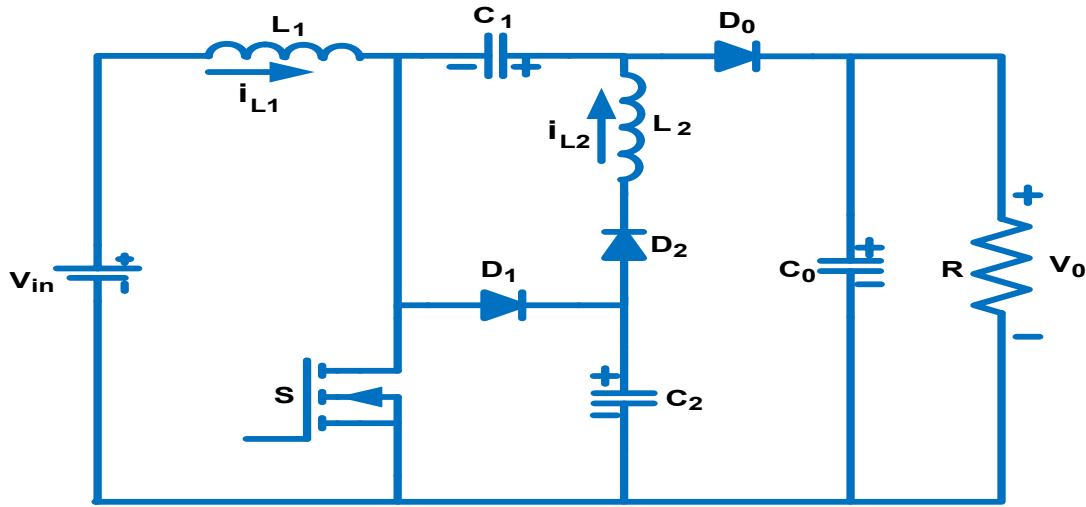


Figure 10: Circuit of the DC–DC Converter

5.1 Operation Principle Dc-Dc Converter

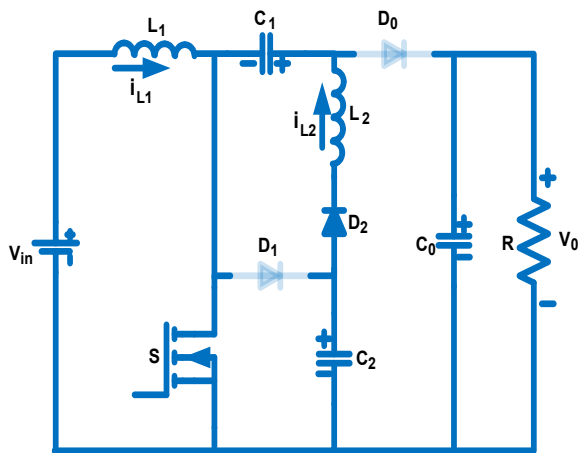


Figure 11. Energy Charging Phase (ON) of the DC–DC Converter

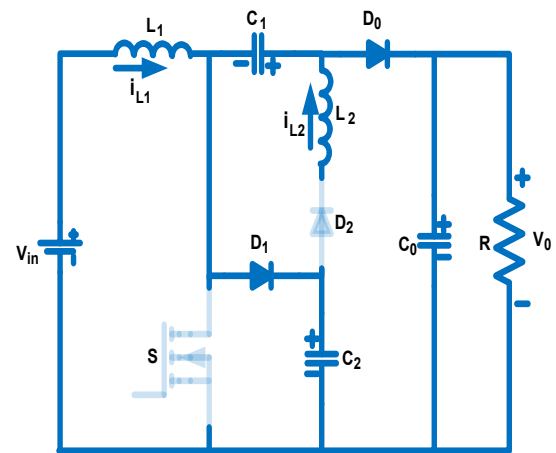


Figure 12. Energy Discharging Phase (OFF) of the DC–DC Converter

Smooth energy transfer is ensured by the inductors L_1 and L_2 , which constantly carry current without decreasing to zero. The input source charges L_1 when switch S is turned on and L_2 storing energy in their magnetic fields, whereas diodes D_1 and D_2 continue to be reverse prejudiced as shown in Figure 11[61]-[62]. Capacitor C_0 simultaneously provides energy to the load. Diodes D_0 allow the stored energy in both inductors to be released when the switch is turned off as shown in the Figure 12. Charging capacitors C_1 , D_1 , and D_2 C_2 , C_0 , and increasing the output voltage. The converter delivers increased efficiency, decreased ripple, and a constant high-gain output since the inductor currents never reach zero [63]. Starting from the volt-second balance on the circuit, the relation can be expressed as

$$V_{in} \cdot d - V_{C_2} + V_{C_2}d + V_{in} - V_{in}d = 0 \quad (9)$$

The average voltage across inductor L_2 is zero during steady-state operation, providing

$$(V_{C2} - V_{C1})d = (V_0 - V_{C2})(1 - d) \quad (10)$$

$$\frac{V_{in}}{1-d} - \left(V_0 - \frac{V_{in}}{1-d} \right) d = V_0(1 - d) \quad (11)$$

$$\frac{V_0}{V_{in}} = \frac{1+d}{1-d} \quad (12)$$

Capacitor C_1 voltage is

$$V_{C1} = V_{in} \left(\frac{1+d}{1-d} \right) - \frac{V_{in}}{1-d} \quad (13)$$

$$V_{C1} = \left(\frac{V_{in}}{1-d} \right) \cdot d \quad (14)$$

Inductor Design

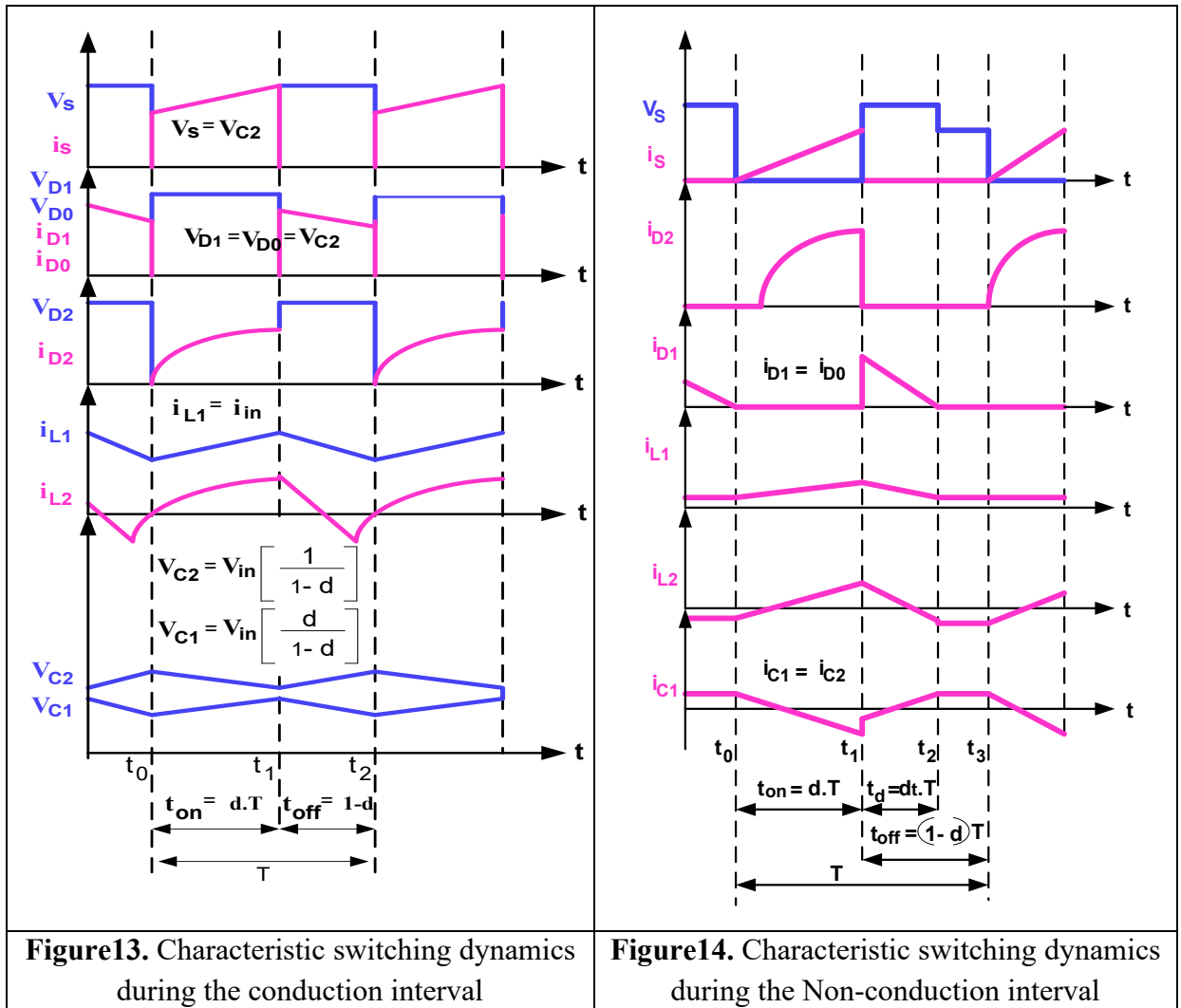
$$L_1 = \left(\frac{V_{in} \cdot d}{f \cdot \Delta i_{L1}} \right) \quad (15)$$

$$L_2 = \left(\frac{V_{C2} \cdot (1-d)}{f \cdot \Delta i_{L2}} \right) \quad (16)$$

Capacitor Design

$$C_1 = C_2 = \left(\frac{I_0}{f \cdot \Delta V_C} \right) \quad (17)$$

$$C_0 = \left(\frac{P_0}{4\pi f_G V_0 \Delta V_0} \right) \quad (18)$$



The waveforms for the DC-DC converter topology [64] in ON and OFF mode are shown in Figures 13 and 14.

6. SOLAR PV DRIVEN DC-DC CONVERTER WITH MPPT AND 11-LEVEL INVERTER CONTROL

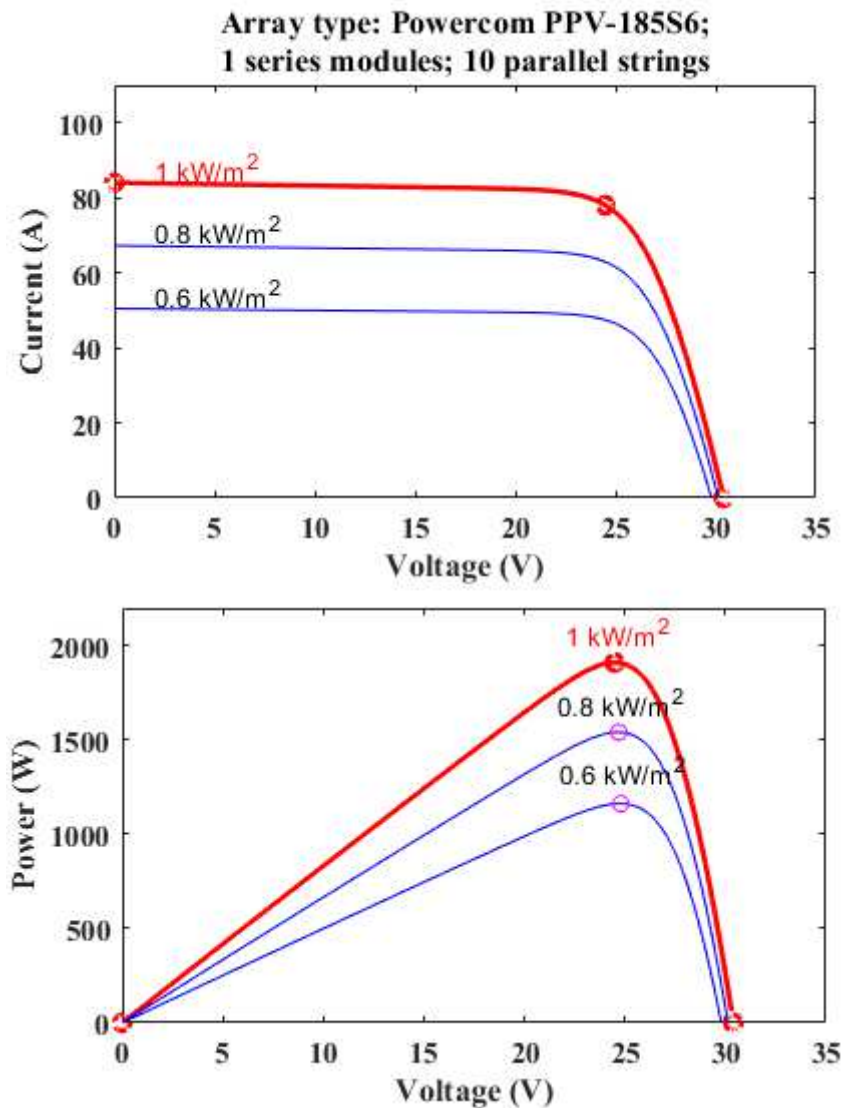


Figure 15: Influence of varying solar irradiance on the electrical characteristics of the Powercom

The P&O algorithm is employed for MPPT in a high-gain DC-DC converter that is connected to the PV module [65]. The voltage-power (PV) and current-voltage (IV) characteristics of the POWERCOM system are shown in Figures 15 and 16.

The effectiveness of the high-gain DC-DC converter is verified using a solar source, where the input voltage of 30 V is stepped up to 200 V, resulting in a significantly higher output. Figures 17 and 18 show the associated voltage and current waveforms.

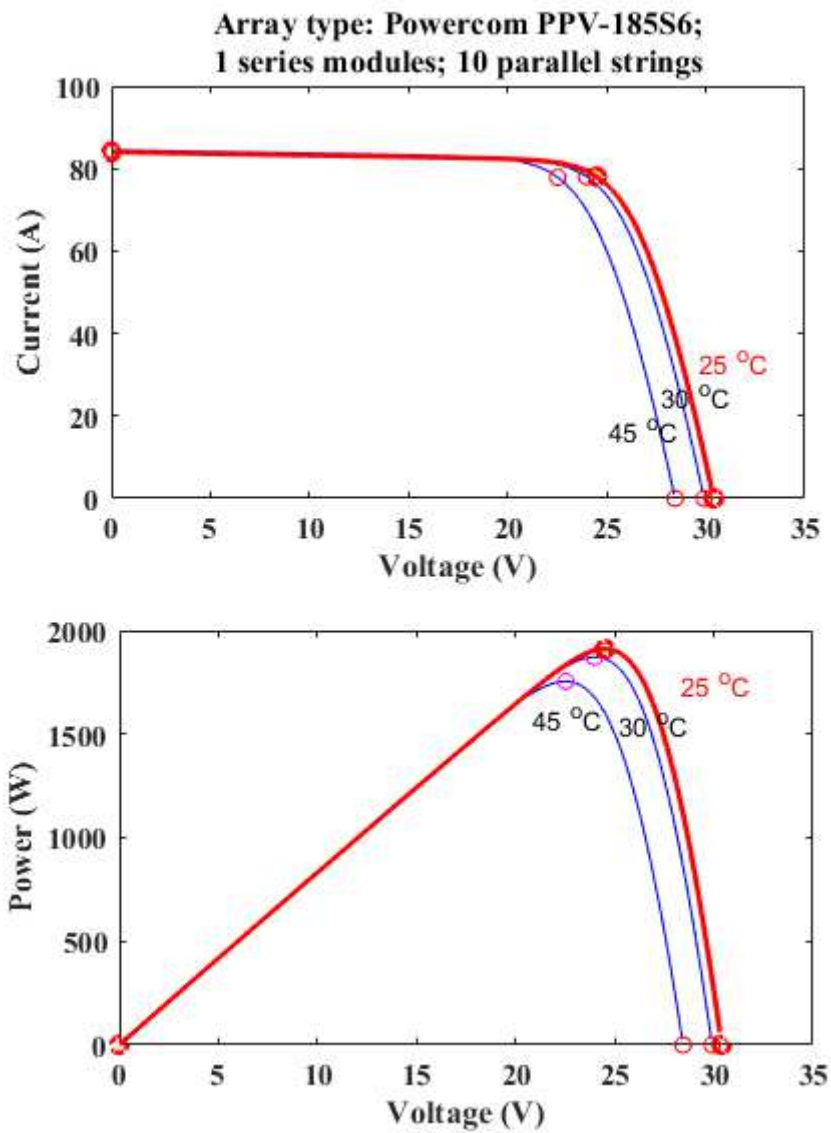


Figure 16: Thermal degradation analysis of I-V and P-V characteristics for the Powercom

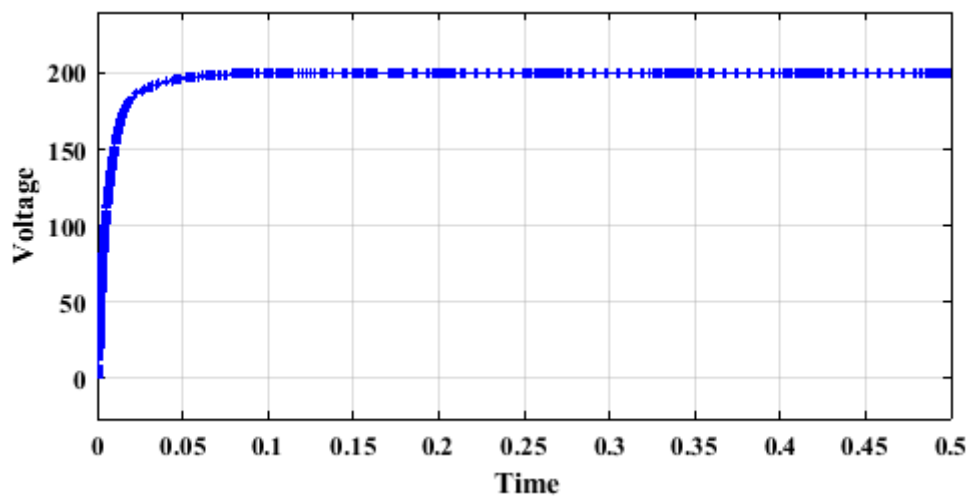


Figure 17: Output voltage profile under nominal switching conditions

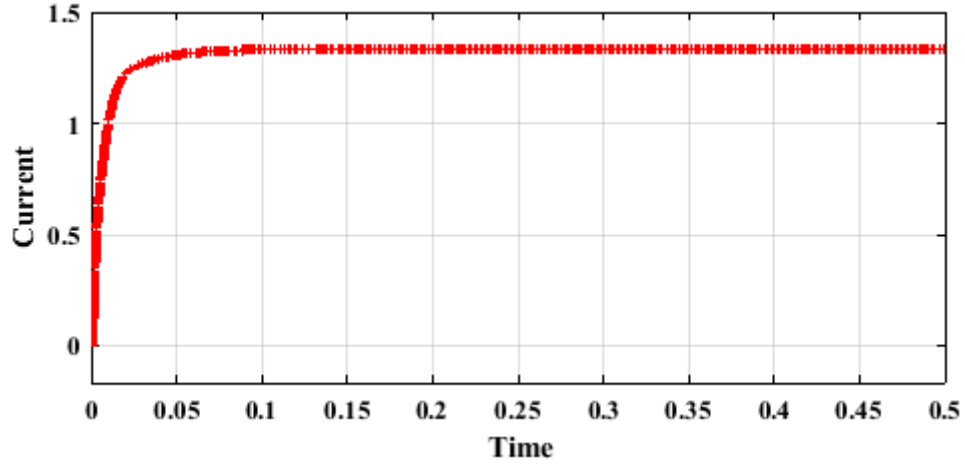
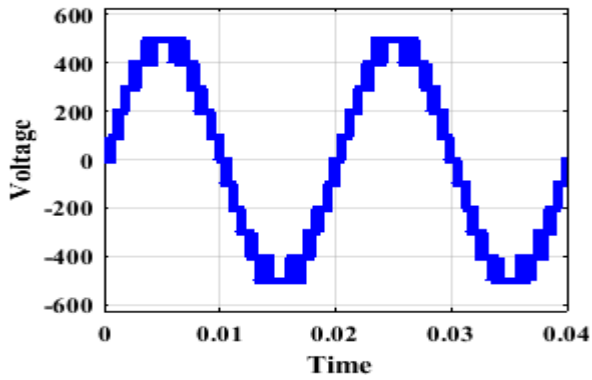
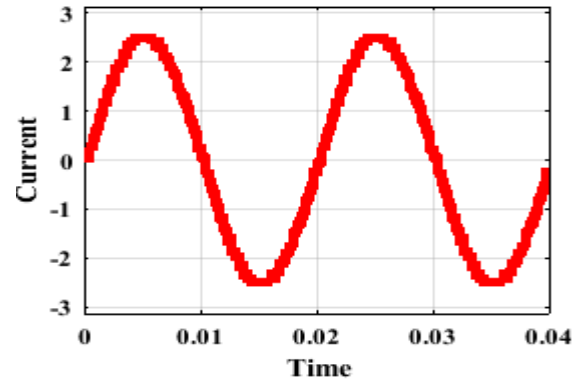


Figure 18: Output voltage profile under nominal switching conditions

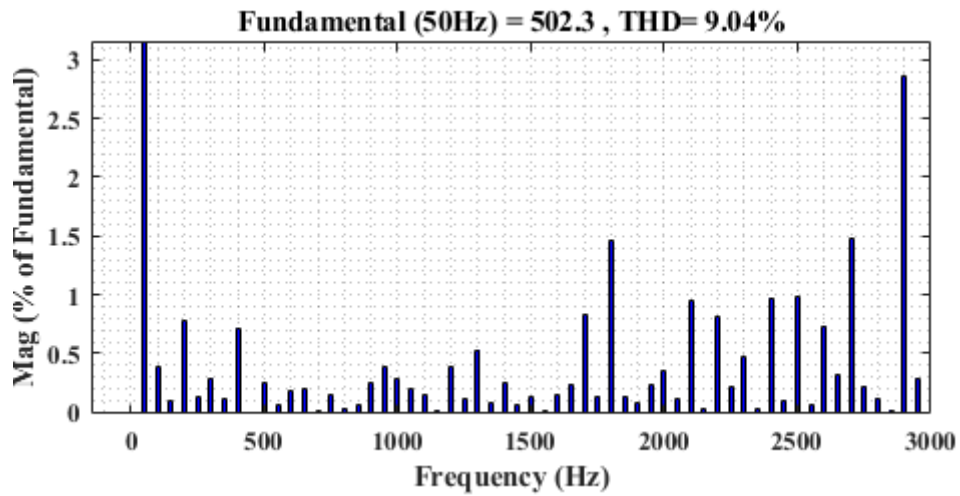
The system consists of a solar PV source connected to a high-gain DC–DC converter using the P&O MPPT technique, along with an 11-level multilevel inverter regulated by a PI (Proportional Integral) controller for an RL load. Figure 19 presents the load voltage and current waveforms, with THD values of 9.04% and 9.85%, respectively.



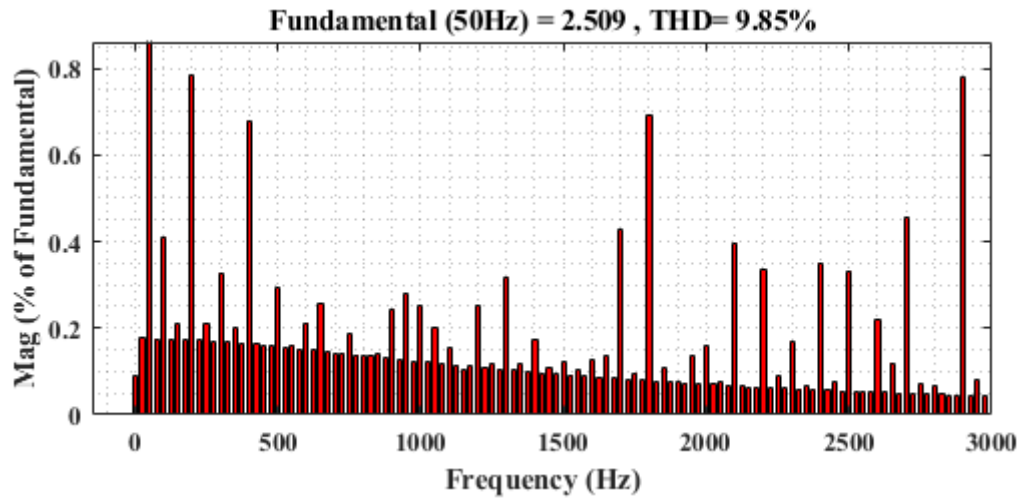
(a) Load terminal voltage



(b) Load terminal current



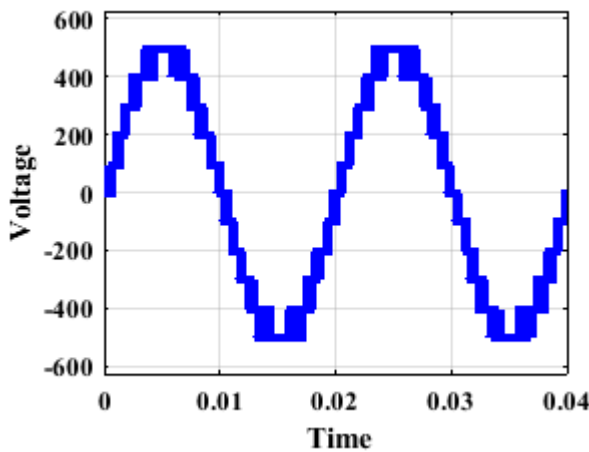
(c) Harmonic Content of Load Voltage



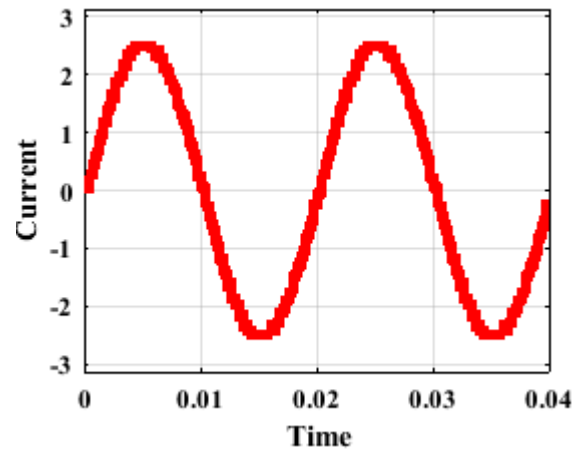
(d) Harmonic Content of Load Current

Figure 19: Output Performance Evaluation of Photovoltaic System Using DC–DC Converter and PI-Based 11-Level MLI

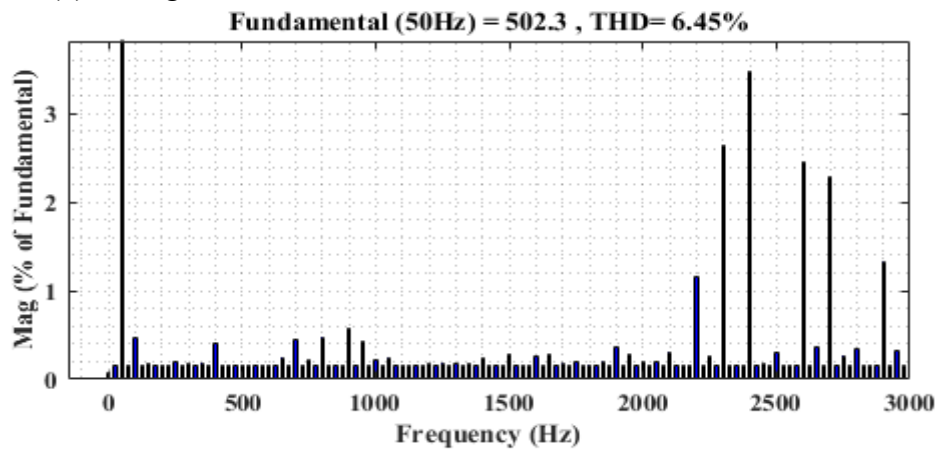
The system consists of a solar PV source connected to a high-gain DC–DC converter using the P&O MPPT technique, along with an 11-level multilevel inverter regulated by a PR (Proportional Resonant) controller for an RL load. Figure 20 presents the load voltage and current waveforms, with THD values of 6.45% and 94.65%, respectively.



(a) Voltage at Load



(b) Current at Load



(c) Harmonic Spectrum of Load Voltage

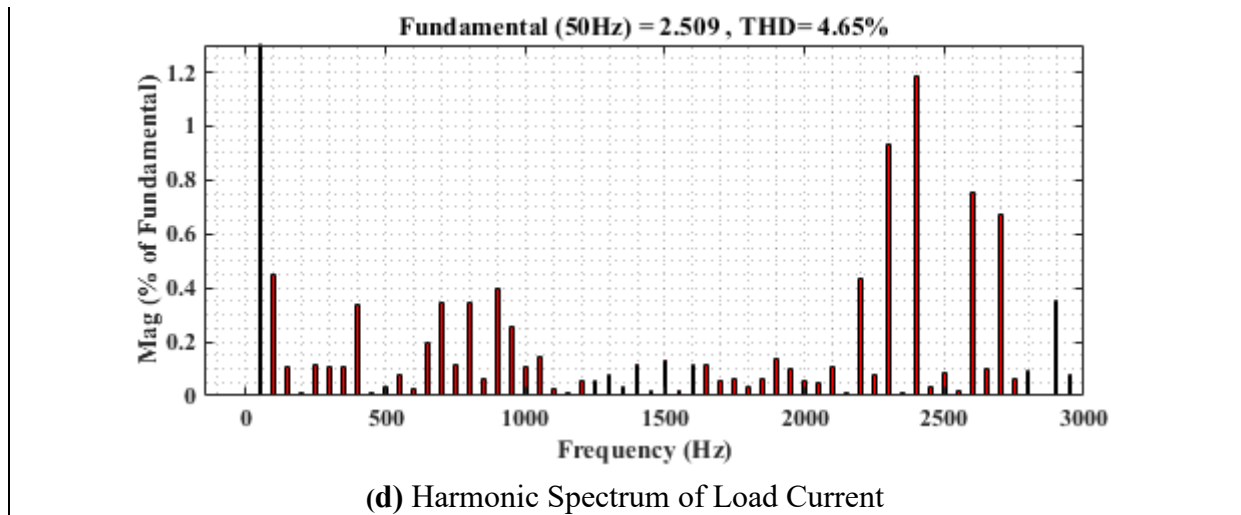


Figure 20: Output Performance Evaluation of Photovoltaic System Using DC–DC Converter and PR-Based 11-Level MLI

Table 6: Comparison of Load Harmonic Distortion Using PI and PR Controllers

Category	PI	PR
Load Voltage THD%	9.04%	6.45%
Load Current THD%	9.85%	4.65%

The comparison Table 6 shows that the PR controller performs better than the PI controller in reducing harmonic distortion. With the PI controller, the load voltage and current contain higher distortion levels of 9.04% and 9.85%, respectively. In comparison, these values drastically decrease to 6.45% for voltage and 4.65% for current when the PR controller is utilized.

Table 7: Comparison of PR-Controlled Multilevel Inverter THD Performance with Various PWM Techniques

Load Parameter	PR-PDSPWM Controller	PR-PODSPWM Controller	PR-APODSPWM Controller	PR-In Shift PWM Controller	PR-RTSPWM Controller
Voltage	12.42%	9.53%	9.98%	6.73%	6.45%
Current	10.8%	5.37%	5.91%	4.69%	4.65%

Table 7 illustrates how the choice of PWM method under the PR controller significantly affects the harmonic performance with a modulation index (MI) of 1.0. Out of all the techniques, RTPWM and in-phase shifted PWM yield the greatest results with the least amount of distortion. Cleaner and more sinusoidal waveforms are seen by the voltage THD dropping to 6.73% and 6.45%, and the current THD dropping to 4.69% and 4.65%, respectively.

Table 8: Modulation Index's Impact on Load Current and Voltage

MI	Load Voltage	Load Current
1.0	6.45%	4.65%
0.8	7.16%	5.38%
0.6	8.76%	6.47%
0.4	10.21%	7.11%
0.2	15.41%	10.48%

Table 8 illustrates how the modulation index (MI) affects harmonic distortion. Better waveform quality is indicated by the lowest voltage and current distortions (6.45% and 4.65%, respectively) when MI is at its maximum value of 1.0. The THD values for both voltage and current progressively rise as the modulation index falls. For instance, the distortion increases somewhat for MI = 0.8 and 0.6, but it increases significantly at lower values like 0.4 and 0.2, reaching 10.21% and 15.41% for voltage and 7.11% and 10.48% for current.

7. EXPERIMENTAL VALIDATION



Figure 21: An 11-level inverter's hardware demonstration

The prototype of a single-phase, 11-level, multilevel inverter with a 24 V output voltage is depicted in Figure 21. The modulation approach is used in the Digital Signal Controller (DSC) dsPIC20F2010. The experimental setup consists of a single module made consisting of MOSFET switches. A DSC is made up of a microcontroller and a DSP. Microchip has created devices with substantial DSP functionality, such as the dsPIC30F. The dsPIC30F2010 has six PWM output channels, four 16-bit capture input functions, three 16-bit timers/counters, dual data fetch, and a modified Harvard architecture.

Table9. %THD Evaluation of output voltage in comparison

Controller	Simulation	Experimental
PR-PDSPWM	12.42	12.42
PR-PODSPWM	9.53	9.54
PR-APDSPWM	9.98	10.01
PR-In Shift SPWM	6.73	6.74
PR-RTSPWM	6.45	6.46

The DSC uses MPLAB software for code development and compilation. Three 16-bit timers/counters are included in this DSC. The THD derived from the hardware prototype is displayed in Figure 22. The performance percentage THD voltage value of several PR-based PWM control methods under both simulation and experimental settings is compared in Table 9. PR-RTSPWM provides the best performance with the lowest value out of all the approaches.

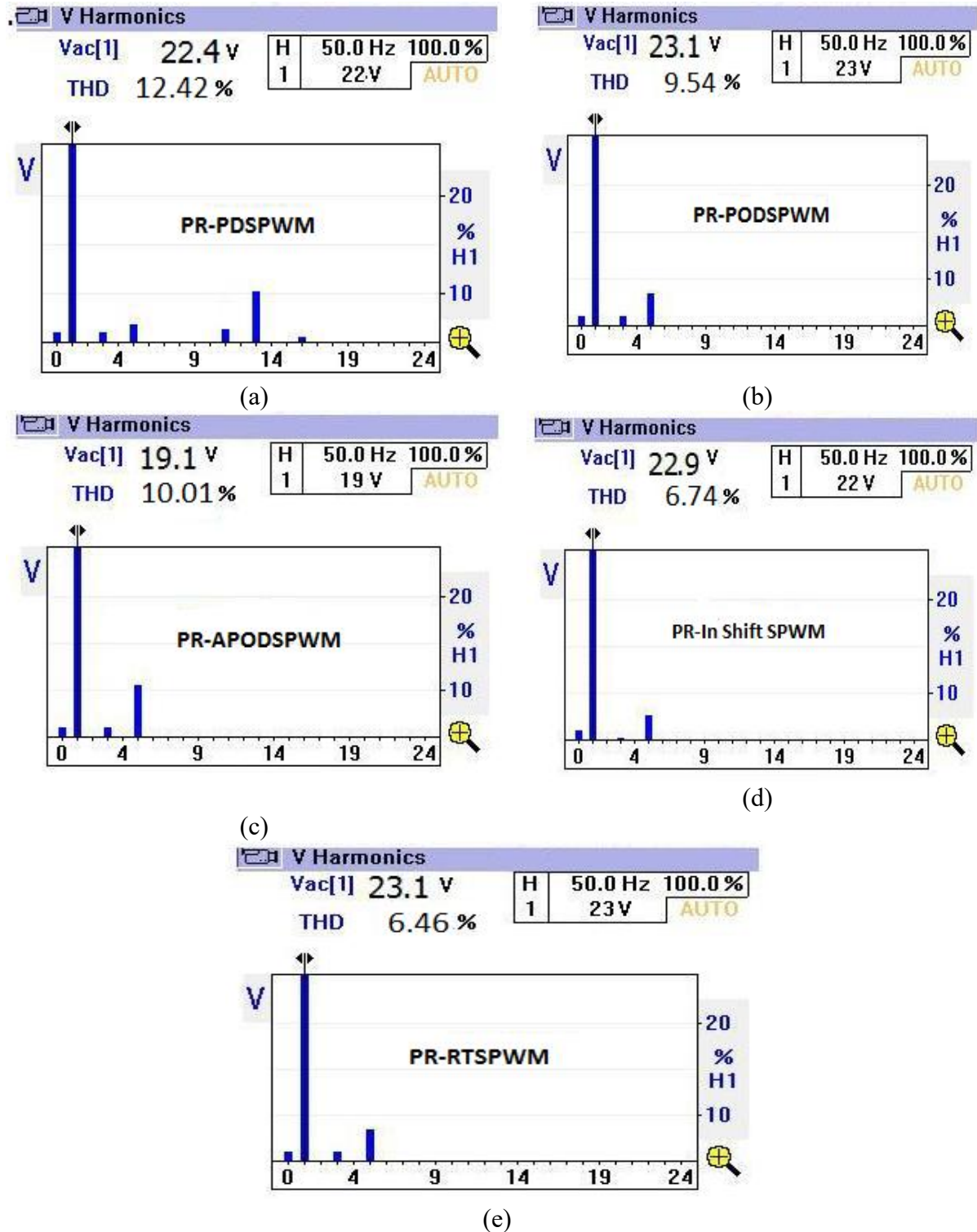


Figure 22 : THD of output voltage produced experimentally utilizing different modulation techniques

8. CONCLUSION

The study confirms that integrating a high-gain DC–DC converter with an 11-level reduced-switch multilevel inverter significantly enhances the performance of photovoltaic energy systems. The converter effectively increases the low PV voltage to a suitable level,

while the multilevel inverter produces a near-sinusoidal output with reduced switching stress. Among the control strategies examined, the proportional–resonant controller outperforms the proportional–integral controller by achieving lower voltage and current distortion. Additionally, the selection of PWM technique plays a crucial role, where PD and rotating trapezoidal methods yield better harmonic performance. The analysis of modulation index reveals that operating at higher values results in lower total harmonic distortion and improved waveform quality. The modulation approaches have been validated using a real-time prototype single-phase 11-level multilevel inverter. The experimental data validates the simulated results.

Data Availability: The datasets used and/or analysed during the current study are available from the corresponding author upon reasonable request.

Ethical Approval: This paper does not contain any studies with human participants or animals performed by any of the authors.

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