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Current THD Optimization of a Five-Level Active Neutral-Point-Clamped Converter Under Capacitor Voltage Imbalance

Zhan Liu¹ · Jintao Zhang¹ · Jiawei Fu¹ · Yuan Sun¹ · Weilong Jia¹ · Guifeng Wang¹

Abstract

To mitigate the increase in output-current total harmonic distortion (THD) induced by capacitor voltage imbalance in five-level active neutral-point-clamped (5L-ANPC) converters, this paper proposes a current-THD optimization strategy based on the volt-second balance principle. By analyzing the converter topology and switching states, the inherent relationship between capacitor voltage deviation and output-current harmonic distortion is systematically revealed. On this basis, an optimized modulation-wave design method is established by explicitly considering the influence of capacitor voltage fluctuation. Capacitor voltages are regulated through the appropriate selection of redundant switching states, whereas gate signals are generated according to the optimized modulation-wave amplitude and the action durations of the key redundant states. In contrast to existing modulation methods that primarily emphasize voltage balancing, common-mode voltage suppression, or capacitor ripple reduction, the proposed method further characterizes the coupling mechanism between capacitor voltage fluctuation and output-current THD. As a result, harmonic optimization is achieved without sacrificing the capability of capacitor voltage regulation. Experimental results demonstrate that the proposed method can reduce output-current THD by up to 37.7% while maintaining effective capacitor voltage regulation.

Keywords Five-level active neutral-point-clamped (5L-ANPC) converter, capacitor voltage imbalance, total harmonic distortion (THD), volt-second balance, redundant switching states, modulation optimization.

1 Introduction

With the rapid development of renewable energy generation, high-performance motor drives, electric ship propulsion, and electric aircraft propulsion, power electronic converters are increasingly required to provide higher power density, higher efficiency, and better output power quality. Owing to the advantages of low device voltage stress, high output waveform quality, reduced filter requirements, and low electromagnetic interference, multilevel converters have become a major research focus in medium- and high-voltage high-power energy conversion systems. Among these topologies, the five-level active neutral-point-clamped (5L-ANPC) converter combines the structural advantages of the conventional neutral-point-clamped topology with those of active clamping branches, and therefore exhibits strong potential in device voltage sharing, loss optimization, and output performance improvement ^[1].

Although the five-level ANPC converter exhibits strong application potential, practical operation is still significantly limited by capacitor voltage imbalance and large voltage fluctuations. Capacitor voltage deviation alters the actual magnitude and effective duration of each output level, thereby degrading modulation accuracy, output waveform quality, and dynamic performance. Reference ^[2] indicates that, in dual five-level ANPC inverters, the modulation strategy is closely coupled with voltage-balancing control, and improper coordination directly affects stable system operation. Reference ^[3] further shows that, although fixed-switching-frequency model predictive control can simultaneously address voltage balancing and common-mode voltage suppression in five-level ANPC converters, capacitor voltage deviation still affects the

optimal selection of control voltage vectors. The review in ^[1] also identifies capacitor voltage imbalance as one of the key factors limiting the high-performance operation of this topology. Therefore, investigation of the mechanism of capacitor voltage imbalance and its influence on output harmonic characteristics is essential for high-performance control of five-level ANPC converters.

To address capacitor voltage imbalance, a variety of balancing methods have been reported, mainly including modulation-based approaches, redundant-vector duration allocation methods, and model-predictive-control-based optimization methods. Reference ^[4] shows that neutral-point voltage balance in three-level NPC converters can be achieved by adjusting the action durations of redundant vectors. Reference ^[5] shows that discontinuous pulsewidth modulation can simultaneously maintain neutral-point potential balance and acceptable modulation performance in T-type three-level converters. Reference ^[6] shows that an algebraic modulation strategy enables inherent neutral-point voltage balancing in 3L-NPC converters. In addition, Reference ^[7] shows that an improved reference-voltage decomposition method can achieve neutral-point voltage balance while reducing common-mode voltage. Reference ^[8] shows that virtual-space-vector pulsewidth modulation can coordinate voltage balancing and common-mode voltage suppression through active neutral-point control. Beyond modulation methods, Reference ^[9] shows that virtual-vector-based finite-control-set model predictive control can simultaneously ensure neutral-point voltage balance and current control performance without weighting factors. Reference ^[10] further shows that an improved model predictive current control method can simultaneously suppress neutral-point voltage fluctuation, reduce common-mode voltage, and

improve current tracking performance. Although these studies provide useful insights into voltage-balancing control for multilevel converters, the coupling mechanism between capacitor voltage fluctuation and output-current THD in five-level ANPC converters remains insufficiently understood, and dedicated investigations of their complex redundant states are still limited. Therefore, it is necessary to investigate current-THD optimization under capacitor voltage imbalance.

Based on the above analysis, this paper investigates output-current harmonic optimization for the five-level active neutral-point-clamped converter under capacitor voltage imbalance. First, on the basis of the converter topology and operating states, the influence of capacitor voltage deviation on output-level distribution, equivalent effective voltage, and output-current harmonic characteristics is analyzed, and the intrinsic link between capacitor voltage imbalance and the increase in output-current total harmonic distortion is revealed. Then, based on this structural analysis and the volt-second balance principle, an optimized modulation-wave design method that accounts for capacitor voltage fluctuation is developed, and a current-THD optimization strategy under capacitor voltage imbalance is proposed. In this strategy, capacitor voltage regulation is achieved through the proper selection of redundant switching states. The optimized modulation-wave amplitude is derived from the volt-second balance relationship, and the action durations of the key redundant switching states are determined from the planar geometric relationship between the modulation wave and the triangular carrier. Finally, the gate signals of the power devices are generated accordingly. The effectiveness of the proposed method is validated through both simulation and experimental results.

2 Operating Principle Analysis

2.1 Topology Analysis of the 5L-ANPC Converter

The bridge-leg topology of the 5L-ANPC converter is shown in Fig. 1. To suppress dc-side voltage fluctuation, the dc side is formed by two energy-storage capacitors, C_{up} and C_{down} . The dc input voltage V_{dc} is equally divided into the upper dc-capacitor voltage V_p and the lower dc-capacitor voltage V_n . Each phase leg consists of power switches S_{x1} , S_{x2} , S_{x3} , S_{x4} , S_{x5} , S_{x6} , S_{x7} , S_{x8} together with a flying capacitor C_{fx} , where x denotes phases a, b, and c. The flying-capacitor voltage is regulated around $V_{dc}/4$. R and L denote the load resistance and inductance, respectively. Assuming that the dc-bus voltage is $4E$, the topology of each phase leg should satisfy the following conditions to ensure five-level stepped voltage generation and sinusoidal output current characteristics:

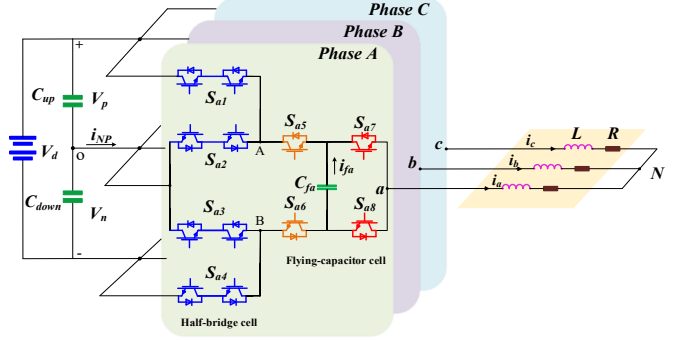


Fig. 1 Topology of 5L-ANPC converter

Assuming that the dc-bus voltage is $4E$, the topology of each phase leg should satisfy the following conditions to ensure five-level stepped voltage generation and sinusoidal output current characteristics:

1. The switch pairs (S_{x1}, S_{x2}) , (S_{x3}, S_{x4}) , (S_{x5}, S_{x6}) and (S_{x7}, S_{x8}) operate in a complementary manner; namely, the two switches in each pair cannot be simultaneously turned on or simultaneously turned off.
2. Switches S_{x1} and S_{x3} , S_{x2} and S_{x4} , are required to switch on and off simultaneously.
3. The flying-capacitor voltage is maintained at E .
4. The voltages of the upper and lower dc-link capacitors are maintained at $2E$.

According to the above operating principles, each phase leg of the 5L-ANPC converter has eight switching states, denoted as V0–V7. The corresponding switching states and output voltages are listed in Table 1. It can be observed that the 5L-ANPC converter contains two pairs of redundant switching states, namely V1/V2 and V5/V6. For a given load current direction, each redundant pair generates the same output voltage, but imposes opposite charging and discharging effects on the flying-capacitor voltage. Therefore, proper selection of the redundant switching states is required to regulate the flying-capacitor voltage balance.

2.2 Analysis of the Influence of Capacitor Voltage Fluctuations on Output Performance

The dc-link capacitor voltages and the flying-capacitor voltage should be maintained around $2E$ and E , respectively. As shown by the analysis of the operating principle of the 5L-ANPC converter in the preceding subsection, the output-voltage magnitude is determined by the internal current conduction paths of the converter. When current flows through the capacitors, any voltage deviation directly affects the output voltage and consequently degrades the waveform quality of the output current. It is therefore necessary to analyze the mechanism by which capacitor voltage deviation influences the output waveform, so that a suitable control method can be developed for the converter under the extreme condition of large capacitor voltage fluctuations.

Taking phase A as an example, the internal current conduction paths of the converter under the eight switching states V0–V7 are shown in Fig. 2. The red lines indicate that the current flows only through the dc-link capacitors, the yellow

lines indicate that the current flows only through the flying capacitor, the blue lines indicate that the current flows through both the dc-link capacitors and the flying capacitor, and the green lines indicate that no current flows through any capacitor. The actual output-voltage magnitudes under these switching

Table 1 Switching state table of the 5L-ANPC converter

V_{xo}	S_{x1}	S_{x2}	S_{x3}	S_{x4}	S_{x5}	S_{x6}	S_{x7}	S_{x8}	i_{fx}	i_{NP}	Switch State
$2E$	1	0	1	0	1	0	1	0	0	0	V7
E	1	0	1	0	1	0	0	1	$-i_x$	0	V6
E	1	0	1	0	0	1	1	0	i_x	i_x	V5
0	1	0	1	0	0	1	0	1	0	i_x	V4
0	0	1	0	1	1	0	1	0	0	i_x	V3
$-E$	0	1	0	1	1	0	0	1	$-i_x$	i_x	V2
$-E$	0	1	0	1	0	1	1	0	i_x	0	V1
$-2E$	0	1	0	1	0	1	0	1	0	0	V0

Based on the previous analysis of the switching states in Table 1, capacitor voltage control is achieved through the selection of redundant switching states. Here, Δu_f is defined as the fluctuation threshold of the flying-capacitor voltage, and in this paper it is set to 0.3 times the supply voltage.

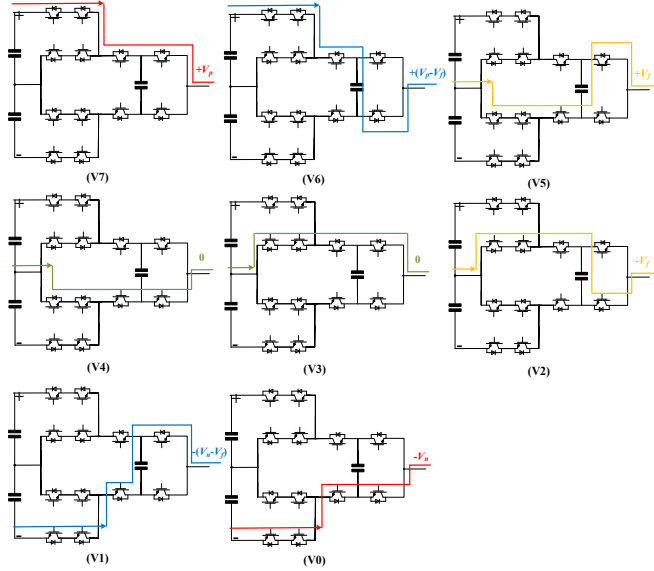


Fig. 2 switch states of ANPC-5L converter

3 Current THD Optimization Method Based on Optimized Modulation-Wave Amplitude

3.1 Ac side current of MPC

SPWM is widely adopted because of its simple algorithmic structure and ease of implementation. Therefore, this section employs a carrier-stacked scheme to address the multi-objective optimization problem under large capacitor voltage fluctuations.

Let v_x denote the modulation wave, where $x=a,b,c$. When the sampling period T_s is sufficiently small, v_x within each switching period can be approximated as a straight line. For the

states are also given in Fig. 2. It is observed that only the output voltages corresponding to V3 and V4 are unaffected by capacitor voltage fluctuation. Under the other six switching states, the output voltage varies with the capacitor voltages.

case $E < v_x < 2E$, taking the redundant switching state V5 as an example, the modulation wave and carrier wave are illustrated in Fig. 3. Under ideal conditions, where the capacitor voltages remain at their reference values, the output voltage within one switching period is $2E - E - 2E$. However, under actual operating conditions with capacitor voltage deviations, the corresponding output voltage becomes $V_p - V_f - V_p$. Based on the volt-second balance principle, this paper proposes a carrier-stacked method with optimized modulation-wave amplitude. Specifically, the modulation-wave amplitude is adjusted in real time according to the instantaneous capacitor voltages such that the time integral of the output voltage under actual conditions is equal to that under ideal conditions, i.e., the green area is equal to the orange area. In this way, the output current waveform quality can be improved under large capacitor voltage fluctuations.

As shown in Fig. 3, SPWM generates a symmetric three-segment switching sequence within each sampling period, and each sequence contains one redundant switching state. Owing to the symmetry of the switching sequence, the duty ratio of the vectors in the sequence can be represented by the dwell time of the redundant switching state. Let t_x denote the dwell time of the key redundant switching state under ideal conditions. Then, according to the similar-triangle relationship, t_x can be expressed as

$$t_x = \begin{cases} T_s \cdot (2E - v_x) / E, & E \leq v_x \leq 2E \\ T_s \cdot v_x / E, & 0 \leq v_x < E \\ T_s \cdot (-v_x) / E, & -E \leq v_x < 0 \\ T_s \cdot (2E + v_x) / E, & -2E \leq v_x < -E \end{cases} \quad (1)$$

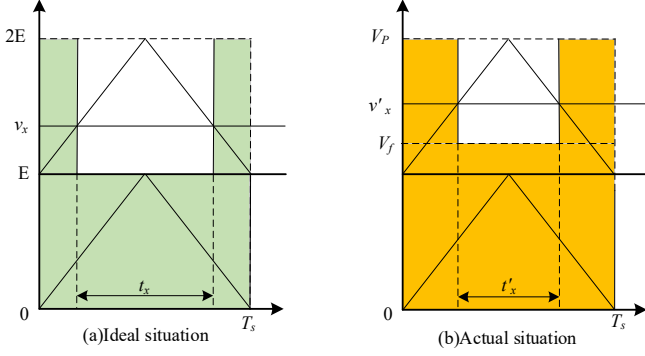


Fig. 3 Modulation wave, carrier wave and their integrated area

Similarly, by substituting the adjusted modulation wave v'_x into the above expression, the dwell time t'_x of the key redundant switching state under actual conditions can be obtained.

$$t'_x = \begin{cases} T_s \cdot (2E - v'_x) / E, & E \leq v'_x \leq 2E \\ T_s \cdot v'_x / E, & 0 \leq v'_x < E \\ T_s \cdot (-v'_x) / E, & -E \leq v'_x < 0 \\ T_s \cdot (2E + v'_x) / E, & -2E \leq v'_x < -E \end{cases} \quad (2)$$

Taking Fig. 3 as an example, the volt-second integral area s_1 under ideal conditions can be expressed as

$$s_1 = (T_s - t_x) \cdot 2E + t_x \cdot E \quad (3)$$

Under actual conditions, the volt-second integral area s_2 can be expressed as

$$s_2 = (T_s - t'_x) \cdot V_p + t'_x \cdot V_f \quad (4)$$

According to the volt-second balance principle, the two integral areas should be equal, i.e., $s_1 = s_2$. By jointly solving this relation with (1) and (2), the adjusted modulation-wave amplitude v'_x can be obtained as

$$v'_x = \frac{E \cdot (v_x - 2V_f + V_p)}{V_p - V_f} \quad (5)$$

The derivation of v'_x for the remaining operating conditions follows the same procedure and is thus omitted for brevity. According to the original modulation-wave amplitude v_x and the selected key redundant switching state, the calculation expressions of the optimized modulation wave v'_x are shown in Fig. 4.

Table 2 Optimized modulation wave expression

	Expression of the Optimized Modulation Wave	The Selected Key Redundant Switching States
$E \leq v_x \leq 2E$	$v'_x = \frac{E \cdot v_x - 2V_f + V_p}{V_p - V_f}$	V5
	$v'_x = \frac{E \cdot v_x + 2V_f - V_p}{V_f}$	V6
$0 \leq v_x < E$	$v'_x = \frac{E \cdot v_x}{V_f}$	V5

$$\begin{aligned} v'_x &= \frac{E \cdot v_x}{V_p - V_f} & \text{V6} \\ v'_x &= \frac{E \cdot v_x}{V_f} & \text{V2} \\ -E \leq v_x < 0 & \\ v'_x &= \frac{E \cdot v_x}{V_n - V_f} & \text{V1} \\ v'_x &= \frac{E \cdot v_x + 2V_f - V_n}{V_n - V_f} & \text{V2} \\ -2E \leq v_x < -E & \\ v'_x &= \frac{E \cdot v_x - 2V_f + V_n}{V_f} & \text{V1} \end{aligned}$$

In summary, the control flow of the proposed method is shown in Fig. 4. The method consists of two stages. The first stage is capacitor voltage control, which is achieved through the selection of redundant switching states. The second stage is current harmonic optimization. In this stage, the modulation-wave amplitude is calculated from the volt-second balance principle while taking capacitor voltage fluctuation into account, and the action durations of the key redundant switching states are then determined from the planar geometric relationship between the modulation wave and the triangular carrier. Finally, the switching signals for the power devices are generated.

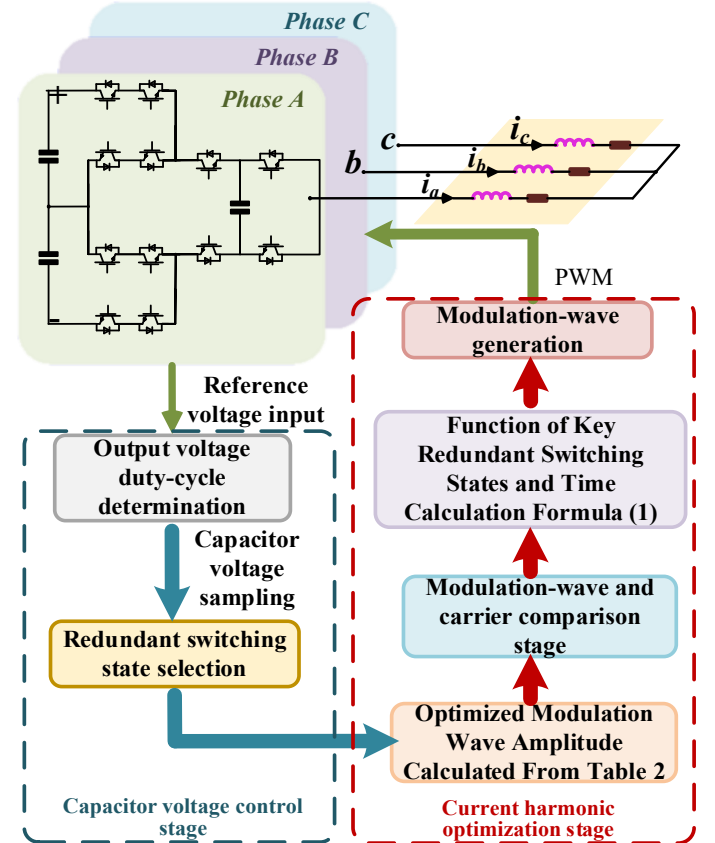


Fig. 4 Control diagram of the proposed algorithm

4 Simulation and Experimental Verification

4.1 Simulation Validation

To verify the effectiveness of the proposed method, simulations are first conducted in Matlab/Simulink.

A simulation model was established to validate the effectiveness of the proposed method, and two operating conditions were designed for comprehensive evaluation.

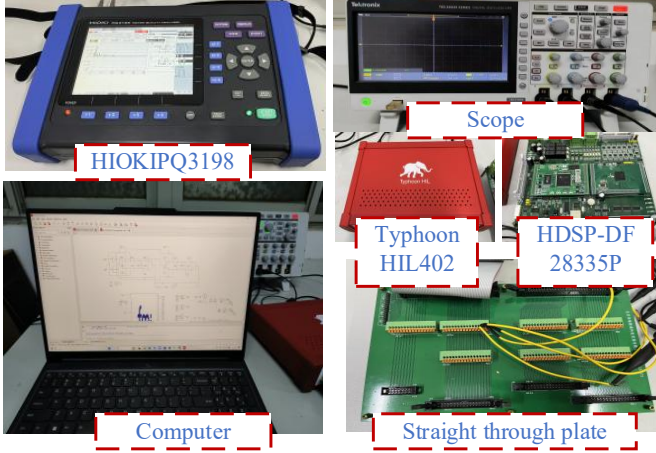


Fig. 5 Single phase ANPC-5L inverter platform based on Typhoon HIL402

Condition 1: To emulate the operating scenario of electrolytic-capacitorless motor drives, small-capacitance film capacitors are used to replace conventional large-capacitance electrolytic capacitors. In this case, both the dc-link capacitor and the flying capacitor are set to $500\mu\text{F}$ to evaluate the converter control performance under small-capacitance conditions. The sampling frequency is set to 2kHz .

Table 3 The main parameters of case 1 and 2

Parameters	Conditions 1	Conditions 2
DC source voltage V_{dc}	400 V	400 V
DC-link capacitor C_{up} & C_{dn}	$500\mu\text{F}$	$3000\mu\text{F}$
Flying capacitor C_{fs}	$500\mu\text{F}$	$1000\mu\text{F}$
Sampling frequency f_c	2 kHz	1 kHz
System frequency f	50 Hz	50 Hz
Load inductance L	5 mH	5 mH
Load resistance R	10Ω	10Ω

Condition 2: To emulate the operating scenario of high-power drives under low-switching-frequency operation, the system sampling frequency is reduced to 1kHz . Under such conditions, capacitor voltage fluctuations become more significant and may degrade the converter output performance. In this case, the dc-link capacitor and the flying capacitor are maintained at their nominal values to evaluate the control performance of the proposed algorithm under low-switching-frequency conditions.

The main parameters of Operating Conditions 1 and 2 are listed in Table 3.

Under Operating Condition 1, the output voltage, output current, and THD of the 5L-ANPC converter are shown in Fig. 6, while the flying-capacitor voltage and dc-link capacitor voltages are shown in Fig. 7. It can be observed that the relatively small capacitance values limit the charge storage

capability of the capacitors, resulting in significant voltage fluctuations. Specifically, the peak-to-peak fluctuation of the flying-capacitor voltage is about 65V , whereas that of the dc-link capacitor voltage is about 30V . Due to these large capacitor voltage fluctuations, the output voltage still maintains the five-level characteristic, but exhibits obvious distortion, which further degrades the sinusoidal quality of the output current. Under the conventional method, the output current THD is 4.77% . In contrast, by considering the effect of capacitor voltage fluctuations based on the volt-second balance principle, the proposed method reduces the output current THD to 2.97% , corresponding to a 37.7% reduction in harmonic content.

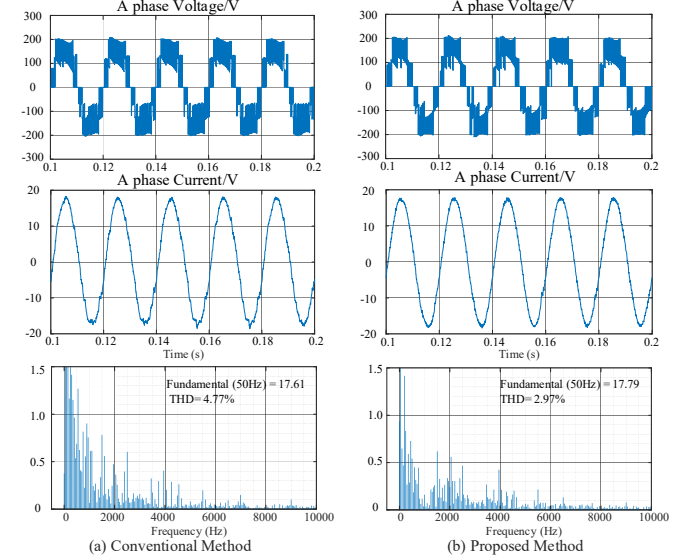


Fig. 6 Output voltage, current, and harmonic analysis in case 1

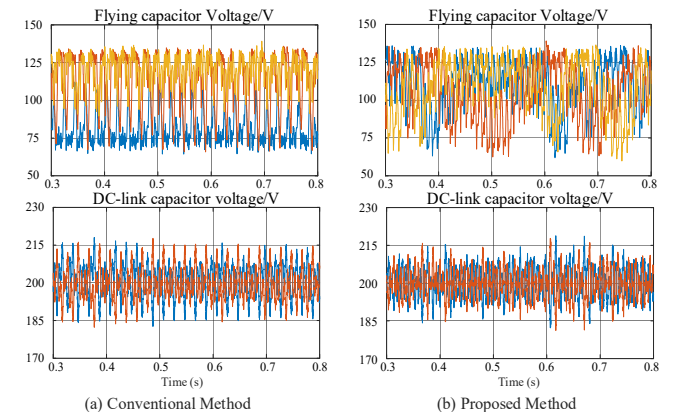


Fig. 7 Capacitors' voltages in case 1

Under Operating Condition 2, the output waveforms of the control system and the corresponding harmonic analysis are shown in Fig. 8, while the flying-capacitor voltage and dc-link capacitor voltages are shown in Fig. 9. It can be observed that the reduced sampling frequency leads to a longer carrier period and lower reference-voltage tracking accuracy of the control algorithm. This not only weakens the capacitor voltage regulation capability, but also degrades the sinusoidal quality of the output waveform. When the sampling frequency is reduced to 1kHz , the peak-to-peak fluctuation of the flying-capacitor

voltage is about 75V, whereas that of the dc-link capacitor voltage is about 7V.

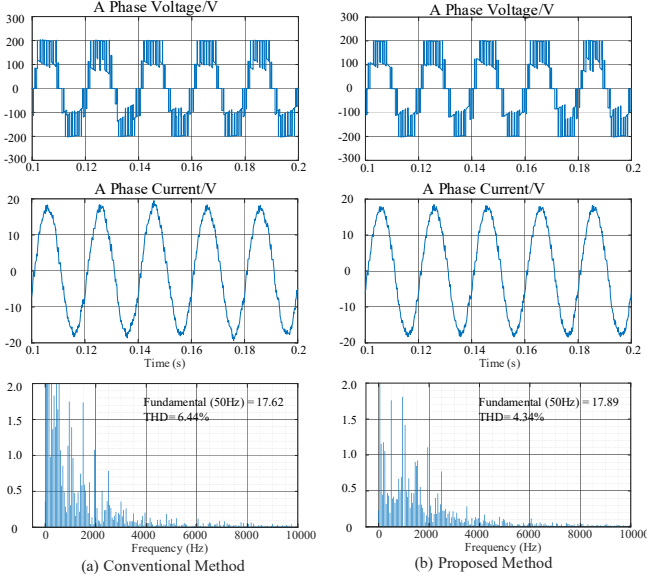


Fig. 8 Output voltage, current, and harmonic analysis in case 2

Because the control algorithm is simultaneously affected by capacitor voltage fluctuations and limited calculation accuracy, the output voltage under Operating Condition 2 also exhibits severe distortion, and the harmonic content of the output current is higher than that under Operating Condition 1. Under the conventional method, the output current THD is 6.44%, whereas the proposed method reduces it to 4.34%, corresponding to a reduction of about 32.6%.

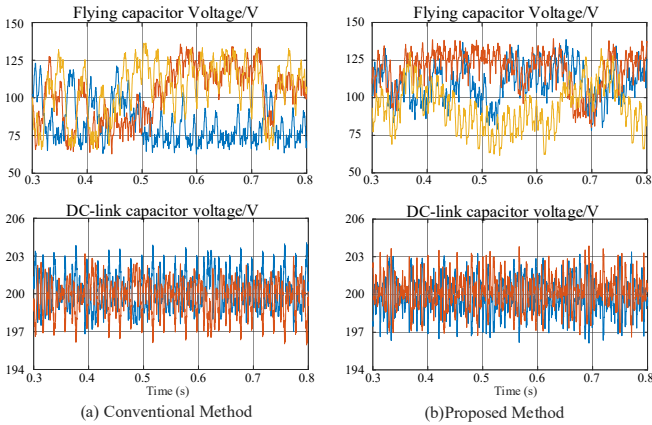


Fig. 9 Capacitors' voltages in case 2

4.2 Experimental Validation

To further validate the effectiveness of the proposed method, a three-phase 5L-ANPC converter experimental platform was established based on Fig. 5, and the experimental parameters were set identical to the simulation parameters. Under Operating Condition 1, the experimental waveforms of the conventional method and the proposed method at a high modulation index ($m=0.8$) are shown in Fig. 10, whereas the corresponding results at a low modulation index ($m=0.4$) are shown in Fig. 11.

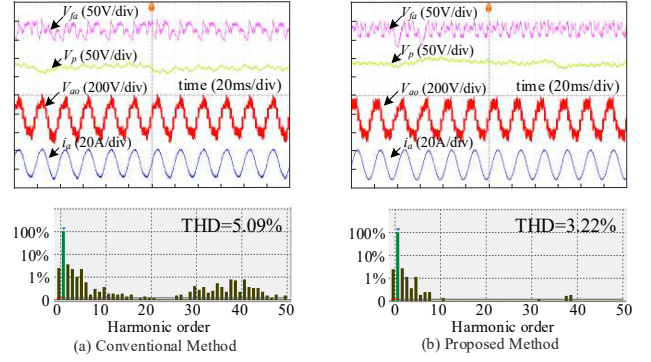


Fig. 10 Experimental waveforms under case 1 when the system is in high modulation

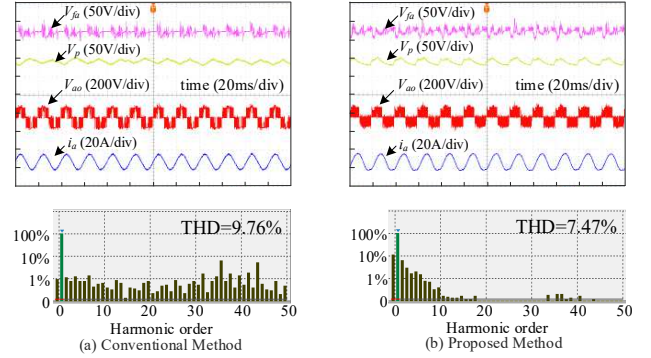


Fig. 11 Experimental waveforms under case 1 when the system is in low modulation

When the modulation index is high, the phase voltage exhibits a five-level stepped waveform. Under low-capacitance conditions, the peak-to-peak fluctuation of the flying-capacitor voltage is about 50V for both the conventional method and the proposed method, whereas the peak-to-peak fluctuation of the dc-link capacitor voltage is about 30V. Compared with the conventional method, the proposed method reduces the current THD by 36.7%. When the modulation index is low, the phase voltage exhibits a three-level stepped waveform. In this case, the peak-to-peak fluctuation of the flying-capacitor voltage is about 40V for both methods, whereas the peak-to-peak fluctuation of the dc-link capacitor voltage is about 25V. Compared with the conventional method, the proposed method reduces the current THD by 23.5%.

Under Operating Condition 2, the experimental waveforms of the conventional method and the proposed method at a high modulation index are shown in Fig. 12, whereas the corresponding results at a low modulation index are shown in Fig. 13.

Similar to the experimental results under Operating Condition 1, under Operating Condition 2, the phase voltage exhibits a five-level stepped waveform when the modulation index is high. Under reduced control-frequency conditions, the peak-to-peak fluctuation of the flying-capacitor voltage is about 55V for both the conventional method and the proposed method, whereas the peak-to-peak fluctuation of the dc-link capacitor voltage is about 8V. Compared with the conventional method, the proposed method reduces the current THD by 30.8%. When the modulation index is low, the phase voltage exhibits a three-level stepped waveform. In this case, the peak-to-peak

fluctuation of the flying-capacitor voltage is about 40 V for both methods, whereas the peak-to-peak fluctuation of the dc-link capacitor voltage is about 6V. Compared with the conventional method, the proposed method reduces the current THD by 17.9%.

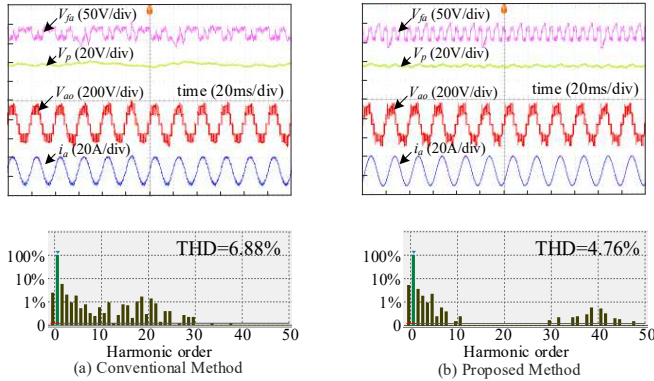


Fig. 12 Experimental waveforms under case 2 when the system is in high modulation

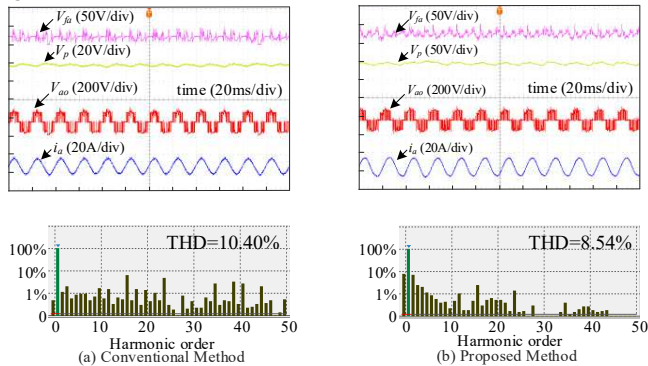


Fig. 13 Experimental waveforms under case 2 when the system is in low modulation

5 Conclusion

This paper addresses a control problem that has not been sufficiently investigated in converters operating under large capacitor voltage fluctuations and proposes a carrier-based current harmonic optimization method. First, the influence of capacitor voltage fluctuation is theoretically analyzed on the basis of the topology of the 5L-ANPC converter. For different switching states, the actual output-voltage values of the converter under capacitor voltage imbalance are clarified. Then, by incorporating the volt-second balance principle, the implementation procedure of the proposed harmonic optimization strategy is analyzed in detail. Finally, simulation and experimental results verify the effectiveness of the proposed method. Under a high modulation index, the current THD is reduced by 36.7% and 30.8% in simulation and experiment, respectively. Under a low modulation index, the corresponding reductions are 23.5% and 17.9%. This work provides a new approach for improving converter performance in electrolytic-capacitor-free motor drives and under high-power operating conditions with low switching frequency.

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