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Impact of the gate oxide material composition on the self-heating and short channel effects in nanosheet field effect transistor

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Abstract

This study investigates a nanosheet field-effect transistor with a gate oxide composed of two oxide layers: SiO_2 and HfO_2. Using simulation-based analysis, this study focused on the impact of the gate dielectric composition on the self-heating effect, DIBL effect, subthreshold swing (SS), and switching ratio I_{on}/I_{off}. Specifically, we consider the impact of the thickness ratio R of the SiO_2 and HfO_2 layers under a constant equivalent gate oxide thickness. Unlike previous works, the dependence of the thermal conductivity on the thickness of the SiO_2 and HfO_2 layers was accounted for in the simulation of the self-heating effect. The temperature difference over the entire range of the considered ratios R, with and without accounting for the thickness dependence of the thermal conductivity of the SiO_2 and HfO_2 dielectric layers, does not exceed 0.5 K. The simulation results indicate that, as the ratio R increases from 1.286 to 10.154, the drain-induced barrier lowering effect increases by 34%, the subthreshold swing increases by 5.7%, and the I_{on}/I_{off} ratio decreases by 52%.

The observed variations associated with changes in the thickness ratio of the gate dielectric layers are attributed to modifications in the electrostatic potential distribution in the channel and to a change in the threshold voltage, caused by edge effects within the channel.

Keywords: nanosheet field-effect transistor, self-heating, short channel effects, Joule heat, heat dissipation, thermal conductance.

1. Introduction

The advancement of information technologies and artificial intelligence requires substantially larger memory capacity and increased energy consumption. Addressing this challenge is inherently linked to increasing the integration density of elements in integrated circuits while simultaneously reducing their power consumption. One of the key approaches to achieving this is the scaling of device dimensions within integrated circuits, particularly metal–oxide–semiconductor (MOS) transistors, which constitute the fundamental building blocks of most modern electronic systems. However, continuous transistor scaling to significantly reduce power consumption and increase integration density should be done without degrading device performance. To meet these scaling requirements, various advanced transistor structures have been proposed. In particular, following planar MOS transistors, multi-gate FinFETs were proposed [1–3].

The relatively recent development is the stacked nanosheet field-effect transistor (SNSHFET), which is based on horizontally aligned nanosheets fully surrounded by a gate [4, 5]. The SNSHFET enabled vertical nanosheet stacking with varying channel widths within the same footprint. Such architectures make it possible to fabricate transistors with gate lengths of less than 7

nm. These devices also demonstrate superior switching speed and optimized power-performance trade-offs compared to multigate FinFET structures [6].

The continued downscaling of transistor dimensions leads to the enhancement of various degradation effects, particularly short-channel effects such as drain-induced barrier lowering (DIBL), and an increase in subthreshold swing (SS) [7, 8, 9]. In addition, scaling of SNSHFET dimensions induces the self-heating effect (SHE) [10–13]. The self-heating effect arises because, in the SNSHFET architecture, the transistor channel is fully surrounded by the gate dielectric, which reduces heat dissipation from the channel and increases its temperature. The reduced heat-dissipation rate is primarily attributed to the low thermal conductivity of the gate dielectric materials.

Numerous studies have been devoted to the investigation of short-channel effects (drain-induced barrier lowering (DIBL) and subthreshold swing (SS)) in nanosheet FETs [14–19]. The influence of various factors on these effects has been examined. In particular, works [14,15] analyze the impact of geometrical parameters, such as nanosheet thickness and width [14], as well as gate length [15], on the switching ratio, drain-induced barrier lowering (DIBL), and subthreshold swing (SS). In addition, the impact of device-to-device interference on the electrical behavior of adjacent nanosheet FETs has been investigated using TCAD simulations. It was demonstrated that both off-state current (I_{OFF}), and short-channel effects (SCEs) immunity are significantly affected by adjacent NS FETs ' on/off operation [16]. Several studies have analyzed the influence of spacer material on the DC and analog performance of nanosheet FETs [17–19]. A comprehensive evaluation of key performance parameters, including transfer characteristics, threshold voltage, switching ratio, DIBL effect, and SS, was conducted for the NS FETs with various spacer region configurations, including single-K materials (Air, SiO_2) and dual-K combinations (HfO_2+SiO_2, Nitride + HfO_2) [17]. The impact of dual-*k* spacer combinations-such as HfO_2+Air, HfO_2+Si_3N_4, Al_2O_3+Air, Al_2O_3+Si_3N_4, and Al_2O_3+SiO_2-on the DC characteristics of SNSHFETs, including ON current (I_{ON}), I_{ON}/I_{OFF} ratio, subthreshold swing, and drain-induced barrier lowering, has also been investigated [18,19].

An analysis of these and other publications indicates that there is a lack of studies dedicated to examining the influence of the gate dielectric stack composition on DC performance, particularly on the switching ratio, drain-induced barrier lowering (DIBL), and subthreshold swing (SS) of nanosheet FETs.

Several studies have investigated the self-heating effect in nanosheet FETs [5, 20, 21, 22]. In [20], the SHE-induced performance degradation was examined, particularly its impact on the $I_D - V_{GS}$ characteristics of nanosheet FETs. The work [21] explored the analog/RF and linearity performance of NSFETs under the influence of self-heating, with comparative results presented for cases with and without an SHE. The effect of the number of nanosheets on device temperature was also analyzed. In [5], the influence of the geometrical parameters of the in situ oxide, high-k oxide, and nanosheet dimensions on the self-heating behavior was investigated. Reference [22] studied the impact of varying the number of sheets/fins on key performance metrics, such as transconductance, total gate capacitance, and lattice temperature, while accounting for SHE.

The gate dielectric material, its geometrical parameters, and its composition play a significant role in the aforementioned degradation effects, as the gate dielectric in nanosheet FETs typically consists of two stacked layers: SiO_2 and HfO_2 [5, 21, 22]. In our previous work [23], the influence of the gate dielectric stack composition on the self-heating effect was investigated. It was shown that the composition of the gate dielectric significantly affects the channel temperature. However, in that study, the thickness dependence of the thermal conductivity of SiO_2 and HfO_2 layers at nanoscale dimensions was not taken into account, and the impact of the dielectric stack composition on short-channel effects was not considered. Therefore, the main objective of this work is to investigate how the composition (i.e., thickness ratio of SiO_2 and HfO_2 in the gate dielectric stack) affects the self-heating and short-channel effects behavior in stacked nanosheet field-effect transistors.

The key contributions of this work are as follows: investigation of the impact of the gate dielectric composition and geometrical dimensions on the self-heating effect, on short-channel effects such as the DIBL effect and Subthreshold Swing (SS), and switching ratio I_{on}/I_{off} of the transition I-V curve.

The remainder of this paper is organized as follows. Section 2 discusses the device dimensions and validation of the TCAD simulation models by comparing the simulation results with experimental data and provides detailed aspects of the simulation of the nanosheet FET. In Section 3, the simulation results and discussion are presented. This section is divided into three parts. Finally, the limitations of this research and future research proposal are described in Section 4, Section 5 presents the conclusions of this study.

2. Simulation approach and Transistor parameters

TCAD Sentaurus was used to 3D simulations study of the SNSHFET. The transistor structure was designed using Sprocess, where the technological parameters were selected from the data presented in [5]. The resulting transistor structure obtained from Sprocess is shown in Fig. 1. The values of the geometric parameters shown in Fig. 1 are listed in Table 1. The gate dielectric of the transistor consists of two layers: a SiO_2 layer adjacent to the channel and an HfO_2 layer above it.

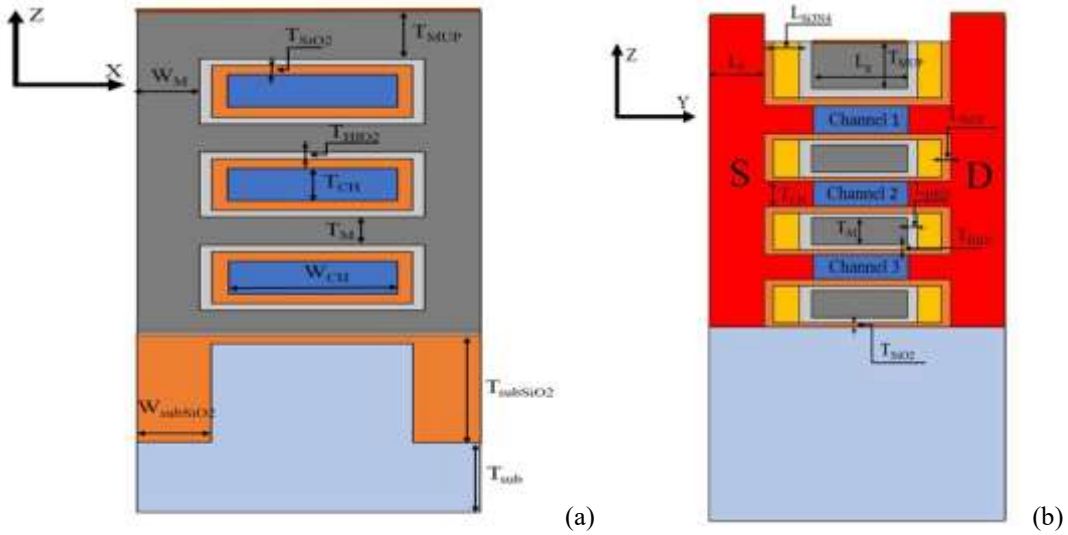


Fig. 1. Cross-sectional views of the modeled SNSHFET: (a) transverse to the channel and (b) longitudinal along the channel.

The source and drain are arsenic-doped following a Gaussian distribution with a peak concentration of 3×10^{20} cm^{-3}, whereas the channel is uniformly boron-doped to 1×10^{17} cm^{-3}.

Table 1. Geometrical parameter values of the transistor shown in Fig. 1.

L_g	L_{SiO2}	L_{Si3N4}	L_{HfO2}	$L_S = L_D$	T_{CH}	T_{SiO2}	T_{HfO2}	$T_{subSiO2}$	T_M	T_{MUP}	W_{CH}	W_M
12 nm	0.5 nm	4.25 nm	1.28 nm	10 nm	5 nm	0.55 nm – 0.25 nm	0.846 nm – 2.538 nm	50 nm	4.5 nm	16 nm	50 nm	10 nm

For simulation of the SNSHFET characteristics, as well as in [23], a thermodynamic transport model was employed, which accounted for both drift–diffusion transport and thermoelectric effects.

Shockley-Read-Hall (SRH) recombination, commonly used in silicon-based devices, was implemented to model the carrier recombination processes. In addition to the Shockley–Read–Hall (SRH) recombination model, the nonlocal Schenk recombination model was also employed.The mobility model accounts for the doping-dependent mobility degradation and carrier velocity saturation at high electric fields. Because the channel dimensions are on the order of 10 nanometers, quantum confinement effects were accounted for using the eQuantumPotential quantum correction model.

The simulation model was calibrated by comparing the simulated transfer current-voltage characteristics with the experimental ones obtained for a transistor with identical parameters, as reported in [24] (Fig.2).

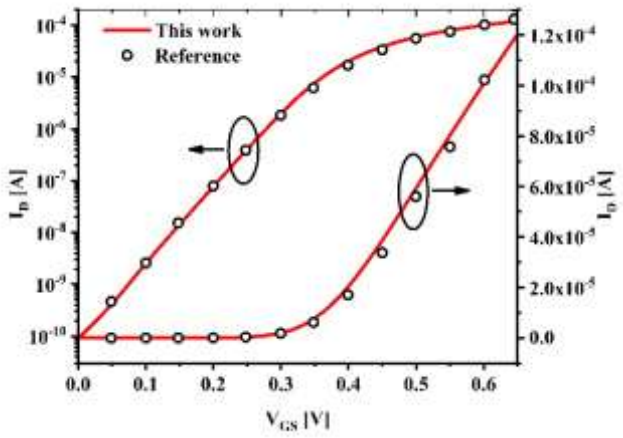


Fig. 2. Comparison of the transfer I_D–V_{GS} characteristics of the simulated and experimental SNSHFET.

In this study, the impact of the thickness ratio between the SiO_2 layer (T_{SiO_2}) and HfO_2 layer (T_{HfO_2}) of the gate dielectric on the self-heating effect (SHE), DIBL effect, and SS was investigated. The dependence of the SHE, DIBL, and SS on the ratio $R=T_{HfO2}/T_{SiO2}$ of the HfO_2 and SiO_2 thicknesses was modeled while maintaining the equivalent thickness of the gate dielectric unchanged.

The condition for maintaining the equivalent thickness is related to the requirement of the gate dielectric capacitance to remain unchanged when the dielectric thickness is modified. As mentioned in our previous work [23], the capacitance of the gate dielectric consisted of parallel-connected horizontal capacitance (C_H) and lateral capacitance (C_L) components (Fig. 3). Because the channel width (W_{CH}=50 nm) is considerably larger than the thickness ($T_{CH}=T_{Si}$=5 nm) of the dielectric layer, the horizontal component of capacitance C_H can be approximated as a parallel plate capacitor. Therefore, when changing the composition of the gate dielectric, to determine the range of thicknesses for T_{SiO_2} and T_{HfO_2}, whose combination corresponds to

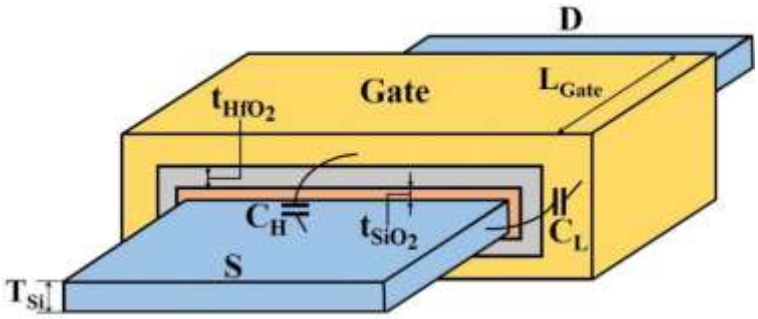


Fig. 3. Transistor channel structure showing the horizontal C_H and lateral C_L gate capacitances.

the equivalent thickness t_{eqv}, we use the formula (1), derived from the condition of constant capacitance:

$$\frac{1}{t_{eqv}} = \frac{\varepsilon_{HfO_2}}{\varepsilon_{SiO_2} T_{HfO_2} + \varepsilon_{HfO_2} T_{SiO_2}} \quad (1)$$

where ε_{SiO2} and ε_{HfO2} are the dielectric constants of SiO_2 and HfO_2, respectively. In our case, t_{eqv} is set to 0.7 nm. The lateral component C_L was also approximated using the parallel-plate capacitor model, although the edge effects, as it was shown in our previous work [23], influenced it. These edge effects were neglected in estimating the equivalent oxide thickness.

Using equation (1), the ranges of T_{HfO_2} and T_{SiO_2} values corresponding to the equivalent oxide thickness were determined (see Table 2). Table 2 also presents the range of the ratio $R=T_{HfO2}/T_{SiO2}$, which reflects the compositions of the gate dielectric layers investigated in this work for their impact on the self-heating effect.

Table 2. Values of the ratio R used in the simulations, which correspond to equivalent dielectric thickness.

№	1	2	3	4	5	6	7	8
T_{SiO2}, nm	0.57	0.55	0.5	0.452	0.4	0.35	0.29	0.25
T_{HfO2}, nm	0.733	0.846	1.128	1.399	1.692	1.974	2.313	2.538
R	1.286	1.538	2.256	3.095	4.230	5.641	7.975	10.154

3. Results and discussion.

3.1 Effect of Gate Dielectric Stack Composition on Self-Heating

The dependence of the self-heating effect on the gate dielectric stack composition was previously examined in our earlier work [23]. However, in that study, although the dielectric layer thicknesses were in the nanoscale regime, the thickness dependence of the thermal conductivity of the dielectric layers was not taken into account. In nanoscale structures, phonon-boundary scattering becomes a dominant mechanism limiting thermal transport when the characteristic dimensions approach the phonon mean free path. Under such conditions, the effective phonon mean free path is primarily constrained by the smallest geometric dimension of the structure [25]. Therefore, in this work, the dependence of the self-heating effect on R was investigated, taking into account the thickness dependence of the thermal conductivity of the dielectric layers. The thickness-dependent thermal

conductivity of HfO_2 and SiO_2 layers, extracted from the results reported in [26,27], is shown in Fig. 4. These dependencies were incorporated into the simulation of channel-centre temperature as a function of the ratio R.

To investigate the impact of the dielectric layer composition on the self-heating effect (SHE), the temperature at the center of the 2-nd (central) channel was used as an indicator. The simulation results for the dependence of the channel center temperature on the thickness ratio R of the SiO_2 and HfO_2 layers are shown in Fig. 5.

The rate of heat generation and dissipation determines the resulting temperature in the channel. Heat generation in the channel occurs due to Joule heating, which results from current flowing through it. Heat dissipation from the channel occurred through the gate dielectric layer. The rate of heat generation depends on the drain current, which is determined by the dielectric constant of the gate dielectric, whereas the rate of heat dissipation depends on the thermal conductivity of the same gate dielectric material. Therefore, the composition of the gate dielectric layer plays an important role in setting a specific temperature in the channel.

It is well known that the resulting temperature in the channel is determined by the balance between the rates of heat generation and dissipation. To explain the observed temperature behavior with increasing R, in work [23], the rates of heat generation and dissipation in the transistor channel were estimated and compared. It was shown that across the entire range of R, the power of Joule heat generation exceeds the dissipated heat flux by approximately two orders of magnitude.

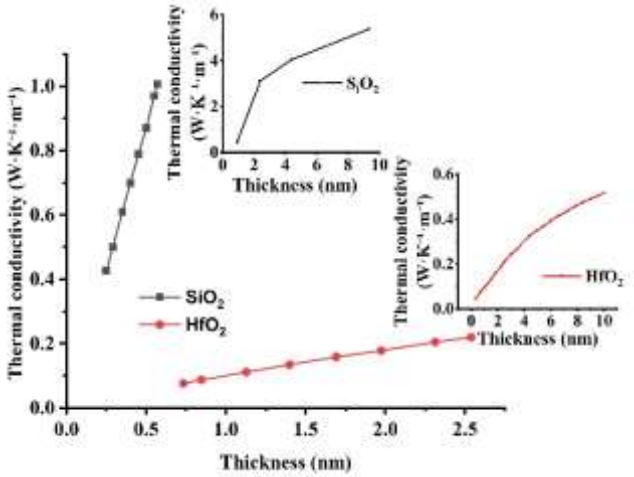


Fig.4.Thickness dependence of the thermal conductivity of SiO_2 and HfO_2 layers. The insets show plots adapted from works [26,27] of the thermal conductivity versus layer thickness for HfO_2 [26] and SiO_2 [27] over a wider thickness range.

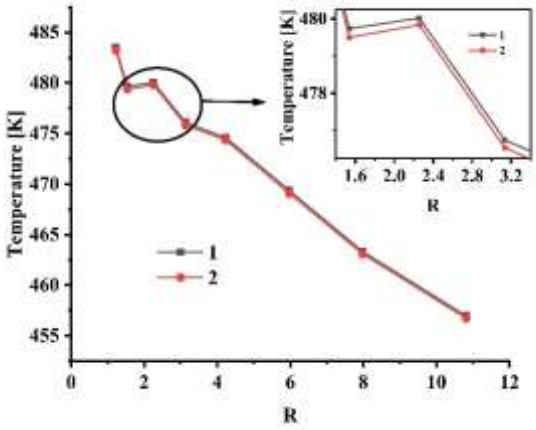


Fig. 5. Dependence of the channel center temperature Tch on the ratio R. The channel width-to-thickness ratio is W_{ch}/T_{ch} = 10.

It is also shown that the dependence of the channel center temperature on R fully correlates with that of the drain saturation current (Fig. 6), thereby explaining the observed behavior of the channel temperature. Step-like behavior at small R and decreasing the I_{Dsat} and consequently the temperature T with increasing R, as explained in [23], is likely associated with edge effects occurring in the lateral regions of the channel.

Figure 5 illustrates the dependence of temperature on R, both with consideration of the thickness-dependent thermal conductivity (Fig. 5, curve 1) and without accounting for this dependence (Fig. 5, curve 2). The simulation result for the temperature dependence on R, assuming constant (thickness-independent) thermal conductivity of the SiO_2 and HfO_2 dielectric layers, is taken from our previous work [23].

As shown in the figure, in both cases the temperature generally decreases with increasing R; however, when the thickness dependence of the dielectric thermal conductivity is taken into account, the temperature is slightly higher (by approximately 0.5 K) than in the case of constant thermal conductivity.

The simulation results indicate that incorporating the thickness dependence of the dielectric thermal conductivity does not significantly affect the considered relationship. This is evidently due to substantial heat dissipation from the channel not only through the gate, but also via the source and drain regions.

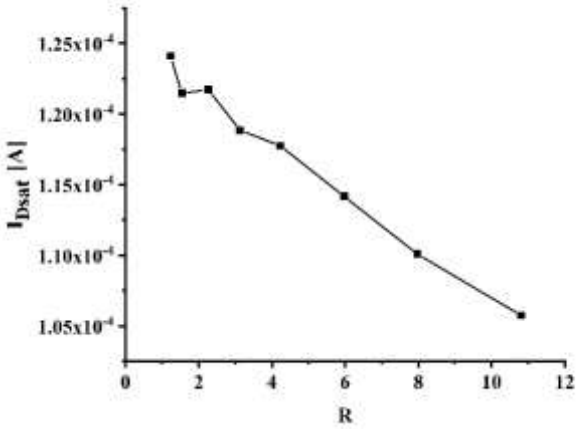


Fig. 6. Dependence of the saturation drain current on the ratio R. W_{ch}/T_{ch} =10, V_{GS}=0.65 V, V_D=0.65 V

Thus, the results indicate that as the ratio R increases from 1.286 to 10.154, corresponding to an increase in the fraction of the HfO_2 layer (see Table 2), the temperature rise due to the self-heating effect decreases from 482 K to 457 K, indicating a suppression of the self-heating effect by approximately 25 K.

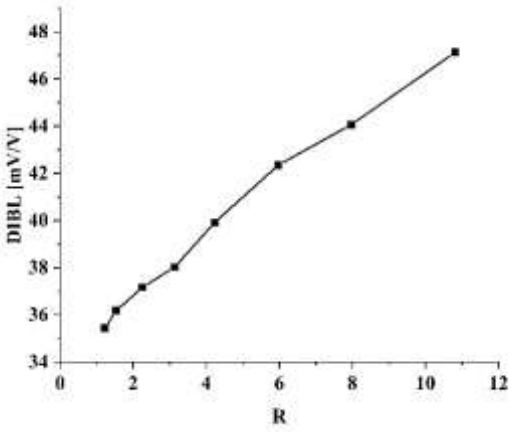
3.2. Dependence of the DIBL Effect on Gate Dielectric Stack Composition

The simulation results illustrating the dependence of the DIBL effect on the dielectric stack composition are presented in Fig. 7. The shown increase in the DIBL effect can be explained in the context of a simple model describing the capacitive coupling between the channel and the device electrodes, proposed in [28]**.** Within the context of a simple model, the modified expression for DIBL is expressed as follows [28]:

$$DIBL = \frac{C_G}{C_D} \qquad (2)$$

where C_G and C_D are gate-channel and drain-channel coupling capacitances, respectively (Figure 8). Two components contribute to the drain-channel capacitance (C_D): the capacitive coupling through the channel layer ($C_{D.ch}$) and the coupling through the gate oxide ($C_{D.ox}$). Therefore, the drain-channel capacitance (C_D) is expressed as follows:

$$C_D = C_{D.ch} + C_{D.ox} \qquad (3)$$



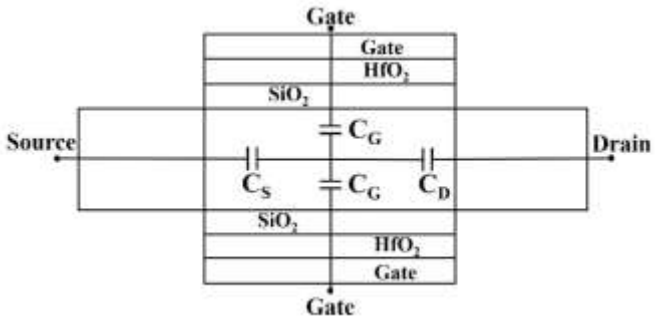


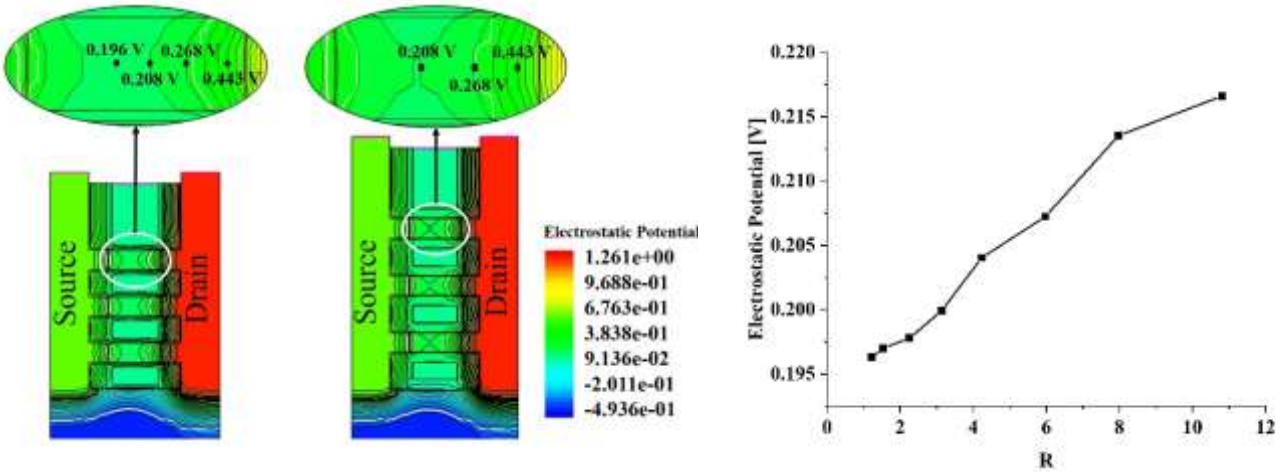
Fig.7. Dependence of the DIBL effect on the ratio R.

Fig.8.Equivalent circuit describing the capacitive coupling between the channel and the device electrodes in one of the channels of SNSHFET

At the simulation of transistor characteristics at different values of R, to satisfy the condition of a constant equivalent gate dielectric thickness, the gate–channel capacitance C_G was approximated using a parallel-plate capacitor model and assumed to remain invariant. Therefore, according to Eq. (2), variations in the DIBL effect can be attributed solely to changes in the lateral drain–channel capacitance C_D.

Based on the definition of capacitance, the channel potential U_{CH} can be considered inversely proportional to the lateral capacitance, i.e., $U_{CH} \propto 1/C_D$. Simulation results of the potential distribution along the channel indicate that the channel potential increases with increasing R (Fig. 9). This increase in channel potential with R implies a reduction in C_D, which explains the observed enhancement of the DIBL effect as R increases.

The decrease in C_D with increasing R can be attributed to a reduction in its oxide-related component $C_{D,ox}$, which is evidently caused by longitudinal (with respect to channel length) edge effects that become significant at reduced channel dimensions.



R=1.28 R=10.154 (b)

(a)

Fig. 9. (a) Potential distribution along the channel for R=1.28R = 1.28R=1.28 and R=10.154R = 10.154R=10.154. (b) Dependence of the potential at the center of the second (middle) channel on the ratio R. V_G=0 , V_{DS}=0.65 V.

Thus, the simulation results of the dependence of the DIBL effect on the composition R show that with an increase in the ratio R from 1.286 to 10.154, the value of the DIBL effect increases by 34%, although the absolute values of the DIBL effect in the entire considered range of R are not very large and do not exceed the target values [29, 17, 30].

3.3. Dependence of SS and the ratio I_{on}/I_{off} on the composition of the dielectric layer.

The results of simulation of the I_d-V_g characteristics show that the composition of the gate dielectric also affects the subthreshold swing SS (Fig. 10). SS monotonically increases with increasing the ratio R in all ranges, except for the range of

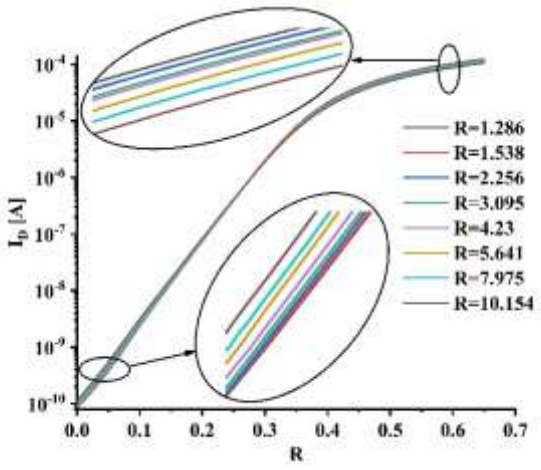


Fig.10. Transfer I_d-V_g characteristics of the transistor at different values of the R. V_g=0.65 V, V_{ds}=0.65 V

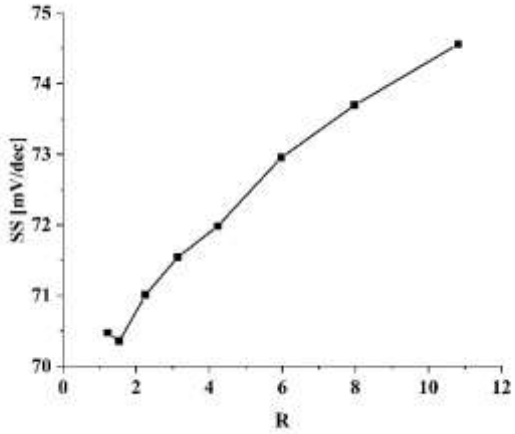


Fig.11. Dependence of SS on the ratio R. V_g=0.65 V V_{ds}=0.65 V

values R<2 (Fig. 11). The increase in SS can be explained based on the simple expression (4) for SS presented in [31]:

$$SS \propto \left(1 + \frac{C_{dep}}{C_G}\right) \qquad (4)$$

where C_{dep} is the capacitance of the depleted layer at the channel-dielectric interface, C_G, as mentioned above, is the capacitance of the gate dielectric. C_{dep} depends on the dielectric permittivity of the channel material and the level of channel doping, and does not change with changes in R. Although the capacitance of the gate dielectric C_G, was approximated as a flat capacitor and treated as constant with increasing the ratio R, it decreases with increasing R due to the lateral (with respect to the channel length) edge effect shown in [23]. This is also evidenced by the decrease in drain current with an increase in R (Fig.6). Thus, the increase in SS with an increase in R is associated with a decrease in CG capacitance caused by edge effects relative to the channel. The increase of SS with the ratio R leads to an increase in the threshold voltage and, accordingly, to a decrease in the switching ratio Ion/Ioff (Fig.12). In the considered range of R, the Ion/Ioff values are decreasing, although not less than up to the critical values: 10^4 - 10^5 .

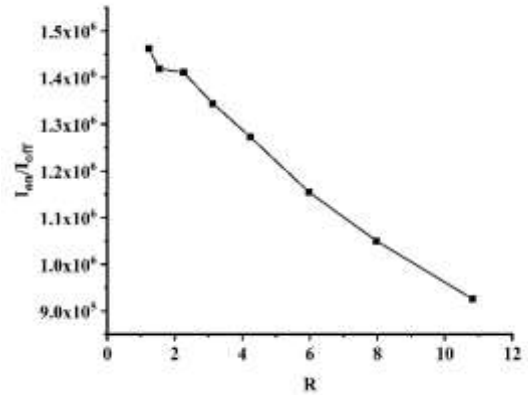


Fig.12. Dependence of switching ratio I_{on}/I_{off} on R. V_g=0.65 V, V_{ds}=0.65 V.

The results show that within the considered range of the ratio R, SS values increase by 5.7%, while the Ion/Ioff switching ratio decreases by 52%. These specified changes of SS do not lead to a significant exceedance of their values beyond the target ranges [24, 32, 33]. Ion/Ioff values are within the frame of the target values, and their changes also do not lead to exceeding practical target values [17, 33, 34].

4. Limitations of This Research and Future Research Proposal.

In this study, the dependence of degradation effects such as self-heating effect, DIBL effect, and SS on the composition of the gate oxide layer was investigated in detail. At the same time, however, this study has the limitations listed below, which are planned to be addressed in the future research.

Values of $R \leq 1$ correspond to HfO_2 layer thicknesses that are less than or equal to the thickness of the SiO_2 layers. In this work, these regions of R were not considered in detail. At small values of R (around 1), variations in temperature and saturation current are observed, which disappear as R increases. These small R regions are interesting from both a physics perspective and a practical standpoint. In this region, although higher self-heating temperatures are observed, short-channel effects (DIBL effect and SS) are small, and Ion/Ioff values are higher than at high R.

It is known that at nanometer transistor sizes, quantum capacitance can also contribute to the capacitance of the depleted layer in the channel [35, 36]. Therefore, it would be reasonable to also assess the contribution of quantum capacitance at small R values, which manifests at small channel sizes.

The observed self-heating behavior highlights the need to optimize the thickness ratio of the SiO_2 and HfO_2 gate dielectric layers in SNSHFET design to minimize self-heating without degrading transistor electrical performance, including DIBL, SS, and Ion/Ioff ratio.

5. Conclusion.

The dependence of the self-heating effect on the ratio $R = T_{HfO2}/T_{SiO2}$ was modeled, taking into account the dependence of the thermal conductivity of the HfO_2 and SiO_2 layers on their thickness. The results of this modeling were compared with the results of modeling where the thermal conductivity of the mentioned layers was taken as independent of thickness and equal to the thermal conductivity of the bulk material. The comparison shows that over the entire range of R, the temperatures in both models differ by no more than 0.5 K. The simulation results show that when the HfO_2 layer thickness exceeded that of the SiO_2 layer, the channel temperature began to decrease. This temperature behavior is explained by the reduction in drain current and the dominance of Joule heat generation over heat dissipation from the channel for all T_{HfO_2}/T_{SiO_2} thickness ratios.

The dependence of short-channel effects such as the DIBL effect and SS, and the I_{on}/I_{off} ratio on the ratio $R = T_{HfO2}/T_{SiO2}$ was simulated. The simulation results show that the DIBL effect, as well as SS, increase with an increase in the ratio R. The increase in the DIBL effect is associated with an increase in the channel potential, which is explained by a decrease in the $C_{D.ox}$ gate-to-drain capacitance. The observed increase in SS is associated with a decrease in the capacitance of the sub-gate dielectric layer C_G with an increase in the ratio R. The decrease in $C_{D.ox}$ as well as C_G is explained by edge effects. The reduction of these capacitances leads to an increase in the transistor threshold voltage and, accordingly, to the observed decrease in the I_{on}/I_{off} ratio.

The observed dependencies of SHE, DIBL effect, SS, and Ion/Ioff ratio on the composition of the gate dielectric layer R show that with an increase in the ratio R in the range from 1.286 to 10.154, the channel self-heating effect is reduced by 25 K, while the DIBL effect and SS increase by 34% and 5.7%, respectively, and the switching ratio Ion/Ioff decreases by 52%.

The observed self-heating and short channel effects behavior highlights the necessity of optimizing the thickness ratio of the SiO_2 and HfO_2 gate dielectric layers during the design of SNSHFETs to minimize self-heating without degrading the electrical performance of the transistor, such as DIBL, SS, and I_{on}/I_{off} ratio.

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Conflict of Interest

The authors declare that they have no conflict of interest.

Data Availability

The data supporting the findings of this study are available from the corresponding author upon reasonable request.

Ethical Approval

This research did not involve human participants, human data, human tissue, or animals, and therefore did not require ethics committee approval.

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