Research Square

Preprints are preliminary reports that have not undergone peer review.
They should not be considered conclusive, used to inform clinical practice,
or referenced by the media as validated information.

H- SPICE Simulation of Graphene Nanoribbon Field-Effect Transistor Ternary Logic Gates: A Power-Delay Optimal Implementation of Multiple-Valued Logic Circuits

Jetya Banothu[1]

mamy.jetu@gmail.com

MANIT Bhopal

Sangeeta Nakhate[2]

MANIT Bhopal

Research Article

Keywords: Graphene Nanoribbon Field-Effect Transistor (GNRFET), Ternary Logic Gates, Multi-Valued Logic (MVL), STI, TDECODER

Posted Date: July 1st, 2026

DOI: https://doi.org/10.21203/rs.3.rs-9499643/v1

License: This work is licensed under a Creative Commons Attribution 4.0 International License.
Read Full License

Additional Declarations: No competing interests reported.

H- SPICE Simulation of Graphene Nanoribbon Field-Effect Transistor Ternary Logic Gates: A Power-Delay Optimal Implementation of Multiple-Valued Logic Circuits

Authors

Jetya Banothu[1]*, Sangeeta Nakhate[2]

Author Affiliations

[1]Department of Electronics and Communication Engineering, MANIT Bhopal, India

Email: mamy.jetu@gmail.com

[2]Department of Electronics and Communication Engineering, MANIT Bhopal, India

Email: nakhatesangeeta1@gmail.com

*Corresponding Author

Jetya Banothu

Department of Electronics and Communication Engineering,

MANIT Bhopal, India

Phone: 9640611456

Email: mamy.jetu@gmail.com

Abstract

In this paper, a novel Graphene Nanoribbon Field-Effect Transistor (GNRFET)-based ternary decoder circuit along with a conventional ternary inverter (STI) is designed and analyzed for its comprehensive performance analysis. Because of their high electrical performance, in terms of tunable bandgap and high ON/OFF current ratio, the GNRFETs are expected to achieve a greater information density and circuit complexity reduction by using MVL (Multiple-Valued Logic), to surmount the limitations of traditional binary logic. The proposed ternary decoder architecture implements only nine GNRFETs and it is optimally designed for high speed and energy efficiency. Through extensive HSPICE simulations with a 16nm GNRFET model, we perform a comparative evaluation of our GNRFET-based ternary circuits against the existing presentations based on CNTs or silicon nanotransistors (as the basis for imitation) in terms of key values: propagation delay, total power consumption and power-delay product (PDP). The results show that our proposed design of GNRFET based ternary decoder give significant 2% reduction of delay and 16% improvement of PDP when compared to state-of-the-art designs. These results show the tremendous potential of GNRFETs for implementing high performance and energy-efficient three-terminal logic circuits for future computing paradigms.

Keywords: Graphene Nanoribbon Field-Effect Transistor (GNRFET); Ternary Logic Gates; Multi-Valued Logic (MVL); STI; TDECODER.

1. Introduction

A disparity in dynamism between transmission and assembly availability for chemical bond formation is often observed in most electromechanical maneuvers [1]. In contrast to bulk graphene, the graphene nanoribbon (GNR), or its narrow derivative, shows a substantial band gap and thus it is a highly suitable material for use in nanoscale electronic devices with an enhanced ON/OFF current ratio. [2,3]. GNRs are considered among the most promising alternatives to silicon in field-effect transistor (FET) applications [1]. Extensive research has been carried out on carrier transport in GNR Field-Effect Transistors (GNRFETs) [5-7]. The mechanisms of electron pairing that underlie the macroscopic quantum effects in terms of e-ph scattering processes play a crucial role in determining graphene transistors electrical properties which otherwise tend to be weakly bound in that they are wide-area devices [1,7,8,41]. Therefore, the electron-phonon interactions are a factor that must be considered in the simulation of GNRFETs, even when at relatively low frequencies. [2,9,36].

Due to the ability of Multiple-Valued Logic (MVL) techniques to deliver increasingly faster performance as evidence density grows, they have been widely studied in recent decades. In contrast to binary logic in computing and electronics (base 2), with each logic bit having only two possible values (low (0) or high (1)) each symbol in an MVL system (base 3 or higher) can have three or more possible values. This results in higher information density, smaller logic gates, and simpler circuitry.

Carbon-based transistors such as Graphene Nanoribbon Field-Effect Transistors (GNRFETs) and Carbon Nanotube Field-Effect Transistors (CNTFETs), have become significant topics of research [27-29,31,41]. Numerous studies have focused on CNTFETs and GNRFETs, particularly in the context of multivalued logic approaches, which offer advantages over traditional binary logic strategies [9-17]. Graphene nanoribbons can be produced with widths up to 20 nm and with irregular edges [20]. In [21], a combination of lithography and etching techniques was used to create tapered graphene strips, resulting in GNRs with a width of approximately 4 nm. Also, chemical synthesis has been employed to make GNRs whose widths are below 2 nm wide [22]. The fabrication of precise 2 nm wide GNRs is also discussed in [18,19,25] shows how to make such tiny GNRs with flawless edges using the method described there.

This paper makes the following contributions:

- To analyse different electromechanical properties of Graphene Nanoribbon Field-Effect Transistors (GNRFETs).
- To design a series of simple ternary logic gates utilizing GNRFET technology.
- To compare the proposed circuits with existing design in terms of propagation delay, power consumption and power delay product (PDP).

This work extends the basic ideas that were presented in earlier works [9], offering a unified approach to the design of logic and computational circuitry based on Graphene Nanoribbon Field-Effect Transistors (GNRFETs) [38-41]. Section II presents the mathematical formulation of the three-valued logic system. Section III describes the working mechanism of GNRFET and its application of Tesla (ternary) logic and calculations. Section 4 gives

a comparative evaluation of GNRFET-based ternary logic circuits with respect to existing technologies with respect to both qualitative and quantitative performance metrics. Finally, Section 5 provides a summary of the major outcomes and indicates the overall contributions of this study.

2. GNRFET Logic Ternary System

In conventional digital electronics, there is a binary system which has two discrete system states, namely the logic high (1) and the logic low (0). The generalized multi-valued logic (MVL) from a binary truth functional with two truth values to an MVL system with R truth values where R>2 can be generalized from the two-valued MVL to an MVL system with R truth values. A particular example of MVL is the three-valued logic (Ternary Logic) where R = 3. Depending on the symmetry of the values of the logic states three valued systems might be either balanced or unbalanced, typically denoted by the sets {-1, 0, 1} and {0, 1, 2}, respectively. The present work is based on the design of unbalanced three valued logic system with supply voltage (VDD) = 0.95 V and ground potential = 0 V. The notations used for the unbalanced logic levels and its associated energy states are outlined in Table 1 [41].

General three-valued power supply device (GTI) is divided into Negative, Positive or Standard energy supply device according to the work mode. The corresponding functional relations are given by respectively Equation (1)-(3) for the Negative three-valued power device (NTI), Positive three-valued power device (PTI), and Standard three-valued power device (STI) [20] with x, y0, y1, y2 as inputs and outputs, respectively [41].

Table 1: Three-Valued Voltage Level and Logic Levels

Voltage Level (V)	Logic Symbol	Logic State
0	0	False (Low)
0.45 (½ VDD)	1	Intermediate
0.90 (VDD)	2	True (High)

Table 2: Functional Behaviour of NTI, PTI, and STI Devices

Input (X)	NTI (Y_0)	PTI (Y_1)	STI (Y_2)
State 0 (0 V)	2	2	2
State 1 (0.45 V)	0	2	1
State 2 (0.9 V)	0	0	0

Table II shows the genuine statistics which are reflecting the functions y0, y1, and y2 [41].

$$y_0 = Z_0(x) = \begin{cases} 2, & x\ when = 0 \\ 0, & x\ when \neq 0 \end{cases} \quad (1)$$

$$y_1 = Z_1(x) = \begin{cases} 0, & x\ when = 2 \\ 2, & x\ when \neq 2 \end{cases} \quad (2)$$

$$y_2 = Z_2(x) = \overline{x} = 2 - x \quad (3)$$

2.1 Significance of GNRFET

GNRs are used in this study as the multi-valued logic (MVL) architecture [20]-[26]. The structures of armchair graphene nanoribbon (AGNR) with N dimer lines are displayed in Figure 1. The number of dimer lines (N) has a very important role in picking the electronic behaviour of the GNR. Particularly, in the case when N = 3p or N = 3p + 1, where p is an integer, the ribbon demonstrates semiconductor characteristics [30]-[32]. Using Equation (5), width (W) of the GNR is determined as a function of the carbon-carbon bond length (aC-C) as: aC-C = 0.142 nm [41].

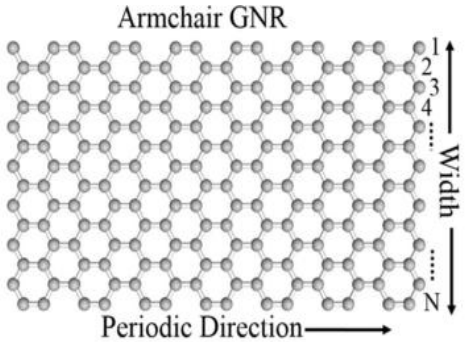


Fig. 1. Size about an Armchair GNR by means of high opinion of Dimer lines [41].

$$W_{GNR} = (N - 1)\frac{\sqrt{3}}{2} a_{c-c} \quad (4)$$

For the purpose of improving the driving capability and providing a superior contact area, several graphene nanoribbons (GNRs) are placed in parallel. The three parallel GNR strip configuration is shown in Figure 2. The source and drain regions of each strip act as the interconnection between the access terminals and the active channel and they are stabilized with a fixing factor (f_{dop} = 0.001) as reported in [33]. In Figure 2, the parameters are shown as: L_{ch} is the channel length, L_{res} is the reservoir length, W_{ch} (or WGNR) is the ribbon width, W_{gate} represents the gate width and $2W_{sp}$ is the distance between adjacent ribbons. Drain current of GNRFET can be calculated using Equation (5) given in [33].

$$(\Psi_{CH}, V_D, V_S) = \frac{2qkT}{h}\sum_{\alpha}\left[\ln\left(1 + e^{\frac{q(\Psi_{CH} - V_S) - \varepsilon_\alpha}{kT}}\right) - \ln\left(1 + e^{\frac{q(\Psi_{CH} - V_S) - \varepsilon_\alpha}{kT}}\right)\right] \quad (5)$$

Here, Ψ_{CH} represents potential within the channel, V_D and V_S are drain and source potential respectively. The variable εα represents the sub-band energy and α is the sub-band index ($1 \leq \alpha \leq N$). The constant k (or kB) is the Boltzmann constant which expresses the average heating of the particles in the gas as a function of its temperature. The second is denoted by h, and the first by T, for absolute temperature.

For any given Part code there is a point beyond which drain current (I_D) is essentially flat providing the indicator of saturation region of operation (V_{DS}) at the level. The I_D vs V_G characteristics carried out for a channel bias of 1.0 V, exhibit characteristics similar to that of a conventional MOS transistor with a well-defined threshold voltage transition. When the voltage V_{GS} at the gate is more than a threshold voltage, the N-type GNRFET switches ON and the drain current also increases proportionally to the gate voltage applied. Therefore, depending on the number of dimer linewidth (ribbon width) in the graphene nanoribbon field-effect transistor (GNRFET), by adjusting the model parameters, the targeted threshold voltage (V_{TH}) can be realized. In such a design each transistor will be according to 16 nm channel length.

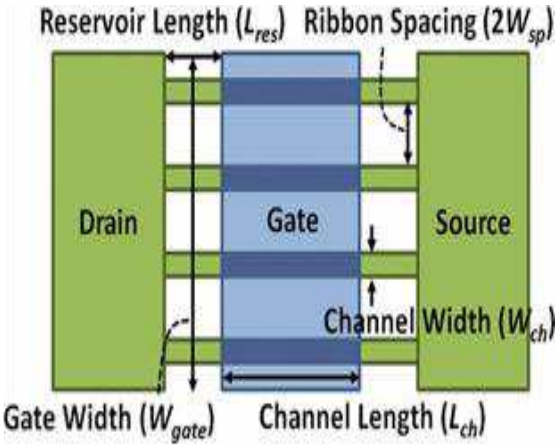


Fig. 2. Multiple (three) ribbon Armchair GNRFET [30].

2.2 Inverter

The structural layout of the Negative Three-Valued Power Device (NTI) and the Positive Three-Valued Power Device (PTI) are presented in figure 3. In the NTI configuration the p-type and n-type GNRFET are built with 7 and 9 dimer lines respectively. On the contrary, in the PTI design, the p-type GNRFETs use 9 dimer lines and the n-type GNRFETs use 7 dimer lines. The schematic of the Standard Three-Valued Power Device (STI) is as shown in Figure 4. This circuit consists of six transistors - Q1, Q2 and Q3 as n-type and Q4, Q5 and Q6 as p-type GNRFETs. The threshold voltages of the transistors Q1, Q2 and Q3 are -0.24V, 0.24V, 0.6V respectively [41].

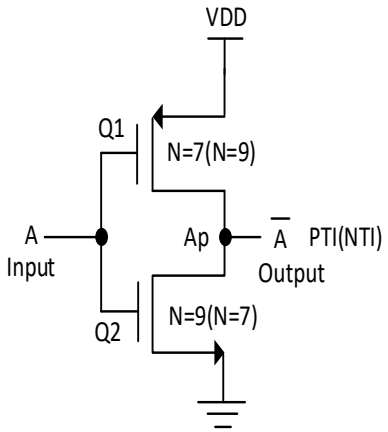


Fig. 3. Representation Illustration of Adverse (Positive) Three valued Device that produce power [41]

The transistors Q1 and Q2 are N = 9 and N = 7 dimer lines, whereas Q3 is N = 10 so that the resulting threshold voltage has the desired value. When input voltage (V in) is low (-0.3 V) and starts increasing, Q1 turns ON giving high output voltage. As V_{in} rises in the range (0.3 V to 0.6 V), Q3 is switched ON while both Q1 and Q2 are switched OFF. Finally, when V_{in} is between 0.6 V to 0.9 V and decreasing, Q2 is switching ON and thus producing a low output voltage [41].

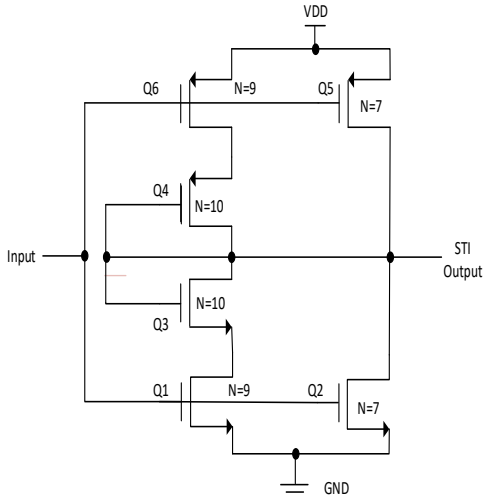


Fig. 4. Representation of Drawing of Normal Three valued Inverter using GNRFET [41]

3. Ternary Logic Design

In this subsection, the design of ternary inverters and ternary decoders are explained and the design and operation of the proposed implementation using logic gates are described.

3.1 Standard Ternary Inverter (STI)

This section demonstrates a new design of the Standard Ternary Inverter (STI), as shown in Figure 5. While the previous works have shown the validation of ternary logic gates with CNTFETs [16], in this paper, the gates are implemented and validated with GNRFETs.

Table 3: Dependence of GNRFET Behavior on Dimer Lines (N)

Dimer Lines, N	Band Gap	I_{on}/I_{off}	Order of I_{on}/I_{off}	I_{on}
8, 11, 14, 17	Small	Lowest	$\sim 10^1$	Highest
6, 9, 12, 15, 18	Moderate	High	$\sim 10^6$	High
7, 10, 13, 16	Highest	Highest	$\sim 10^6$	Low

The circuit of Figure 5 is evaluated for GNRFETs for the dimer line structures given in Table III. When A = logic 1, then transistors Q1, Q4, and Q5 turn ON and transistors Q2 and Q3 turn OFF, thus creating a logic 0 output. Conversely, when the output needs to become logic 2, Q3 is switched on, thus output will become a logic

2. For input A = logic 1, Q1 is turned ON, while Q2, Q4, and Q5 are turned OFF resulting in the corresponding output based on the ternary logic rules [41].

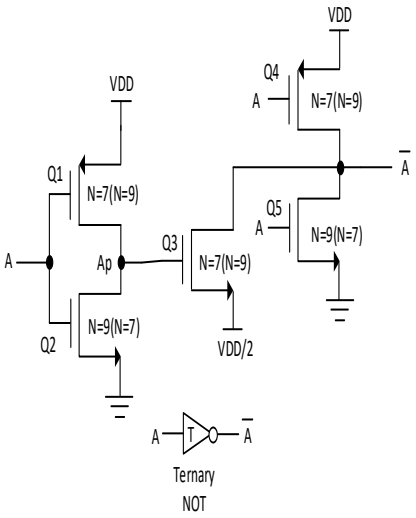


Fig. 5. The Standard Ternary Inverter circuit with GNRFET [41]

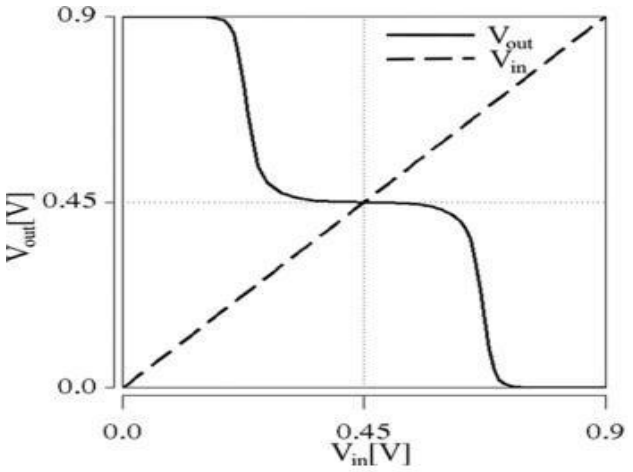


Fig. 6. Transfer curve of STI using GNTFET [41]

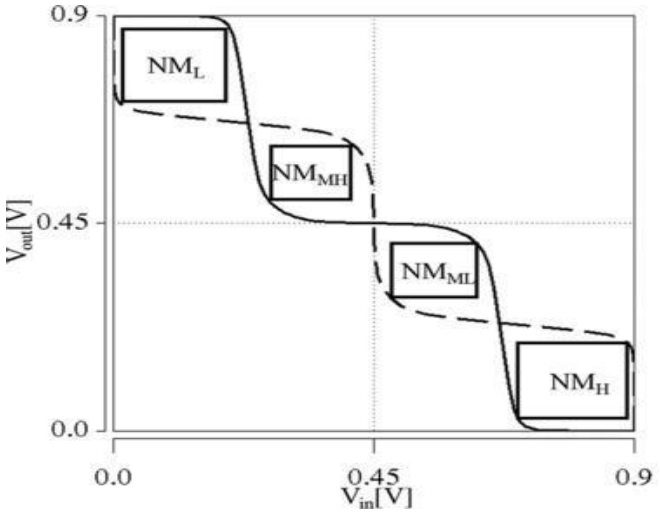


Fig. 7. Noise Margins for GNRFET-based STI are shown as butterfly curves (NM) [41]

The Standard Ternary Inverter (STI) as shown in Figure 5 is implemented in GNRFETs with configurations of dimers as listed in Table III. In the case for an input A = logic 1, transistors Q1, Q4, and Q5 are ON and Q2 and Q3 are OFF resulting in a logic 0 output. When the output A_p is to be a logic 2, then Q3 is turned on so that the output is a logic 1. For A = logic 2, transistors Q2 and Q5 turn ON and Q1 and Q4 stay OFF, Q3 is turned OFF when A"" = logic 0 which results in a logic 0 output. The voltage transfer characteristics (VTC) of the STI, as displayed in Figure 6, show that the device can retain three different levels of output voltage over a wide range of input voltage. The four noise margins are defined as Noise Margin Low (NML) Noise Margin Low-to-Medium (NM_{ML}) Noise Margin Medium-to-High (NM_{MH}) Noise Margin High (NMH), which are shown in Figure 7 and the output waveform is shown in Figure 8 [41].

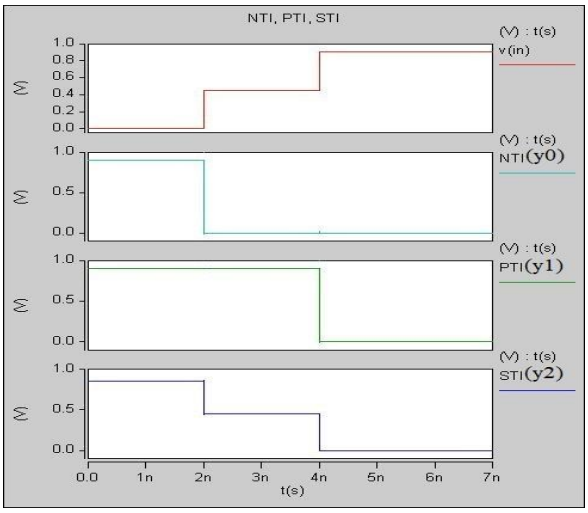


Fig. 8. The output waveforms of STI

3.2 Proposed Ternary Decoder

This subsection contains a suggested combinational circuit in the form of a Ternary (T) Decoder. As shown in figure 9, the design has a novel architecture that consists of nine transistors. The decoder has one ternary input (X) and three binary inputs (X0, X1, and X2). Its output mathematical expression is given in Equation (6) and it is summarized in Table 4.

$$X_k = \begin{cases} 2 & x = k \\ 0 & x \neq k \end{cases} \qquad (6)$$

Table 4: Dimer Lines and Threshold Energy of The GNRFETs Used in the Proposed T Decoder

GNRFET Type	Dimer Line (N)	V_{th} (V)
P-GNRFET (Q1, Q5)	7	-0.559
P-GNRFET (Q3, Q8)	12	-0.289
N-GNRFET (Q4, Q6, Q9)	7	0.559
N-GNRFET (Q2, Q7)	12	0.289

Source:[41]

The circuit consists of one Negative Ternary Inverter (NTI), one Positive Ternary Inverter, NTI (PTI), binary inverter and another sub-circuit. Table 4 shows the dimer line numbers and threshold voltage (Vth) of the GNRFETs adopted and the operating characteristics of the proposed design are described in Table 5.

For input X=logic 0, transistor Q1 and Q3 are ON but Q2, Q4 and Q7 are OFF. As a result, the intermediate signal Y, output X0 are set to logic 2, and Q6, Q9 are ON and Q5, Q8 are OFF and therefore, the outputs X1, X2 are set to logic 0. When X = logic 1, Q2, Q3 and Q7 cross ON and Q1 and Q4 are turned OFF. This causes the value of intermediate signal Y to be set to logic 2, and the value of the output to be set to logic 0 to X0. Also, Q6 and Q8 are ON and Q5 and Q9 are OFF with the result that X1 = logic 2 and X2 = logic 0. For X = logic 2, the following logic are activated: Q2, Q4 and Q7 and the logic Q1 and Q3 are OFF. In this condition, outputs X0 and Y will be logic 0, Q5 and Q8 will be ON, Q6 and Q9 will be OFF thus X1 will be logic 0 and X2 will be logic 2. The simulated output waveform of the Ternary Decoder is shown in Figure 10 validates the proper working of the proposed design for all the input levels.

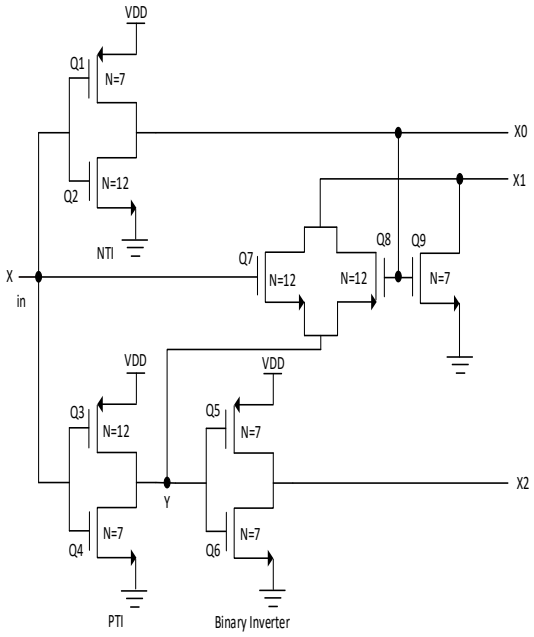


Fig. 9. The proposed transistor Level of T Decoder with 9 GNRFETs.

Table 5: The proposed t decoder detailed operation of fig. 9.

Ternary Input X	**0 (0 V)**	**1 (0.45 V)**	**2 (0.9 V)**
P-GNRFET Q1	ON	OFF	OFF
N-GNRFET Q2	OFF	ON	ON
OUTPUT X0	**2**	**0**	**0**
P-GNRFET Q3	ON	ON	OFF
N-GNRFET Q4	OFF	OFF	ON
INTERMEDIATE Y	**2**	**2**	**0**
P-GNRFET Q7	OFF	ON	ON
P-GNRFET Q8	OFF	ON	ON
N-GNRFET Q9	ON	OFF	OFF
OUTPUT X1	**0**	**2**	**0**
P-GNRFET Q5	OFF	OFF	ON

N-GNRFET Q6	ON	ON	OFF
OUTPUT X2	**0**	**0**	**2**

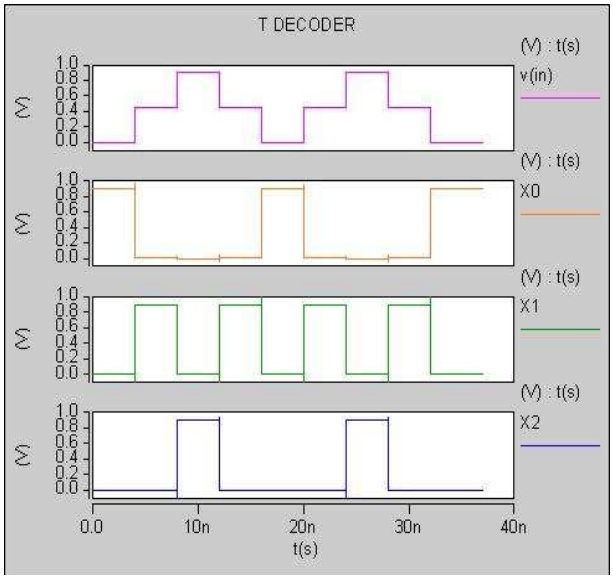


Fig.10. The proposed transient analysis of T Decoder

4. Comparison

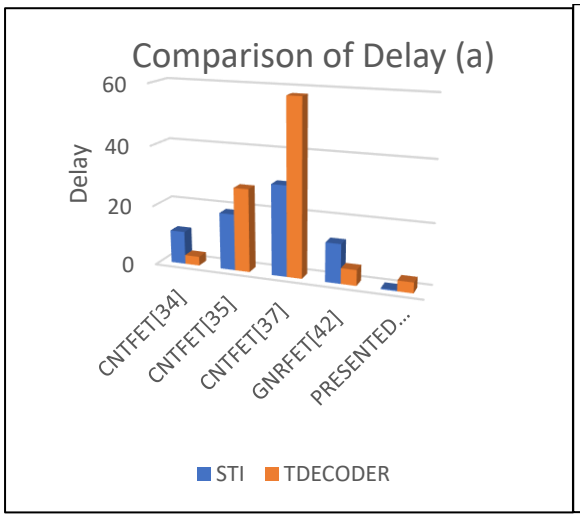
Various implementations of ternary logic gate using CNTFETs have been reported in the literature. However, graphene nanoribbons (GNRs) are a promising alternative for use in logic networks based on transistors. This section presents a comparison between selected ternary logic circuits implemented using CNTFETs, GNRFETs, and a comparison with the results obtained using the proposed GNRFET-based circuits and the results obtained using a model (circuits) that exist in the literature. All the simulations were with an input slew rate of 50 ps, an output load of 1 pF, and the doping fraction (f_{dop}) of 0.001 applied uniformly to all transistors. The model for simulation using CNTs (CNTFET model) was taken from [37], while the 16 nm CNTFET devices given in [34] were used as reference devices.

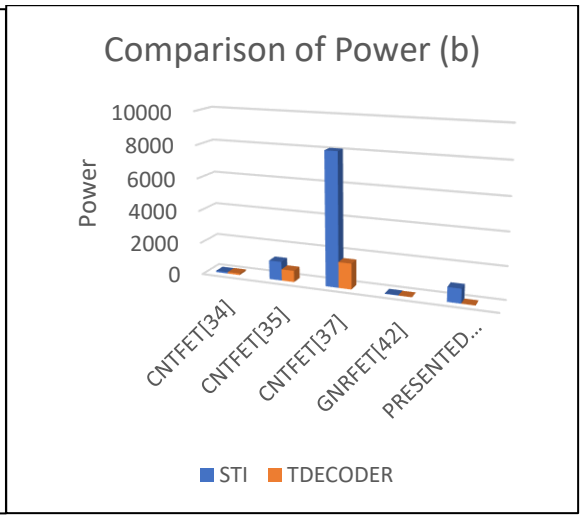
Figures 11(a) - 11(c) show comparative results for delay, power and Power-Delay Product (PDP) for the Standard Ternary Inverter (STI) and the Ternary Decoder (TDECODER). Table 6 summarises the performance comparison between the CNTFET and GNRFET implementations in terms of delay, total power and PDP. The proposed GNRFET-based logic gates show significant improvements in the ternary logic performance such as delay reduction, power consumption reduction and PDP improvements.

Specifically, the STI and TDECODER circuits are faster than previously reported designs [34,35, 37,42] and the number of transistors is greatly reduced. These results show that the proposed GNRFET-based ternary inverter and decoder provide meaningful advantages in Power-Delay Product and overall circuit efficiency of the circuit compared to conventional approaches.

Table 6: Comparative Analysis between the Proposed GNRFET-based Ternary Logic Gates and Existing CNTFET

	Logic Gates	Transistor count	Delay (ps)	Total Power (nW)	Power Delay Product (PDP) e-18
STI	CNTFET [34]	6	11	88.6	0.98
	CNTFET [35]	6	18.8	1170	33.2
	CNTFET [37]	6	30	8100	24
	GNRFET [42]	6	13	23.22	0.302
	Presented Work	5	0.38	880	0.33
TDECODER	CNTFET [34]	10	3	100.8	0.3
	CNTFET [35]	-	27.6	704.8	19.46
	CNTFET [37]	10	58	1580	92
	GNRFET [42]	11	14	6.09	0.09
	Presented Work	9	3.5	8.83	0.03





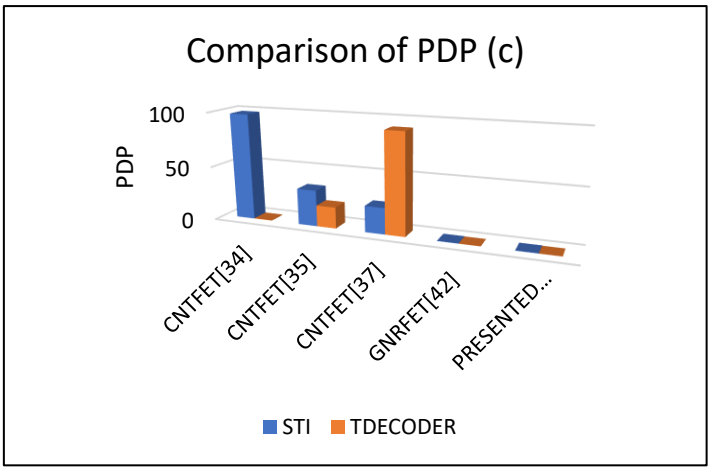


Fig. 11. The comparative transient analysis of STI, and TDEODER for (a) Delay, (b) Power, and (c) PDP

5. Conclusion

This paper confirmed the functionality of the Standard Ternary Inverter (STI) and recently introduced Ternary Decoder, which is executed using GNRFETs, with a focused on the improvement of the work and energy efficiency. They were simulated using the HSPICE model with a 16 nm feature size, 0.9 V supply voltage and 0.45 V intermediate voltage. The evaluation assessed the power consumption and latency values of ternary circuit designs using GNRFETs, and compared to the traditional design. The findings show that GNRFET-based circuits can provide better power efficiency and lower delay, which makes the use of ternary logic on a gate and a circuit-level beneficial. Such circuits can be considered especially applicable in low-power systems, such as portable devices and embedded systems, where energy conservation is an important factor.

Credit Authorship Contribution Statement

Jetya Banothu: Conceptualization, Methodology, Software, Validation, Formal analysis, Investigation, Writing – original draft, Writing – review & editing, Visualization.

Sangeeta Nakhate: Conceptualization, Methodology, Writing – original draft, Writing – review & editing, Supervision.

Declaration of Competing Interest: The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data Availability: No data was used for the research described in the article

Funding Source: No

Conflict of Interest – No

Reference

[1] W. Zhang, C. Basaran, and T. Ragab, “Impact of geometry on transport properties of armchair graphene nanoribbon heterojunction,” Carbon N. Y., vol. 124, pp. 422–428, Nov. 2017, doi: 10.1016/j.carbon.2017.09.005.

[2] S. S. Ghoreishi, R. Yousefi, K. Saghafi, and H. Aderang, “A numerical study of the nanoribbon field-effect transistors under the ballistic and dissipative transport,” Int. Nano Lett., vol. 7, no. 3, pp. 225–232, Sep. 2017, doi: 10.1007/s40089-017-0219-x.

[3] IEEE Staff and IEEE Staff, Graphene Nanoribbon Field-effect Transistors-2008.pdf. 2008.

[4] M. S. Fahad, A. Srivastava, A. K. Sharma, and C. Mayberry, “Analytical current transport modeling of graphene nanoribbon tunnel field-effect transistors for digital circuit design,” IEEE Trans. Nanotechnol., vol. 15, no. 1, pp. 39–50, Jan. 2016, doi: 10.1109/TNANO.2015.2496158.

[5] S. S. Ghoreishi, K. Saghafi, R. Yousefi, and M. K. Moravvej-Farshi, “Graphene nanoribbon tunnel field effect transistor with lightly doped drain: Numerical simulations,” Superlattices Microstruct., vol. 75, pp. 245–256, 2014, doi: 10.1016/j.spmi.2014.07.042.

[6] A. Naderi, “Theoretical analysis of a novel dual gate metal-graphene nanoribbon field effect transistor,” Mater. Sci. Semicond. Process., vol. 31, pp. 223–228, 2015, doi: 10.1016/j.mssp.2014.11.051.

[7] S. S. Ghoreishi, K. Saghafi, and M. K. Moravvej-Farshi, “A novel graphene nano-ribbon field effect transistor with Schottky tunneling drain and ohmic tunneling source,” Mod. Phys. Lett. B, vol. 27, no. 26, Oct. 2013, doi: 10.1142/S0217984913501893.

[8] Y. Ouyang, Y. Yoon, and J. Guo, “Scaling behaviors of graphene nanoribbon FETs: A three-dimensional quantum simulation study,” IEEE Trans. Electron Devices, vol. 54, no. 9, pp. 2223–2231, Sep. 2007, doi: 10.1109/TED.2007.902692.

[9] K. C. Smith, “The Prospects for Multivalued Logic: A Technology and Applications View,” 1981. doi: 10.1109/TC.1981.1675860.

[10] IEEE Nanotechnology Council and Institute of Electrical and Electronics Engineers, Enabling Energy-Efficient Ternary Logic Gates using CNFETs Sepehr. 2017.

[11] A. Heung and H. T. Mouftah, “Depletion/Enhancement CMOS For a Low Power Family of Three-Valued Logic Circuits,” IEEE J. Solid-State Circuits, vol. 20, no. 2, pp. 609–616, 1985, doi: 10.1109/JSSC.1985.1052354.

[12] P. C. Balla and A. Antoniou, “Low Power Dissipation MOS Ternary Logic Family,” IEEE J. Solid-State Circuits, vol. 19, no. 5, pp. 739–749, 1984, doi: 10.1109/JSSC.1984.1052216.

[13] A. Raychowdhury and K. Roy, “Carbon-nanotube-based voltage-mode multiple-valued logic design,” IEEE Trans. Nanotechnol., vol. 4, no. 2, pp. 168–179, Mar. 2005, doi: 10.1109/TNANO.2004.842068.

[14] S. Karmakar, J. A. Chandy, and F. C. Jain, “Design of ternary logic combinational circuits based on quantum dot gate FETs,” IEEE Trans. Very Large Scale Integr. Syst., vol. 21, no. 5, pp. 793–806, 2013, doi: 10.1109/TVLSI.2012.2198248.

[15] G. K. Johnsen, “An introduction to the memristor - A valuable circuit element in bioelectricity and bioimpedance,” J. Electr. Bioimpedance, vol. 3, no. 1, pp. 20–28, 2012, doi: 10.5617/jeb.305.

[16] R. A. Jaber, A. Kassem, A. M. El-Hajj, L. A. El-Nimri, and A. M. Haidar, “High-Performance and Energy-Efficient CNFET-Based Designs for Ternary Logic Circuits,” IEEE Access, vol. 7, pp. 93871–93886, 2019, doi: 10.1109/ACCESS.2019.2928251.

[17] R. A. Jaber, A. M. El-Hajj, A. Kassem, L. A. Nimri, and A. M. Haidar, “CNFET-based designs of Ternary Half-Adder using a novel ‘decoder-less’ ternary multiplexer based on unary operators,” Microelectronics J., vol. 96, Feb. 2020, doi: 10.1016/j.mejo.2019.104698.

[18] V. P. Y. Shital Joshi, Saraju P. Mohanty, Elias Kougianos, Proceedings - 2017 IEEE International Symposium on Nanoelectronic and Information Systems, iNIS 2017, vol. 2018-Febru. IEEE, 2018.

[19] Y. Yoon, G. Fiori, S. Hong, G. Iannaccone, and J. Guo, “Performance comparison of graphene nanoribbon FETs with Schottky contacts and doped reservoirs,” IEEE Trans. Electron Devices, vol. 55, no. 9, pp. 2314–2323, 2008, doi: 10.1109/TED.2008.928021.

[20] Z. Chen, Y. M. Lin, M. J. Rooks, and P. Avouris, “Graphene nano-ribbon electronics,” Phys. E Low-Dimensional Syst. Nanostructures, vol. 40, no. 2, pp. 228–232, Dec. 2007, doi: 10.1016/j.physe.2007.06.020.

[21] X. Wang and H. Dai, “Etching and narrowing of graphene from the edges,” Nat. Chem., vol. 2, no. 8, pp. 661–665, Aug. 2010, doi: 10.1038/nchem.719.

[22] X. Li, X. Wang, L. Zhang, S. Lee, and H. Dai, “Chemically derived, ultrasmooth graphene nanoribbon semiconductors,” Science (80-.)., vol. 319, no. 5867, pp. 1229–1232, Feb. 2008, doi: 10.1126/science.1150878.

[23] J. Cai et al., “Atomically precise bottom-up fabrication of graphene nanoribbons,” Nature, vol. 466, no. 7305, pp. 470–473, Jul. 2010, doi: 10.1038/nature09211.
[24] X. Wang, Y. Ouyang, X. Li, H. Wang, J. Guo, and H. Dai, “Room-temperature all-semiconducting sub-10-nm graphene nanoribbon field-effect transistors,” Phys. Rev. Lett., vol. 100, no. 20, May 2008, doi: 10.1103/PhysRevLett.100.206803.
[25] L. Jiao, L. Zhang, L. Ding, J. Liu, and H. Dai, “Aligned graphene nanoribbons and crossbars from unzipped carbon nanotubes,” Nano Res., vol. 3, no. 6, pp. 387–394, 2010, doi: 10.1007/s12274-010-1043-z.
[26] Z. T. Sandhie, F. Uddin Ahmed, and M. Chowdhury, “GNRFET based Ternary Logic - Prospects and Potential Implementation,” Feb. 2020. doi: 10.1109/LASCAS45839.2020.9069028.
[27] A. Dhande and V. Ingole, “Design And Implementation Of 2 Bit Ternary ALU Slice,” 2005.
[28] E. P. D. Chen, S. Chilstedt, C. Dong, “What Everyone Needs to Know about Carbon-Based Nanocircuits,” 2010. [Online]. Available: www.dac.com
[29] M. Y. Han, B. Özyilmaz, Y. Zhang, and P. Kim, “Energy band-gap engineering of graphene nanoribbons,” Phys. Rev. Lett., vol. 98, no. 20, May 2007, doi: 10.1103/PhysRevLett.98.206805.
[30] Y. Y. Chen et al., “A SPICE-Compatible Model of MOS-Type Graphene Nano-Ribbon Field-Effect Transistors Enabling Gate- and Circuit-Level Delay and Power Analysis under Process Variation,” IEEE Trans. Nanotechnol., vol. 14, no. 6, pp. 1068–1082, Nov. 2015, doi: 10.1109/TNANO.2015.2469647.
[31] M. T. Ahmadi, Z. Johari, D. C. Y. Chek, N. A. Amin, and R. Ismail, “Modelling of graphene nanoribbon Fermi energy,” J. Nanomater., vol. 2010, 2010, doi: 10.1155/2010/909347.
[32] Y. W. Son, M. L. Cohen, and S. G. Louie, “Energy gaps in graphene nanoribbons,” Phys. Rev. Lett., vol. 97, no. 21, 2006, doi: 10.1103/PhysRevLett.97.216803.
[33] Y. Chen, “Graphene Nano-Ribbon And Transition Metal Dichalcogenide Field-Effect Transistor Modeling And Circuit Simulation,” 2015.
[34] S. Lin, Y. Bin Kim, and F. Lombardi, “CNTFET-based design of ternary logic gates and arithmetic circuits,” IEEE Trans. Nanotechnol., vol. 10, no. 2, pp. 217–225, Mar. 2011, doi: 10.1109/TNANO.2009.2036845.
[35] S. Tabrizchi, F. Sharifi, A.- H. Badawy, and Z. M. Saifullah, “Enabling energy-efficient ternary logic gates using CNFETs,” in Proc. IEEE 17th Int. Conf. Nanotechnol., 2017, pp. 542–547.
[36] B. Shukla et al., Proceedings - 2014 3rd International Conference on Reliability, Infocom Technologies and Optimization: Trends and Future Directions, ICRITO 2014. 2015.
[37] P. A. Gowrisankar, “Design of multi-valued ternary logic gates based on emerging sub-32nm technology,” in Proc. 3rd Int. Conf. Sci. Technol. Eng. Manage., 2017, pp. 1023–1031.
[38] D. G. Anil, Y. Bai, and Y. Choi, “Performance evaluation of ternary computation in SRAM design using graphene nanoribbon field effect transistors,” in 2018 IEEE 8th Annual Computing and Communication Workshop and Conference, CCWC 2018, Feb. 2018, vol. 2018-Janua, pp. 382–388. doi: 10.1109/CCWC.2018.8301723. R. Faghih Mirzaee, K. Navi, and N. Bagherzadeh, “High-efficient circuits for ternary addition,” VLSI Des., vol. 2014, 2014, doi: 10.1155/2014/534587.
[40] S. P. P. and M. B. S. Chetan Vudadha, Proceedings - 2017 IEEE International Symposium on Nanoelectronic and Information Systems, iNIS 2017, vol. 2018-Febru. IEEE, 2018.
[41]M. H. Moaiyeri, A. Doostaregan, and K. Navi, “Design of energy-efficient and robust ternary circuits for nanotechnology,” IET Circuits, Devices Syst., vol. 5, no. 4, pp. 285–296, Jul. 2011, doi: 10.1049/iet-cds.2010.03

[40] Z. Tasnim, S. Student, F. Uddin, and A. Student, “Design of Ternary Logic and Arithmetic Circuits Using GNRFET,” no. July, 2020, doi: 10.1109/OJNANO.2020.3020567.
[41] Banothu J, Nakhate S. Design of high-speed GNRFET-based analog to digital converter. Library Progress International. 2024;44(3):23336–50.