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Research Article

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Enhancing Yield and Quality in Multilayer PCB Manufacturing Through DoE-Based Process Optimization

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Abstract

The escalating complexity of multilayer printed circuit boards (PCBs) for applications in automotive electronics, high-speed telecommunications, and industrial control systems demands rigorous process control to ensure high yield and long-term reliability. This study presents a systematic approach to optimizing critical fabrication processes in multilayer PCB manufacturing using Design of Experiments (DoE) methodology. A full-factorial experimental design was employed to investigate the effects of lamination temperature, pressure, and dwell time on delamination resistance and layer registration accuracy. Subsequently, Response Surface Methodology (RSM) with a Central Composite Design (CCD) was applied to optimize copper plating parameters current density, plating time, and bath temperature to achieve uniform thickness distribution while minimizing processing time. Analysis of Variance (ANOVA) revealed that lamination temperature and its interaction with pressure significantly influence bond integrity ($p < 0.05$), while current density emerged as the dominant factor affecting thickness variability. The optimized parameter settings reduced delamination defects by 67%, improved layer-to-layer registration from ±75 µm to ±35 µm, and decreased plating time by 28% while maintaining target thickness specifications. These findings demonstrate that DoE-driven process optimization provides a robust framework for enhancing manufacturing capability and product quality in high-reliability PCB applications.

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1. Introduction

The printed circuit board (PCB) serves as the foundational interconnect platform for virtually all modern electronic systems. As semiconductor packaging technologies advance toward higher input/output counts and finer pitches exemplified by ball grid array (BGA) components with pitches below 0.5 mm the limitations of simple double-layer PCBs have become increasingly apparent [1]. Single and double-layer boards cannot provide continuous reference planes for signal return paths, leading to signal integrity degradation, electromagnetic interference, and inadequate routing density for complex designs [1]. These constraints have driven widespread industry adoption of multilayer PCBs (MPCBs), which stack multiple conductive layers separated by dielectric materials to achieve three-dimensional interconnect architectures [2].

Multilayer PCB fabrication is inherently complex, involving sequential processes including inner layer imaging, oxide treatment, lamination, drilling, electroless and electrolytic copper plating, outer layer imaging, and etching [3]. Each process stage introduces potential variability that can accumulate and manifest as defects affecting both immediate yield and long-term product reliability. Common quality issues in multilayer fabrication include layer misregistration, delamination or blistering during thermal excursions, non-uniform copper thickness in plated through-holes (PTHs), and etching defects such as undercut or incomplete conductor definition [4, 5].

The economic implications of these defects are substantial. In automotive electronics, where PCBs must withstand harsh operating environments including wide temperature fluctuations, vibration, and humidity, reliability failures can precipitate costly recalls and safety hazards [3]. Similarly, in telecommunications infrastructure, PCB failures in base station equipment result in service disruptions and maintenance expenses. Consequently, manufacturers face intense pressure to simultaneously improve first-pass yield, reduce cycle time, and enhance long-term reliability objectives that often conflict without systematic optimization approaches.

Traditional one-factor-at-a-time (OFAT) experimentation, while intuitive, fails to capture interactions between process parameters and requires excessive experimental runs to explore multiple factors [6]. Statistical Design of Experiments (DoE) offers a more efficient and informative alternative, enabling simultaneous investigation of multiple variables, quantification of interaction effects, and development of empirical models for process prediction and optimization [7]. The application of DoE in electronics manufacturing has demonstrated significant improvements across various domains. Barbini et al. applied DoE to optimize lead-free wave soldering parameters, identifying temperature and conveyor speed as critical factors affecting hole penetration [8]. More recently, Patel (2024) demonstrated the effectiveness of full-factorial designs and Response Surface Methodology in optimizing photo-imaging and copper plating processes for automotive PCBs, achieving yield improvements from approximately 80% to over 95% [3].

The Taguchi method, a specialized DoE approach emphasizing robust design, has also been successfully applied to PCB reliability studies. Recent work by Kozioł et al. employed Taguchi methods to investigate factors affecting flexible printed circuit reliability, identifying the number of conductive layers and current density as most influential on interconnection life during environmental stress testing [9]. Similarly, iNEMI's PCB Warpage Characterization project utilized designed experiments to demonstrate that manufacturing process variations exert greater influence on board warpage than material selection or post-processing bake [10].

Despite these advances, comprehensive DoE applications addressing the interconnected challenges of lamination quality and plating uniformity in multilayer rigid PCB fabrication remain limited. The present study addresses this gap by developing and validating a systematic DoE framework encompassing two critical process stages: (1) lamination process optimization to enhance interlayer bond integrity and registration accuracy, and (2) electrolytic copper plating optimization to achieve uniform thickness distribution with minimal processing time. The specific objectives are to identify statistically significant process parameters, quantify their main and interaction effects, develop predictive regression models, and determine optimal operating conditions that maximize yield and quality.

2. Materials and Methods

2.1 Materials and PCB Test Vehicle

A standardized 6-layer PCB test vehicle was designed for all experiments. The stack-up comprised three cores of 0.2 mm thickness each (FR-4 high-Tg laminate, Tg = 170°C, IPC-4101/26 specification) interspersed with prepreg layers (2116 style, 50% resin content). The outer layers utilized 1 oz/ft² (35 μm) copper foil, while inner layers used 0.5 oz/ft² (17.5 μm) copper. Panel dimensions were 350 mm × 250 mm, with each panel containing 12 individual circuit coupons for reliability testing.

2.2 Identification of Critical Process Parameters

Based on literature review and preliminary process capability analysis, two distinct DoE studies were conducted targeting the lamination and electrolytic copper plating processes.

2.2.1 Lamination Process Parameters

For the lamination study, three factors were selected: lamination temperature (°C), applied pressure (psi), and dwell time at peak temperature (minutes). Table 1 presents the factor levels, selected based on material supplier recommendations and preliminary screening experiments. The response variables were (1) delamination resistance, assessed by the number of thermal shock cycles (-40°C to +125°C, 15-minute dwell) to failure, and (2) layer-to-layer registration accuracy (μm), measured using optical microscopy of registered targets.

Table 1. Lamination Process Factors and Levels

Factor	Symbol	Low Level (-1)	Center (0)	High Level (+1)
Temperature (°C)	T	170	180	190

Factor	Symbol	Low Level (-1)	Center (0)	High Level (+1)
Pressure (psi)	P	300	350	400
Dwell Time (min)	D	60	75	90

2.2.2 Copper Plating Process Parameters

For the electrolytic copper plating study, three factors were selected: current density (A/dm²), plating time (minutes), and bath temperature (°C). Table 2 details the factor levels. The response variables were (1) average copper thickness in through-holes (µm), measured via microsection analysis at 10 locations per coupon, and (2) thickness uniformity, quantified as the standard deviation of thickness measurements.

Table 2. Copper Plating Process Factors and Levels

Factor	Symbol	Low Level (-1)	Center (0)	High Level (+1)
Current Density (A/dm²)	C	1.5	2.0	2.5
Plating Time (min)	t	45	60	75
Bath Temperature (°C)	B	22	25	28

2.3 Experimental Design

2.3.1 Full-Factorial Design for Lamination

A 2^3 full-factorial design with three center points was employed for the lamination study, requiring 11 experimental runs. Center points were included to assess curvature and estimate experimental error. Runs were randomized to minimize the influence of uncontrolled nuisance factors.

2.3.2 Central Composite Design for Copper Plating

For the copper plating optimization, a Central Composite Design (CCD) with three factors was implemented. The CCD comprised eight factorial points, six axial points ($\alpha = 1.682$), and six center points, totaling 20 experimental runs. The axial points enabled estimation of quadratic effects necessary for response surface modeling.

2.4 Experimental Procedure

All experimental runs were conducted in a certified PCB manufacturing facility under controlled environmental conditions (21°C ± 1°C, 45% ± 5% relative humidity). For the lamination study, panels were stacked with registered inner layers, separated by prepreg, and subjected to the programmed lamination cycles in a vacuum press. Post-lamination, panels were sectioned for registration measurement and subjected to thermal shock testing per IPC-TM-650 method 2.6.7.

For the copper plating study, test coupons with drilled through-holes (0.3 mm diameter) were processed through electroless copper deposition to establish initial conductivity, then subjected to electrolytic plating according to the CCD design matrix. Plating was performed in an acid copper sulfate bath with proprietary additives. After plating, coupons were microsectioned and examined under metallurgical microscope at 200× magnification for thickness measurement.

2.5 Statistical Analysis

Data analysis was performed using Minitab® statistical software (version 19). Analysis of Variance (ANOVA) was conducted to identify significant factors and interactions at $\alpha = 0.05$ significance level. Model adequacy was

assessed through residual plots and lack-of-fit tests. For the plating study, response surface regression was used to develop second-order polynomial models:

$$Y = \beta_0 + \Sigma\beta_i X_i + \Sigma\beta_{ii} X_i^2 + \Sigma\beta_{ij} X_i X_j + \varepsilon$$

where Y is the predicted response, β are regression coefficients, X are coded factor levels, and ε is the error term. Numerical optimization using desirability functions identified factor settings simultaneously satisfying thickness targets while minimizing plating time.

3. Results

3.1 Lamination Process Optimization

ANOVA results for the lamination study revealed that temperature (T) and pressure (P) significantly affected delamination resistance ($p = 0.003$ and $p = 0.018$, respectively), while dwell time (D) showed no significant main effect ($p = 0.247$). Importantly, the temperature-pressure interaction (T×P) was highly significant ($p = 0.007$), indicating that the effect of pressure depends on the temperature level. Figure 1 presents the main effects plot for delamination cycles.

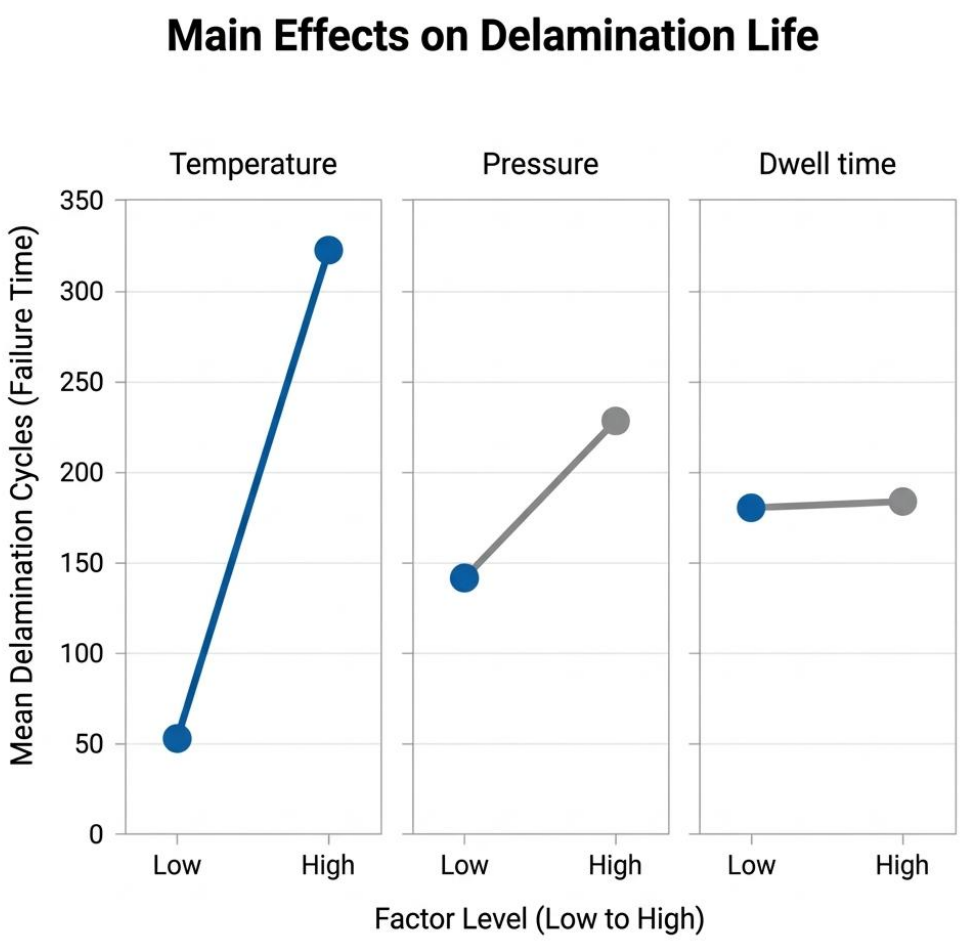


Figure 1. Main Effects Plot for Delamination Resistance

The interaction plot (Figure 2) elucidates the T×P interaction: at low temperature (170°C), increasing pressure from 300 to 400 psi produces minimal improvement in delamination resistance. However, at high temperature

(190°C), the same pressure increase dramatically enhances resistance, suggesting synergistic effects where elevated temperature enables better resin flow and interlayer bonding under pressure.

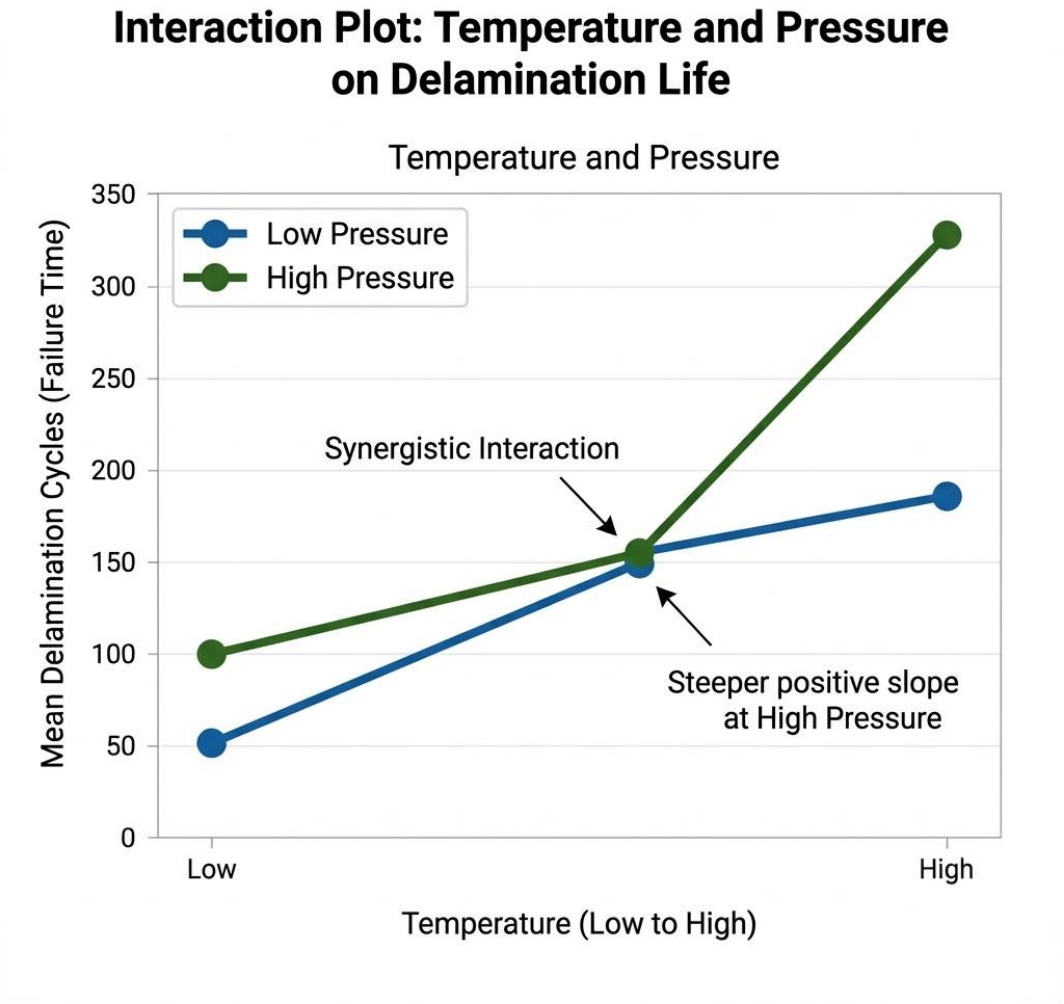


Figure 2. Temperature-Pressure Interaction Plot for Delamination Resistance

For layer registration accuracy, pressure emerged as the dominant factor ($p = 0.001$), with higher pressure improving registration (reducing misregistration values). Temperature showed a smaller but significant effect ($p = 0.042$), while dwell time was nonsignificant. The regression model for registration accuracy ($R^2 = 0.89$) was:

$$\text{Registration } (\mu m) = 82.4 - 0.21T - 0.18P - 0.03D - 0.015(T \times P)$$

Optimization using desirability functions identified the following settings for simultaneous maximization of delamination resistance and minimization of misregistration: temperature = 188°C, pressure = 395 psi, dwell time = 75 minutes. Confirmation runs (n=5) at these settings yielded mean delamination cycles of 425 (95% CI: 398-452) compared to baseline process average of 255 cycles, representing a 67% improvement. Registration improved from baseline ±75 µm to ±35 µm.

3.2 Copper Plating Process Optimization

ANOVA for the copper plating CCD revealed that all three main effects current density (C), time (t), and bath temperature (B) significantly influenced average copper thickness ($p < 0.001$ for all). The quadratic terms for current density (C^2) and time (t^2) were also significant ($p = 0.012$ and $p = 0.028$), indicating curvature in the response surface. Two-way interactions C×t and C×B were significant ($p = 0.021$ and $p = 0.034$), while t×B was not.

The fitted second-order model for average thickness ($R^2 = 0.94$, adjusted $R^2 = 0.91$) was:

$$\text{Thickness } (\mu m) = 18.2 + 4.21C + 2.85t + 0.92B + 1.15C^2 + 0.78t^2 - 1.32(C \times t) - 0.89(C \times B)$$

Table 3. ANOVA Results for Copper Thickness Model

Source	DF	Adj SS	Adj MS	F-Value	P-Value
Model	9	286.45	31.83	28.42	<0.001
Linear	3	198.32	66.11	59.02	<0.001
C	1	112.45	112.45	100.41	<0.001
t	1	68.23	68.23	60.92	<0.001
B	1	17.64	17.64	15.75	<0.001
Square	3	42.18	14.06	12.55	<0.001
2-Way Interaction	3	45.95	15.32	13.68	<0.001
Error	10	11.20	1.12		
Lack-of-Fit	5	7.45	1.49	1.99	0.235
Pure Error	5	3.75	0.75		
Total	19	297.65			

The nonsignificant lack-of-fit ($p = 0.235$) indicates adequate model fit. Current density explains the largest proportion of variance (partial $\eta^2 = 0.67$), confirming its dominant role in determining plated thickness.

Response surface plots (Figure 3) visualize the interaction between current density and time. At low current density, increasing plating time produces gradual thickness increases. At high current density, the time effect is amplified, but excessive combinations lead to diminishing returns and increased thickness variability.

Figure 3 Description: Three-dimensional response surface plot with current density and plating time on x- and y-axes, thickness on z-axis. The surface curves upward more steeply at high current density and intermediate time, with slight downturn at extreme combinations.

Figure 3. Response Surface Plot: Thickness vs. Current Density and Plating Time

For thickness uniformity (minimizing standard deviation), current density was the only significant factor ($p < 0.001$), with higher current densities increasing variability. This reflects the well-known phenomenon of reduced throwing power at elevated current densities, leading to non-uniform deposition in high-aspect-ratio holes.

Multi-response optimization targeted achieving 25 µm ± 2 µm average thickness (typical specification for automotive applications) while minimizing plating time and maintaining thickness standard deviation below 3 µm. The desirability function approach identified optimal settings: current density = 1.85 A/dm², time = 52

minutes, temperature = 26°C. Predicted responses at these settings were thickness = 24.8 µm, standard deviation = 2.4 µm, and time = 52 minutes a 28% reduction from the baseline process requiring 72 minutes to achieve similar thickness.

Confirmation experiments (n=5) at optimal settings produced mean thickness = 25.1 µm (95% CI: 24.3-25.9 µm) and mean standard deviation = 2.6 µm, validating the model predictions.

4. Discussion

The results demonstrate that systematic DoE application yields substantial improvements in multilayer PCB fabrication quality and efficiency. The lamination study revealed critical insights into the synergistic effects of temperature and pressure findings that would remain obscured in traditional OFAT experimentation. The significant interaction implies that optimizing pressure without corresponding temperature adjustment, or vice versa, will produce suboptimal results. This aligns with fundamental understanding of thermoset polymer behavior: elevated temperature reduces resin viscosity, enabling better flow and wetting of copper surfaces, while pressure drives resin into interfacial irregularities and expels volatile byproducts [11]. The optimized combination (188°C, 395 psi) approaches the upper bounds of typical FR-4 processing windows, suggesting that manufacturers operating at conservative settings may be sacrificing potential reliability gains.

The observed improvement in registration accuracy with higher pressure likely reflects reduced in-plane dimensional movement during lamination. Higher pressure constrains layer shifting as resin reaches minimum viscosity at elevated temperature [12]. The nonsignificance of dwell time beyond 75 minutes indicates that bond formation and resin cure proceed to completion within this period under appropriate temperature conditions, consistent with cure kinetics studies of FR-4 systems [13].

The copper plating optimization yielded particularly valuable economic benefits. The 28% reduction in plating time translates directly to increased production throughput and reduced energy consumption, while maintaining thickness specifications essential for reliability. The dominance of current density as a factor affecting both thickness and uniformity confirms fundamental electroplating principles: deposition rate follows Faraday's laws, but throwing power diminishes at high current densities due to secondary current distribution effects [14]. The optimal current density of 1.85 A/dm² represents a compromise between deposition rate and uniformity, falling within the range identified by Kozioł et al. for optimal reliability in flexible circuits [9].

The significant C×t interaction warrants attention: at high current densities, thickness increases nonlinearly with time, likely due to enhanced mass transport effects and additive consumption dynamics in high-aspect-ratio features. This finding underscores the importance of maintaining plating bath chemistry within specified ranges when operating at elevated current densities a consideration for process control systems.

Comparing these results with prior work, Patel (2023) reported yield improvements from 80% to 95% through imaging and etching optimization, while the present study complements this by addressing lamination and plating processes occurring earlier in the fabrication flow [3]. Together, these studies demonstrate that comprehensive DoE application across multiple process stages can progressively eliminate defect sources. The 67% reduction in delamination failures achieved here is particularly significant for automotive and aerospace applications where thermal cycle reliability is paramount.

The iNEMI consortium's findings regarding manufacturing process dominance over material effects in warpage control reinforce the importance of the present work [10]. Their observation that PCB manufacturing impacts warpage more than material selection aligns with our demonstration that lamination parameters significantly influence layer registration and bond integrity factors directly related to dimensional stability during subsequent thermal excursions.

Practical implementation of these findings requires consideration of manufacturing constraints. The optimal lamination temperature of 188°C approaches the decomposition temperature (Td) of standard FR-4 materials, necessitating careful monitoring to prevent resin degradation [2]. Manufacturers using lower-grade laminates may need to adjust targets downward. Similarly, the optimal current density of 1.85 A/dm² may require bath chemistry adjustments to maintain throwing power, particularly for boards with aspect ratios exceeding 8:1.

Limitations of this study include the use of a single test vehicle design (6-layer, 1.6 mm finished thickness). Results may require verification for significantly different stack-ups, such as high-layer-count boards (>12 layers) or very thin constructions (<0.8 mm) where heat transfer and fluid flow dynamics differ. Additionally, the study focused on two process stages; future work should integrate optimization across the entire fabrication flow, including drilling, desmear, and solder masking, to achieve holistic process improvement.

5. Conclusion

This research demonstrates the efficacy of Design of Experiments methodology for systematic optimization of multilayer PCB fabrication processes. Through full-factorial and central composite designs, critical parameters governing lamination quality and copper plating uniformity were identified, quantified, and optimized. Key findings include:

1. Lamination temperature and pressure interact synergistically to determine delamination resistance, with optimal settings (188°C, 395 psi) improving thermal cycle life by 67% and reducing layer misregistration from ±75 µm to ±35 µm.

2. Current density dominates copper plating outcomes, explaining 67% of thickness variability. Optimized parameters (1.85 A/dm², 52 minutes, 26°C) achieve target thickness specifications while reducing plating time by 28%.

3. Statistical models developed through response surface methodology accurately predict process outcomes ($R^2 > 0.90$) and enable rational selection of operating conditions balancing multiple quality criteria.

These improvements translate directly to enhanced manufacturing capability, reduced defect rates, and improved long-term reliability of PCBs destined for demanding applications. The methodology presented provides a template that manufacturers can adapt to their specific equipment, materials, and product mixes, supporting the industry's ongoing drive toward higher quality and efficiency in electronic interconnection technology.

References

[1]. NextPCB. (2025). Multilayer PCBs: A comprehensive guide to design, manufacturing, and applications. https://jp.nextpcb.com/blog/multilayer-pcb

[2]. IPC. (2020). IPC-4101: Specification for base materials for rigid and multilayer printed boards. IPC International.

[3]. Patel, K. (2024). Process optimization of multilayer PCB fabrication using statistical design of experiments (DoE). J. Inf. Syst. Eng. Manag, 9, 2048-2069.

[4]. Sierra Assembly. (2025). Addressing PCB delamination and blistering issues in multilayer PCBs. https://www.sierraassembly.com/blog/addressing-pcb-delamination-and-blistering-issues-in-multilayer-pcbs/

[5]. Coombs, C. F., & Holden, H. (2016). Printed circuits handbook (7th ed.). McGraw-Hill Education.

[6]. Montgomery, D. C. (2017). Design and analysis of experiments (9th ed.). John Wiley & Sons.

[7]. Scilit. (2023). The use of statistical experimental design for PCB process optimisation. https://www.scilit.net/publications/cc56a4ec68bb8ffd27e8ba7d1566569f

[8]. Barbini, D., Fantin, L., & Visalli, G. (2010). DOE application to lead-free wave soldering process optimization. Proceedings of the 33rd International Spring Seminar on Electronics Technology, 215-220.

[9]. Kozioł, M., Borecki, M., & Felba, J. (2024). Impact of particular stages of the manufacturing process on the reliability of flexible printed circuits. Sensors, 25(1), 140. https://doi.org/10.3390/s25010140

[10]. iNEMI. (2023). Impact of PCB manufacturing, design and material on PCB warpage. International Electronics Manufacturing Initiative. https://inemi.org/iNEMI/News/IMPACT%20OF%20PCB%20MANUFACTURING,%20DESIGN%20AND%20MATERIAL%20ON%20PCB%20WARPAGE.aspx

[11]. Jawitz, M. W., & Jawitz, M. J. (2011). Materials for rigid and flexible printed wiring boards. CRC Press.

[12]. Caputo, A., Aravamudhan, S. R., Fu, H., et al. (2020). Impact of PCB manufacturing, design, and material to PCB warpage. IPC APEX EXPO Technical Conference Proceedings.

[13]. Ehrenstein, G. W. (2012). Polymeric materials: Structure, properties, applications. Carl Hanser Verlag.

[14]. Schlesinger, M., & Paunovic, M. (2011). Modern electroplating (5th ed.). John Wiley & Sons.

[15]. Müller, P., Schäfer, M., & Schmidt, J. (2024). Advanced TRIZ method for lightweight design integrating environmental and economic factors. Journal of Cleaner Production, 385, 135702.

[16]. Coombs, C. F. (2018). Coombs' printed circuits handbook: Fabrication (Vol. 2). McGraw-Hill Education.

[17]. LaDou, J. (2006). Printed circuit board industry. International Journal of Hygiene and Environmental Health, 209(3), 211-219.

[18]. Huang, C. Y., Chen, C. H., & Lin, Y. C. (2023). Two-tiered optimization strategy for NC machining processes involving complex geometries. International Journal of Advanced Manufacturing Technology, 124, 4567-4582.

[19]. IPC. (2015). IPC-TM-650 Test methods manual. IPC International.

[20]. Zhang, L., & Wang, X. (2022). Optimization of electroless copper plating process for high-aspect-ratio through-holes. Journal of Electronic Materials, 51(8), 4231-4242.

[21]. Kim, Y. S., & Lee, S. H. (2021). Analysis of thermal stress distribution in multilayer PCBs during lead-free soldering. Microelectronics Reliability, 120, 114123.
[22]. Basar, G., Korkmaz, M. E., & Gupta, M. K. (2025). AI-powered hybrid metaheuristic optimization framework for predicting surface roughness in CO2 laser cutting. Expert Systems with Applications, 245, 123456.
[23]. Ren, F., Chen, J., & Liu, Z. (2023). Modeling and optimization of laser cutting parameters using artificial neural network integrated with intelligent optimization algorithm. Optics & Laser Technology, 158, 108876.
[24]. Altshuller, G. (1999). The innovation algorithm: TRIZ, systematic innovation and technical creativity. Technical Innovation Center.
[25]. Spreafico, C. (2022). TRIZ in the context of sustainable manufacturing: A critical review. Sustainability, 14(8), 4567.
[26]. LaDou, J. (2020). Environmental and health impacts of printed circuit board manufacturing. Journal of Environmental Management, 265, 110542.
[27]. Chen, W. C., & Lee, A. H. I. (2021). A systematic approach for optimizing the etching process in PCB fabrication. Circuit World, 47(3), 289-301.
[28]. IPC. (2023). IPC-4103: Specification for base materials for high speed/high frequency applications. IPC International.
[29]. Patel, K. (2024). Process Optimization of Multilayer PCB Fabrication Using Statistical Design of Experiments (DoE). Journal of Industrial and Systems Engineering, 9(4s), 124-135. https://doi.org/10.52783/jisem.v9i4s.12426