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Research Article

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Posted Date: May 19th, 2026

DOI: https://doi.org/10.21203/rs.3.rs-8997110/v1

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Additional Declarations: No competing interests reported.

Synergistic Control of Ambipolar Conduction in Ge-based Nanowire TFETs Using Gate Underlap and SiGeSn Heterojunction Barriers

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Abstract

Tunnel field-effect transistors (TFETs) offer sub-60 mV/dec switching for ultra-low-power logic, but ambipolar conduction at the drain-side junction remains a critical limiter. We present a p-type Ge gate-all-around (GAA) nanowire TFET (NW-TFET) that synergistically combines a drain-side gate underlap with a local SiGeSn heterojunction barrier to selectively suppress reverse band-to-band tunneling (BTBT) while preserving efficient forward tunneling. The barrier is realized with $Si_{0.49}Ge_{0.38}Sn_{0.13}$, which is Ge-matched having a bandgap of $E_g \approx 0.92$ eV. Using a calibrated TCAD deck, employing non-local BTBT and trap-assisted tunneling, we map the electrostatic/material design space across DC and RF characteristics. With $L_{underlap} = L_{barrier} = 20$ nm, the co-optimized device achieves an ambipolar current of $I_{amb} = 2.4 \times 10^{-13}$ A/μm, while maintaining robust forward conduction and a high cut-off frequency of 6×10^{10} Hz. Compared to underlap-only or barrier-only variants, the co-located barrier beneath the underlapped drain more effectively widens the drain-side tunneling width and relaxes the gate–drain field, thereby closing the parasitic branch across gate bias without substantially degrading I_{ON}. Moreover, under realistic interface-trap densities, work-function retargeting recenters the device, recovering ON/OFF and RF metrics. These results establish a practical, CMOS-compatible route to ambipolar suppression in Ge NW-TFETs using co-optimized electrostatics and group-IV band-engineering.

Keywords: Ge-based TFET; Gate underlap; SiGeSn barrier; ON/OFF ratio; cut-off frequency; TCAD simulation.

1. Introduction

Tunnel field-effect transistors (TFETs) have emerged as auspicious contenders for ultra-low-power electronics owing to their potential to accomplish sub-60 mV/decade subthreshold swing, enabling supply-voltage scaling beyond the limits of conventional MOSFETs. In TFETs, current conduction is primarily governed by band-to-band tunneling (BTBT) instead of thermionic emission. This mechanism presents significant reductions in static and dynamic power consumption for logic and mixed-signal applications. Among the various TFET architectures, nanowire geometries and high-mobility channel materials such as Germanium (Ge) have attracted particular attention because the strong electrostatic gate control and narrow bandgap can substantially enhance the ON-state tunneling probability. However, the narrow bandgap of Ge also imposes ambipolar conduction, which severely degrades device OFF-state leakage and noise margins. In addition, Ge compared to silicon (Si) enables low-voltage operation, which leads to reduced power consumption and potentially faster switching speeds. The low processing temperatures associated with Ge-based technologies further ensure compatibility with advanced high-k dielectrics and metal gate stacks [1].

Notably, ambipolar current originates from parasitic tunneling at the drain–channel junction when the gate bias is reversed with respect to the source junction. In scaled TFETs with steep junctions and high gate–drain coupling, the drain valence (or conduction) band can align with the channel bands, opening an unintended tunneling window that gives rise to significant reverse current. Device-level techniques to suppress this issue include gate–drain underlap, low-k drain spacers, drain-side dielectric pockets, asymmetric doping, and hetero-dielectric back oxides. Gate–drain underlap decreases the electric field at the drain junction and has been shown, experimentally in vertical nanowire TFETs, to lower the minimum current and improve subthreshold swing, albeit with a trade-off of reduced ON current [2–4]. In planar/double-gate TFETs, compact modeling and TCAD corroborate that underlap alleviates ambipolar current and Miller capacitance while slightly degrading ON-state conduction [5]. Further, overlapping or stacked gates on the drain can confine gate control to the source-side tunneling junction and reduce ambipolarity, though increased gate-to-drain capacitance (C_{gd}) may penalize RF figures of merit [6,7]. Drain-side dielectric engineering provides another effective mechanism. Introducing a high-k dielectric pocket (DP) at the channel–drain interface increases the effective tunneling width on the drain side, significantly suppressing ambipolar current without deteriorating ON current. The strategic placement and thickness optimization of the DP can also lower C_{gd} and thus improve f_T [8–10]. Similarly, hetero-dielectric BOX designs (e.g.,

SiO_2 under source/channel and HfO_2 under drain) deplete the drain interface and fully suppress ambipolarity by widening the drain-side tunneling barrier [11,12]. Spacer engineering with low-k material above the drain has been reported to concurrently suppress ambipolarity under overlap conditions and preserve high-frequency performance [13].

From a circuit perspective, both symmetric and asymmetric ambipolarity adversely impact logic correctness and power in complementary TFET circuits, emphasizing that suppression techniques must be validated beyond DC metrics [14]. In nanowire and gate-all-around (GAA) geometries, the stronger electrostatics generally help ambipolar mitigation, yet careful co-optimization of underlap/overlap length, oxide permittivity, and gate segmentation is essential to balance DC and analog/RF figures of merit (g_m/I_d, intrinsic gain, f_T, GBW) [15]. Gate underlap can effectively relax the electric field at the drain junction and push the onset of ambipolar conduction to higher gate voltages; however, excessive underlap generally reduces gate controllability over the channel and may penalize the ON current and high-frequency metrics. Thus, a careful trade-off is required between ambipolar suppression and overall analog/RF performance.

In parallel, heterojunction engineering has been widely explored as a powerful knob to tailor the tunneling landscape in TFETs. Heterojunction TFETs tailor band alignment to simultaneously enhance the source tunneling junction and suppress drain-side parasitic tunneling. Ge-channel heterostructures with Si source/drain or Ge/Si L-shaped junctions exploit direct BTBT at the source while using a larger-bandgap drain to mitigate ambipolar leakage, improving ON-current and SS with reduced reverse conduction [16,17]. Group-IV alloys incorporating Sn (GeSn) provide small/direct bandgaps at the source for high BTBT rates, whereas ternary Si–Ge–Sn (SiGeSn) alloys offer wider bandgaps suitable for the drain side. Combined GeSn/SiGeSn type-II staggered heterojunctions have been theoretically and numerically shown to boost I_{ON} (≈3.4×) and steepen SS versus GeSn homojunction TFETs while limiting ambipolarity [18–20]. SiGeSn alloys can be inserted as wider-bandgap barrier or channel segments in MOSFET structures to suppress OFF-state leakage. This can be done by lowering intrinsic carrier density and mitigating band-to-band tunneling/gate-induced drain leakage, while remaining monolithically integrable on Si. Recent epitaxy advances report SiGeSn nanowire MOSFETs and Ge/(Si)GeSn heterostructures with engineered band alignment, indicating practical routes to reduce I_{OFF} via band-engineering within group-IV stacks [21-25]. Nonetheless, many of these approaches are implemented in planar structures and often rely on abrupt material transitions that may introduce strain, interface traps, and process complexity. Moreover, most prior works treat the hetero-barrier and the electrostatic

design (e.g., gate overlap/underlap) as largely independent mechanisms, without fully exploring their coupled impact on both DC and RF/analog figures of merit.

Despite the extensive literature on ambipolar mitigation, there is still a lack of systematic studies that examine the interplay between gate underlap and bandgap-engineered hetero-barriers in a single, self-consistent TFET design, particularly in nanowire geometries and with attention to both DC and RF/analog performances. Nanowire architectures provide an attractive platform to revisit this problem because their quasi-one-dimensional nature intrinsically alleviates stress and enhances electrostatic control. In this work, we consider a Ge p-channel nanowire TFET, chosen for its narrow bandgap and high tunneling efficiency, while a SiGeSn alloy is employed to form a local heterojunction barrier near the drain. The SiGeSn composition can be engineered such that its bandgap is higher than that of Ge, thereby selectively suppressing parasitic tunneling at the drain side without significantly perturbing the source tunneling junction. A key advantage of SiGeSn grown on Ge is the ability to achieve lattice matching through compositional optimization, specifically by maintaining a Si/Sn ratio of ~3.7. This condition suppresses strain accumulation and mitigates the formation of interface defects. This material system thus offers a flexible and physically realistic route to separate ON-state enhancement from OFF-state control. Thus, the present work proposes and analyzes a Ge-based nanowire NW-TFET that simultaneously employs (i) a SiGeSn heterojunction barrier with $E_g^{\text{barrier}} > E_g^{\text{Ge}}$ and (ii) an optimized gate underlap from the drain side. We demonstrate, through detailed device-level TCAD simulations, that the cooperative action of these two design knobs can strongly suppress ambipolar current while preserving key RF and analog figures of merit. This dual-mechanism strategy and the associated design space exploration address a clear gap in existing TFET ambipolar-suppression approaches.

2. Methods and Materials

2.1. TCAD Simulation Approach

To ensure that the simulated characteristics reflect realistic device physics, we adopt a comprehensive TCAD model. Specifically, band-to-band tunneling is treated using a nonlocal BTBT formulation, which is essential for accurately resolving tunneling paths. Carrier injection over potential barriers was described through thermionic-emission transport. Fermi–Dirac statistics are utilized, while the lattice temperature is kept fixed at 300 K. Recombination is modeled using a concentration-dependent Shockley–Read–Hall framework and Auger recombination mechanism to account for trap-assisted carrier loss under both subthreshold and high-injection conditions [26]. Carrier mobility in Ge is treated as constant ($\mu_e =$

$3900\ \mathrm{cm^2\ V^{-1}\ s^{-1}}$, $\mu_h = 1800\ \mathrm{cm^2\ V^{-1}\ s^{-1}}$). In addition, the intrinsic Ge band gap is set to 0.68 eV, and band-gap narrowing is enabled to account for high-doping effects.

Notably, accurate material calibration is essential for predictive TCAD studies because it anchors the transport and tunneling models to measured device behavior. This ensures that subsequent design optimizations reflect practical device physics rather than idealized assumptions [27]. Here, we calibrate our simulation framework against the fabricated Ge/Si nanowire device with a Ge source reported in [28]. The reference structure employs SiO_2 as the gate dielectric ($\varepsilon_r = 3.9$), an Al metal gate with a work function of 4.75 eV, and a nanowire core radius of $R = 30$ nm. The source, channel, and drain segments each have a height of 50 nm, with doping concentrations of $1 \times 10^{20}\ \mathrm{atoms/cm^3}$ (source), $1 \times 10^{16}\ \mathrm{atoms/cm^3}$ (channel), and $1 \times 10^{19}\ \mathrm{atoms/cm^3}$ (drain). The effective oxide thickness is EOT = 2 nm, and the gate is overlapped to the source, consistent with the experimental layout.

In the calibrated deck, the tunneling effective masses of Ge are set to 0.20 and 0.14 for electrons and holes, respectively, with carrier lifetimes fixed at 0.1 ns. These values were selected to reproduce the experimentally observed characteristics for the structure reported in [28], as shown in the inset of Figure 1, using the same experimental parameters, where the gate length (L_G) is 150 nm, the channel length is 220 nm, the gate underlap length from the drain ($L_{underlap}$) is 100 nm, the gate on source overlap length ($L_{overlap}$) is 30 nm, while the radius is R = 70 nm. Figure 1 also demonstrates that the resulting simulation closely matches the measured transfer response of the reference device at $V_{DS} = 1.5$ V. To capture non-ideal leakage mechanisms, the OFF-state current was fitted by enabling the trap-assisted tunneling (TAT) model. Moreover, interface trap charges at the semiconductor/oxide interface were introduced to account for interfacial defect states. Building on this validated calibration, the next section presents the geometrical and material configurations of the conventional and proposed devices developed from this baseline.

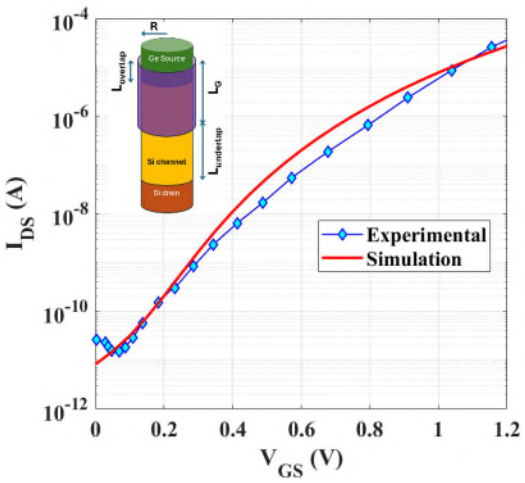
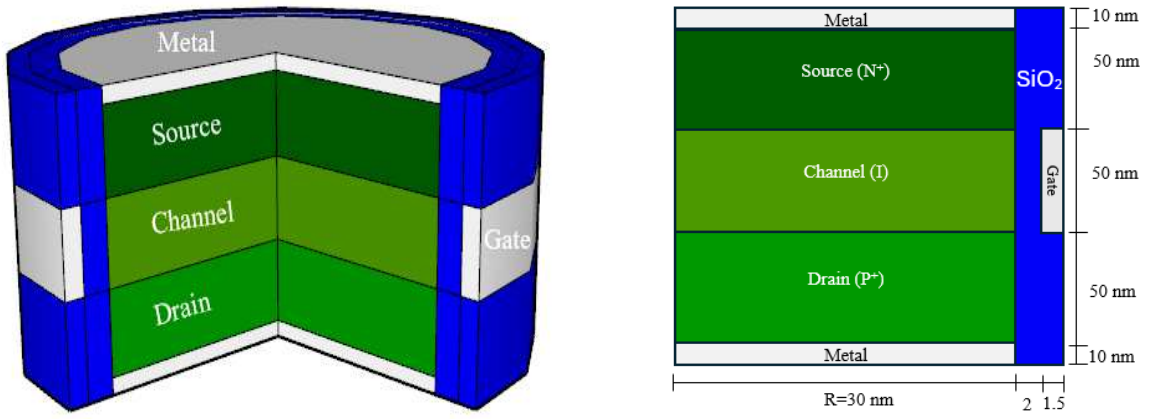


Figure 1. Comparison between experimental and simulated transfer characteristics of the Ge/Si vertical nanowire TFET at V_{DS} = 1.5 V.

2.2. Conventional and Proposed Device Structure

The baseline conventional structure in Figure 2 is used as a reference, and the device is refined step by step until the final proposed NW-TFET is obtained. The structure consists of a GAA Ge nanowire with a core radius of $R = 30$ nm. The device is vertically segmented into source, channel, and drain regions, each having a height of 50 nm. The doping concentrations are set to 1×10^{20} cm^{-3} for the N^{+} source, 1×10^{16} cm^{-3} for the lightly doped channel, and 1×10^{19} cm^{-3} for the P^{+} drain. The gate stack employs a geometry with EOT of 2 nm.

Figure 2a illustrates the three-dimensional schematic of the NW-TFET. The gate-all-around metal electrode fully encloses the Ge core, with the gate edge aligned precisely at the source–channel interface, where the gate continuously covers the channel region up to the channel–drain boundary. Figure 2b presents the corresponding 2D cross-section of the nanowire. The Ge core is shown with its vertically stacked doping regions The vertical dimensions denote the 50 nm heights of the source, channel, and drain segments. The surrounding SiO_2 gate dielectric represents the spacers above the source and drain regions.



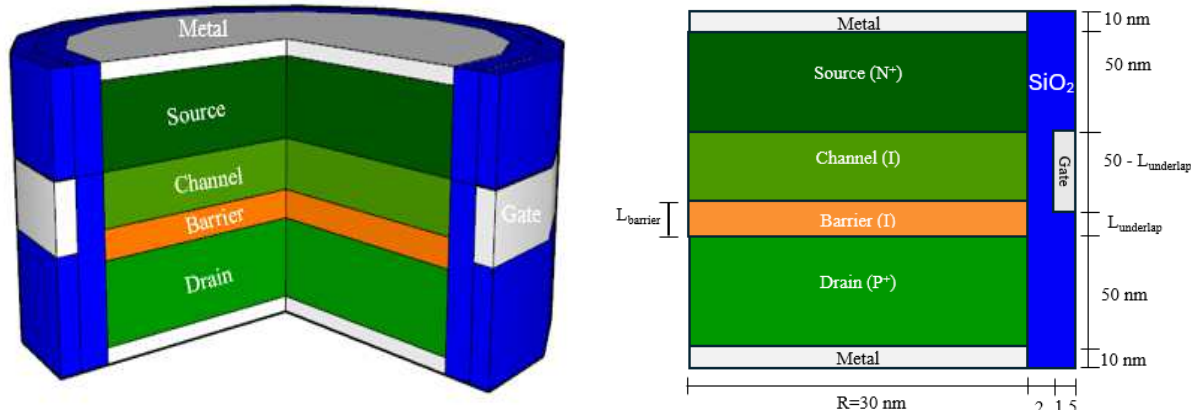
(a) (b)

Figure 2. Conventional all-Ge NW device (a) three-dimensional (3D) cross-section (b) two-dimensional (2D) cross-section.

To address the limitations imposed by Ge narrow bandgap, manifested as increased ambipolar conduction and off-state leakage, we propose introducing a drain-side heterostructure barrier within the channel. Specifically, the barrier is implemented by inserting a heterostructure layer near the drain, where ambipolar injection is most pronounced. This band-engineering approach suppresses parasitic carrier transport and reduces leakage while preserving the desired BTBT current in the ON state. In practice, this barrier can be engineered using a Ge/$Si_xGe_{1-x-y}Sn_y$ heterostructure. Effective implementation of this concept relies on Ge/SiGeSn epitaxial heterostructures, which provide a practical platform for bandgap and band-edge engineering within Ge-compatible technology. A key advantage of SiGeSn grown on Ge is that its composition can be tuned for lattice matching to Ge by maintaining a Si/Sn ratio of approximately 3.7, thereby enabling high-quality layers with reduced strain-related defects. In this study, we therefore consider three Ge-lattice-matched alloy compositions with $y < 0.15$ (specifically, $y = 0.05$, 0.10, and 0.13) to ensure realistic growth feasibility, and we extract the corresponding bandgap and band offsets using a quadratic interpolation model for the ternary alloy together with the Jaros approach for Ge/SiGeSn band alignment [29].

The proposed drain-engineered nanowire device is schematically illustrated in Figure 3. A drain-side underlap of length L_{underlap} is introduced while maintaining alignment of the gate edge with the source–channel interface. For a nominal channel length of $L_{\text{ch}} = 50$ nm, the corresponding gate length becomes $L_{\text{G}} = (50 - L_{\text{underlap}})$ nm. Both L_{ch} and L_{G} can be further scaled, subject to the conventional $I_{\text{ON}}/I_{\text{OFF}}$ trade-off. To realize the intended energy barrier near the drain, the drain-side portion of the intrinsic Ge channel is replaced by an intrinsic $Si_{0.49}Ge_{0.38}Sn_{0.13}$ segment of length L_{barrier}, as dictated by the design. Figure 3a shows a 3D

cutaway view of the GAA nanowire stack, whereas Figure 3b presents the corresponding 2D cross-section, explicitly indicating L_{barrier} and L_{underlap} used in the proposed design.



(a) (b)

Figure 3. Schematic of the proposed NW-TFET Ge-based structure: (a) 3D cross-section and (b) corresponding 2D cross-section.

For all subsequent simulations, the device is operated in p-channel mode; therefore, the applied bias polarities and the definitions of current and voltage conditions follow the hole-conduction convention. Accordingly, the drain voltage is fixed at $V_{DS} = -1$ V (i.e., the drain is biased negative with respect to the source). The ON, OFF, and ambipolar currents are calculated at gate voltages of -1 V, 0 V, and 1 V, respectively. The threshold voltage is computed at $|I_{DS}| = 10^{-7}$ A. The cut-off frequency, f_T, is evaluated using Equation (1).

$$f_T = \frac{g_m}{2\pi C_{GG}} \tag{1}$$

where g_m is the transconductance and C_{GG} is the overall gate capacitance. The average SS, SS_{av}, is computed based on Equation (2).

$$SS_{av} = \frac{V_T - V_{OFF}}{\log(I_{V_T}) - \log(I_{V_{OFF}})} \tag{2}$$

with V_T is the threshold voltage, V_{OFF} is the voltage at the OFF-state point, I_{V_T} is the drain current determined at V_T, and $I_{V_{OFF}}$ is the drain current obtained at V_{OFF}.

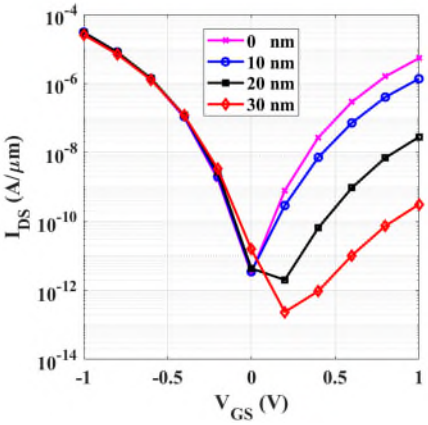
3. Results and Discussion

In this section, the different phases of the design of the proposed Ge p-type GAA NW-TFET are presented, with the goal of suppressing ambipolar leakage while preserving forward BTBT and maintaining competitive RF behavior. We first investigate the role of the drain-side gate underlap length and evaluate its impact on the transfer characteristics and small-signal metrics. Next, we introduce a band-engineering mechanism by inserting a Ge-lattice-matched

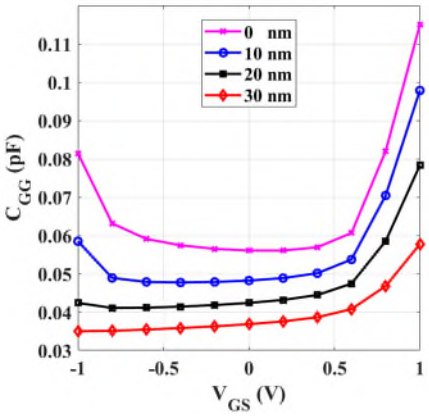
SiGeSn drain-side barrier and sweeping its bandgap and length to quantify how a wider-bandgap segment reshapes drain-side band alignment and reduces leakage. Building on the two single-knob studies, we then co-integrate the barrier with the underlapped region to demonstrate their synergistic action. The co-optimization is subsequently refined by independently tuning barrier length versus underlap length. Finally, we assess robustness to fabrication variability by benchmarking multiple co-optimized design corners and confirming smooth shifts in DC/RF metrics under realistic geometric spreads. We then evaluate non-idealities, focusing on oxide/semiconductor interface traps and the role of work-function retargeting in recovering electrostatics and limiting trap-assisted leakage.

3.1. Effect of Gate–Drain Underlap

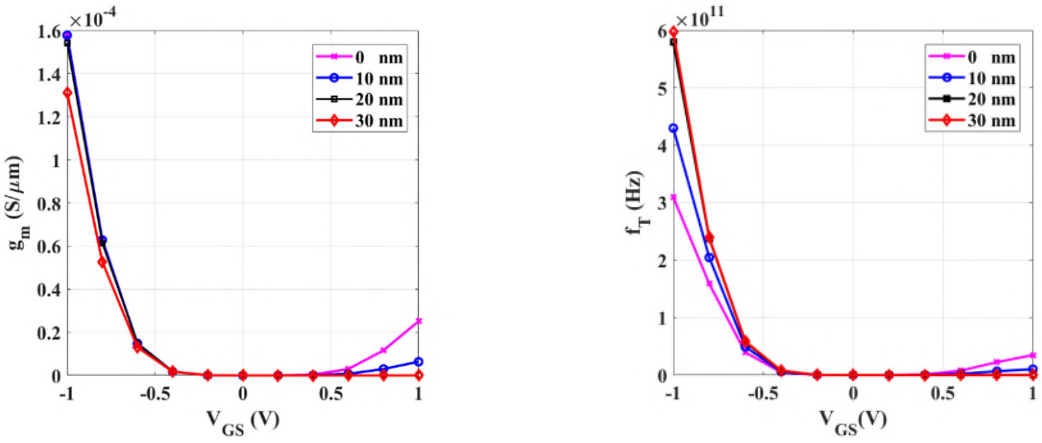
We first explore how gate–drain underlap alone reshapes the transfer and RF behavior. As the underlap increases, the drain-side electric field is relaxed and the unintended tunneling window responsible for the ambipolar branch becomes progressively less accessible. This evolution is reflected in the set of curves collected in Figure 4. The I_{DS}–V_{GS} traces in Figure 4a show the diminishing reverse conduction. The total gate capacitance C_{GG} in Figure 4b declines with underlap, implying reduced gate–drain coupling. Further, the transconductance g_m in Figure 4c slightly decreases at large underlap where gate control weakens. Finally, the cutoff frequency f_T in Figure 4d improves as C_{GG} drops, keeping g_m/C_{GG} favorable in the moderate-underlap regime.



(a)



(b)



(c) (d)

Figure 4. Device characteristics of the initial phase of the design at different underlap values: (a) I_{DS}, (b) C_{GG}, (c) g_m, and (d) f_T as functions of V_{GS}.

Examining the device metrics (I_{ON}, I_{ON}/I_{OFF}, I_{amb}, and f_{Tmax}) as a function of the underlap length $L_{underlap}$ provides a clearer view of the design trade-offs. In Figure 5a, I_{ON} gradually decreases as $L_{underlap}$ increases, whereas Figure 5b indicates that the I_{ON}/I_{OFF} ratio reaches a maximum at an intermediate underlap. In contrast, Figure 5c shows a pronounced, multi-order suppression of the ambipolar current (I_{amb}) with increasing underlap. Finally, Figure 5d shows an overall increase in f_{Tmax} as electrostatic coupling between the drain and the gated region is weakened. Collectively, these trends confirm that the underlap primarily acts to screen the drain potential, thereby mitigating drain-induced leakage pathways while largely preserving the source-side tunneling junction.

The quantitative results summarized in Table 1 further support this interpretation. Specifically, I_{ON} decreases by only $\sim 15\%$, from 5.8×10^{-6} to 4.87×10^{-6} A/μm, when $L_{underlap}$ is extended to 30 nm, while I_{amb} is reduced from 1.02×10^{-6} to 5.89×10^{-11} A/μm (nearly five orders of magnitude). The I_{ON}/I_{OFF} ratio peaks near $L_{underlap} \approx 14$ nm at 1.2×10^{7}, and the average subthreshold swing SS_{av} remains approximately 96–100 mV/dec up to 20 nm before degrading at 30 nm. Meanwhile, f_{Tmax} increases from 6.26×10^{10} to 1.13×10^{11} Hz, consistent with a reduction in C_{GG} as the drain is progressively decoupled.

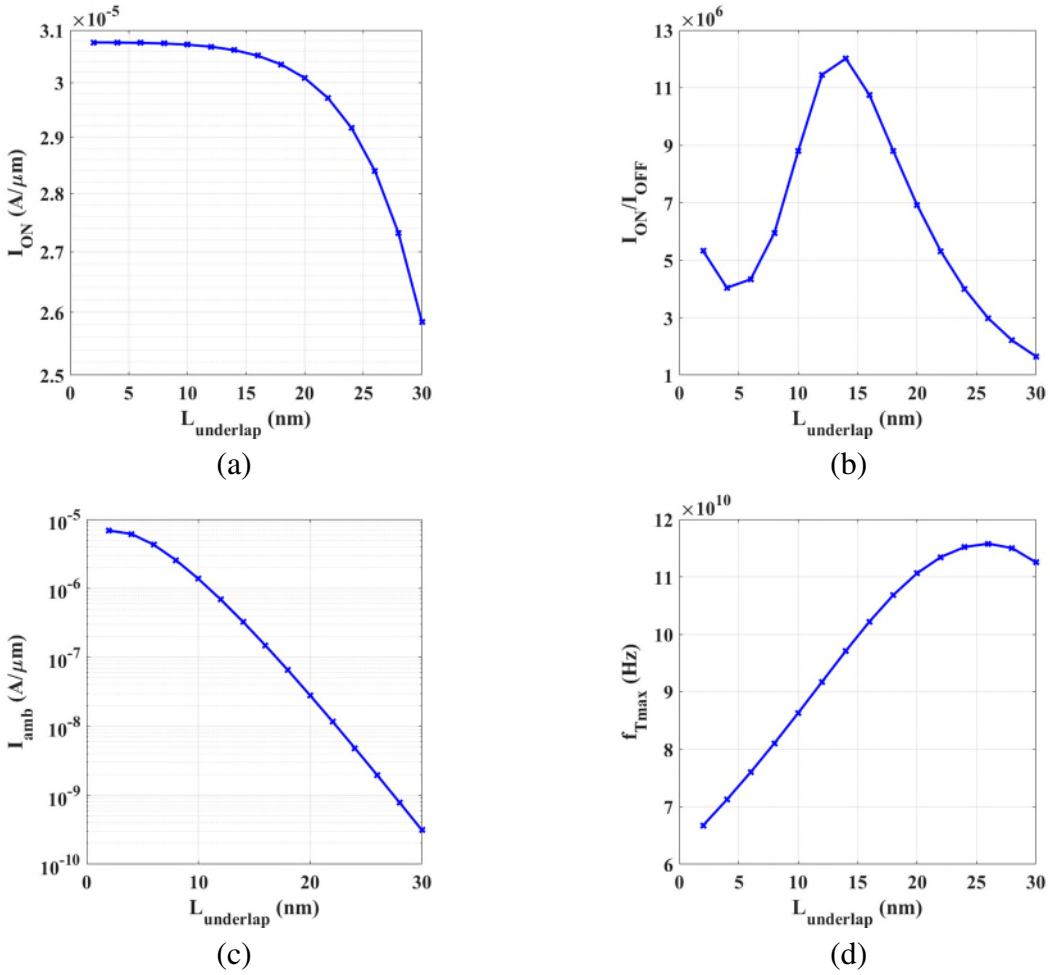


Figure 5. Device metrics of the all-Ge NW-TFET as a function of underlap length: (a) I_{ON} (b) ON/OFF current ratio, (c) I_{amb}, and (d) f_{Tmax}.

Table 1. Main performance parameters at different underlap lengths.

	No underlap	**14 nm underlap**	**20 nm underlap**	**30 nm underlap**
I_{ON} (A/μm)	5.80×10^{-6}	5.77×10^{-6}	5.67×10^{-6}	4.87×10^{-6}
I_{OFF} (A/μm)	5.96×10^{-13}	4.80×10^{-13}	8.19×10^{-13}	2.94×10^{-12}
ON/OFF ratio	9.72×10^{6}	1.20×10^{7}	6.92×10^{6}	1.65×10^{6}
I_{amb} (A/μm)	1.02×10^{-6}	6.13×10^{-8}	5.27×10^{-9}	5.89×10^{-11}
SS_{av} (mv/decade)	98.45	96.06	100.07	113.55
f_{Tmax} (Hz)	6.26×10^{10}	9.71×10^{10}	1.11×10^{11}	1.13×10^{11}
W_{min} at ambipolar (nm)	5.00	8.00	9.68	12.65

3.2. Field-Profile and BTBT Physics in case of Underlap

To anchor the previous device-level observations in physics, we examine the energy bands and local BTBT generation rates along the transport axis. As the underlap grows, the drain-side potential couples less strongly to the gate, which enlarges the minimum tunneling width, W_{min},

and attenuates the BTBT window on the drain side. This progression is visible across Figure 6, where Figure 6a, with no underlap, shows a narrow drain-side window that permits strong ambipolar conduction, as reflected by the elevated tunneling rates. Figure 6b and Figure 6c (at 14 and 20 nm) reveal a broadened barrier and suppressed BTBT rates. Moreover, Figure 6d demonstrates the lowest BTBT rates at an underlap length of 30 nm. These physical trends are quantitatively captured in Table 1. At the ambipolar operating point, the minimum tunneling width $W_{\min}$ increases from approximately 5 nm in the no-underlap case to 12.65 nm when $L_{\text{underlap}} = 30$ nm, which is consistent with the corresponding collapse of I_{amb}. The observed enhancement in f_T can be attributed primarily to a reduction in gate–drain capacitance C_{gd} as the drain becomes progressively decoupled from the gated region, while C_{gs} remains comparatively stable. This preserves a favorable g_m/C_{GG} ratio over moderate underlap lengths, before excessively long underlap begins to penalize overall device transconductance and speed.

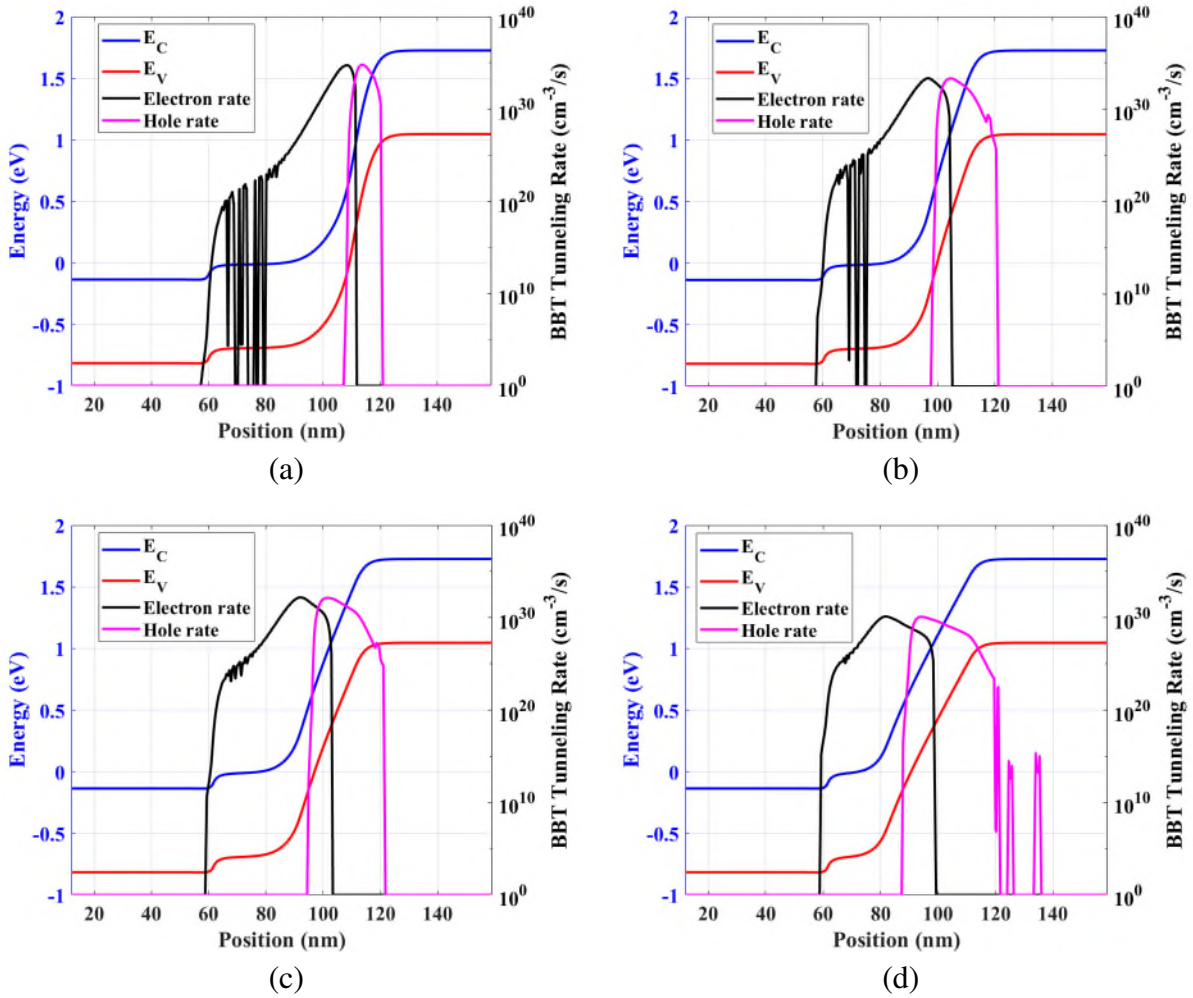


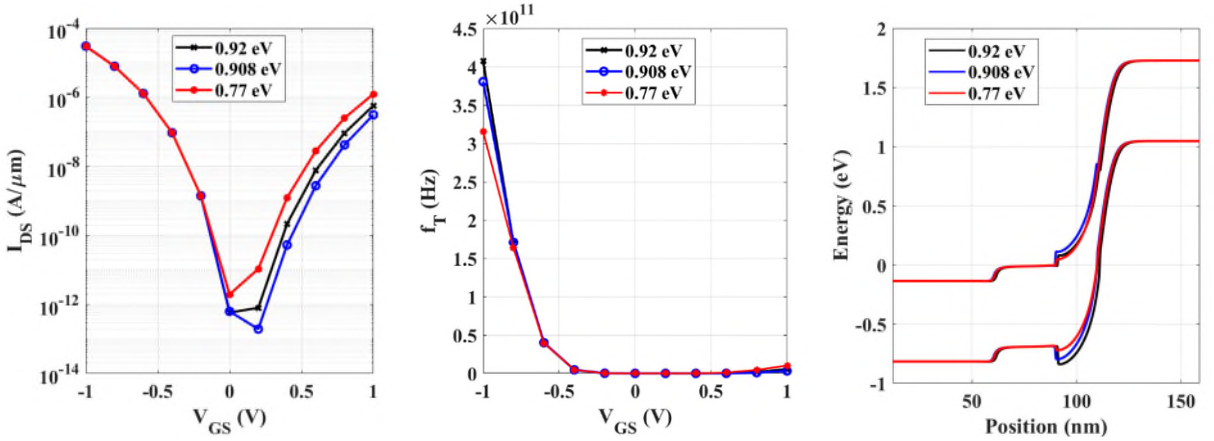
Figure 6. Energy band diagrams and BBT tunneling rates versus position at different underlap lengths: (a) at $L_{underlap} = 0$; (b) $L_{underlap} = 14\ nm$; (c) $L_{underlap} = 20\ nm$; (d) $L_{underlap} = 30\ nm$.

3.3. Barrier-Only Study

Building on the electrostatic insights, we isolate the role of band-engineering by replacing 20 nm of the channel with a 20 nm SiGeSn drain-side barrier without underlap and sweeping its bandgap. Following the Ge-lattice-matched heterostructure model in [29], the drain-side barrier is drawn from the SiGeSn ternary family on the Si/Sn ≈ 3.7 line, where the band gap is tuned by the mixing parameter x in $Ge_{1-x}(Si_{0.79}Sn_{0.21})_x$. In our simulation run, $E_g \approx 0.92$ eV is realized with $Si_{0.49}Ge_{0.38}Sn_{0.13}$, which lies on that Ge-matched line [29]. For $E_g \approx 0.908$ eV, compositions near $x \approx 0.23$ on the same Ge-matched line (e.g., $Si_{0.18}Ge_{0.59}Sn_{0.23}$) produce gaps in the 0.90–0.92 eV range at 300 K, while $E_g \approx 0.77$ eV is obtained near $x \approx 0.13$ (e.g., $Si_{0.10}Ge_{0.78}Sn_{0.12}$). These mappings are consistent with coherent-potential and empirical-pseudopotential band-structure calculations for Ge-matched SiGeSn alloys.

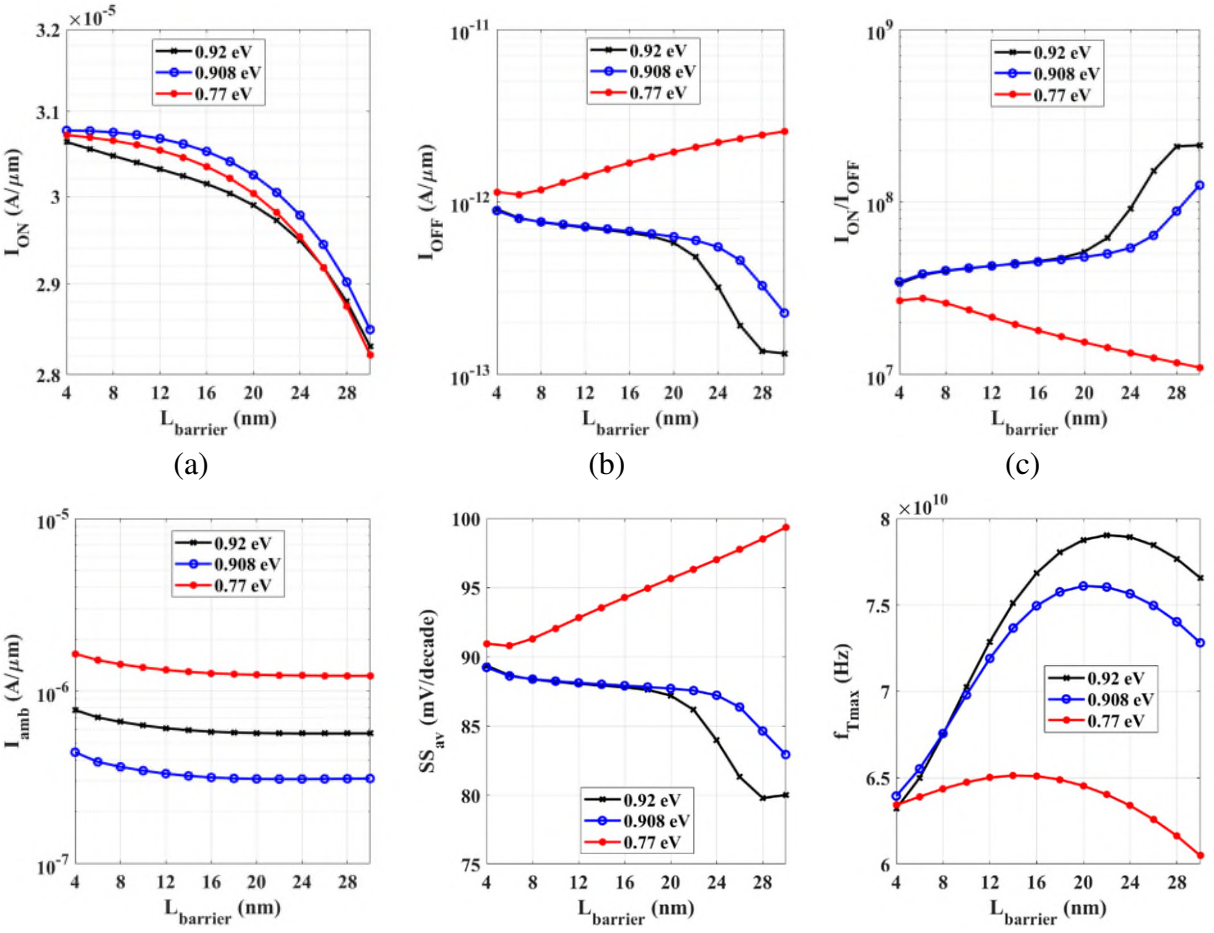
As the barrier E_g increases, the local band edges near the drain are lifted and the tunneling width on the drain side widens, which curbs drain-initiated BTBT. This is evident in Figure 7a by the noticeable reduction of the ambipolar branch. The RF response is monotonic in Figure 7b, where no change occurs in the ON direction, which guarantees that the RF is not significantly affected with the barrier insertion. The band diagrams in Figure 7c visualize this trade-off directly, with stronger conduction–valence separation around the drain as E_g rises. Crucially, the barrier alone does not fully suppress ambipolar conduction across the V_{GS} range as residual gate–drain fringing fields still allow a finite parasitic tunneling window. Thus, we studied the impact of the barrier width on the device metrics for further assessment.

Figure 8 sweeps the barrier width for three E_g choices (no underlap): Figure 8a–8f plot I_{ON}, I_{OFF}, ON/OFF ratio, I_{amb}, SS_{av}, and f_{Tmax}, respectively. Wider barriers more effectively suppress I_{amb}, and I_{OFF}, but beyond ~20 nm they start to erode I_{ON} and f_{Tmax} by over-widening the tunneling path and increasing series resistance. These trends identify a practical window of barrier widths and E_g that preserve ON-state conduction while reducing the parasitic branch. However, this limitation motivates the co-integration with modest gate–drain underlap, which simultaneously relaxes the drain-side field and places the barrier under weaker electrostatic influence so that the parasitic branch closes while forward BTBT and RF performance are preserved.



(a) (b) (c)

Figure 7. Exploration of the barrier energy gap for a 20 nm barrier on (a) I_{DS}, (b) f_T, (c) Energy band diagram.



(a) (b) (c)

(d) (e) (f)

Figure 8. Impact of barrier length on different metrics for different energy gaps with no underlap: (a) I_{ON}, (b) I_{OFF}, (c) ON/OFF ration, (d) I_{amb}, (e) SS_{av} and (f) f_{Tmax}.

3.4. Synergy of Underlap and Barrier

Combining electrostatic and material controls, we next co-locate the SiGeSn barrier beneath the underlapped drain region and set the barrier length equal to the underlap length, then sweep both length and barrier E_g. This co-optimization consistently results in widening the drain-side tunneling barrier while preserving source-side gate control. The resulting trends are evident across Figure 9. In Figure 9a, I_{ON} remains relatively stable for short-to-moderate lengths across the tested E_g values, with a gentle roll-off at larger lengths as the forward tunneling path becomes over-extended. Figure 9b shows a reduction in I_{OFF} as E_g grows, reflecting the combined energetic and electrostatic widening of the drain-side barrier. Consequently, Figure 9c exhibits a pronounced rise in the ON/OFF ratio that peaks within an intermediate window of length and E_g, where the parasitic branch is strongly restrained without substantially degrading the forward window. The same suppression mechanism appears directly in Figure 9d through a multi-order decrease in I_{amb} with increasing length and E_g, confirming that the barrier-underlap stack closes the drain-initiated tunneling window more effectively than either of the mechanism alone.

From a switching-steepness perspective, Figure 9e indicates that the average subthreshold swing SS_{av} initially improves as the parasitic window is narrowed, then can degrade if the length becomes excessive. This trend signifies diminished gate leverage and a broader electrostatic transition region. Finally, Figure 9f captures the RF outcome, where f_{Tmax} benefits in the moderate-length regime because underlap lowers C_{GD} (and hence C_{GG}) while the barrier suppresses reverse tunneling, but very long lengths introduce a modest g_m penalty that can offset the capacitance advantage. Taken together, Figure 9 maps a practical design envelope where barrier-equals-underlap delivers strong ambipolar suppression, high ON/OFF, and favorable f_{Tmax} without compromising the forward branch. Guided by these trends, we next fix the barrier bandgap at $E_g = 0.92$ eV and study the optimum pairing of barrier and underlap lengths to maximize ON/OFF and f_{Tmax} while preserving the forward branch.

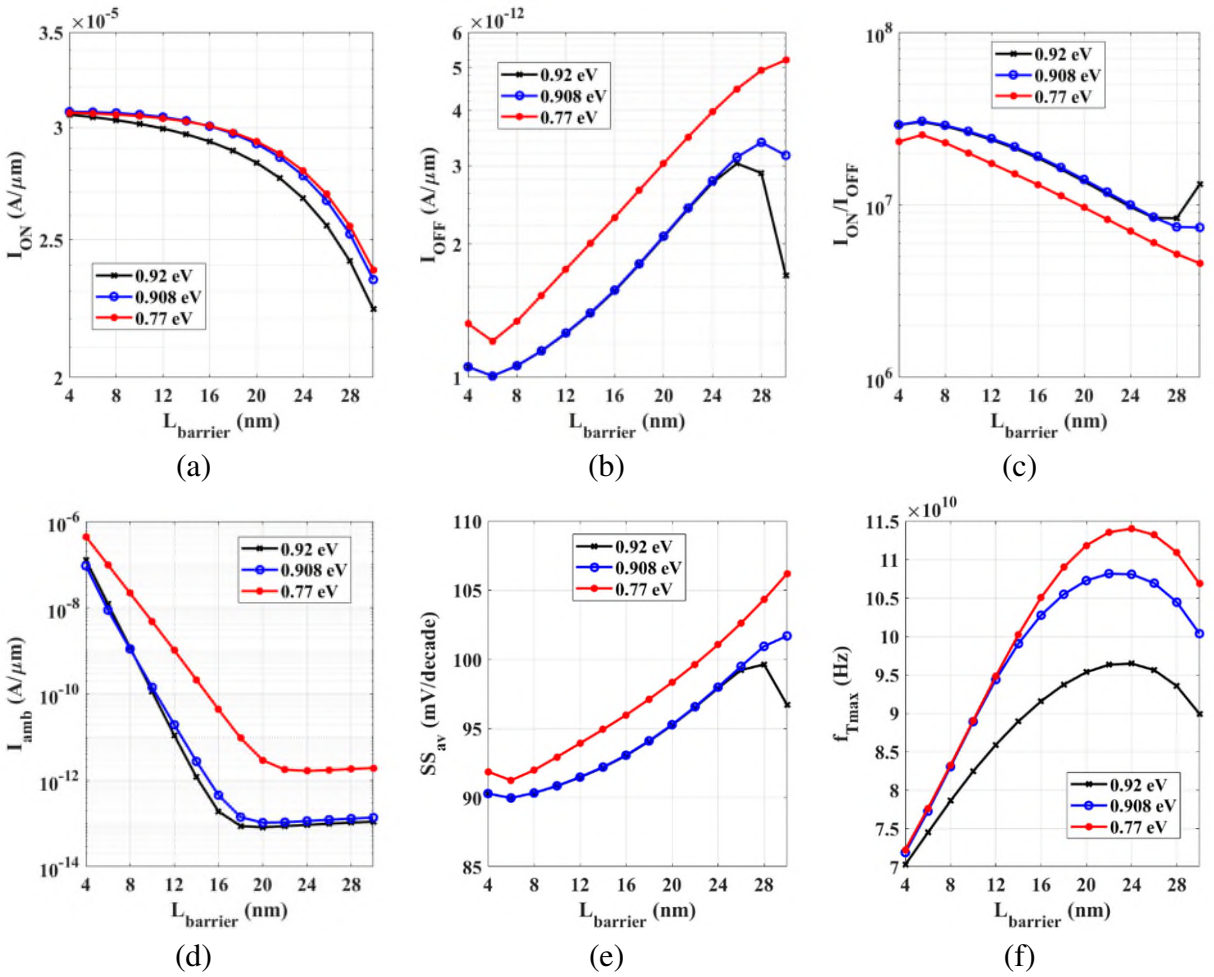


Figure 9. Influence of the barrier length on different metrics for different energy gaps at barrier equals the underlap: (a) I_{ON}, (b) I_{OFF}, (c) ON/OFF ratio, (d) I_{amb}, (e) SS_{av} and (f) f_{Tmax}.

3.5. Co-optimization of barrier and underlap lengths

After individually benchmarking gate–drain underlap and the SiGeSn drain-side barrier, we next co-optimize their lengths to identify a robust operating window that simultaneously suppresses drain-initiated BTBT while preserving forward BTBT drive and RF speed. The underlap primarily weakens gate–drain electrostatic coupling (relaxing the drain-side electric field), whereas the heterojunction barrier increases the effective energetic/tunneling barrier near the drain by inserting a wider-bandgap segment. Together, they enlarge the drain-side tunneling width and reduce the local BTBT generation responsible for ambipolar conduction. In this sweep, the barrier bandgap is fixed to the selected Ge-matched SiGeSn composition (as chosen from the prior optimization), while the barrier length L_{barrier} and the drain-side underlap length L_{under} are varied independently. Figure 10 summarizes the response across the key DC and RF metrics.

Figure 10a shows that I_{ON} experiences only a modest reduction as L_{barrier} increases, confirming that forward conduction, dominated by source-side BTBT, is largely preserved because the barrier is positioned near the drain. The reduction becomes more visible at larger underlap (e.g., 24 nm), where the ungated drain-side region is longer and the barrier adds additional tunneling resistance in the drain-proximal portion of the channel, slightly weakening the overall drive. The dominant benefit of co-optimization appears in Figures 10b–c. As L_{barrier} is extended beyond the short-barrier regime, I_{OFF} decreases sharply, which translates directly into a strong rise in the ON/OFF ratio. This behavior is consistent with the drain-side parasitic tunneling window progressively closing. The underlap screens the drain potential and reduces the electric field near the drain junction, while the wider-bandgap barrier further widens the forbidden region and reduces tunneling probability. In combination, these effects suppress the leakage floor far more effectively than either knob alone.

Figure 10d directly quantifies ambipolar suppression. A clear optimum emerges around a moderate underlap combined with a moderate barrier length, where drain-side BTBT is strongly limited without paying a disproportionate penalty in forward drive. In our sweep, the configuration $L_{\mathrm{under}} = 16$ nm with $L_{\mathrm{barrier}} = 18$ nm provides an effective minimum of I_{amb} while keeping I_{ON} at a practical level, thereby representing the best balance for ambipolar control under the selected barrier bandgap. Further, Figure 10e shows that the average subthreshold swing SS_{av} generally improves in the same region where I_{OFF} is minimized. This is expected because, in the presence of drain-side leakage pathways, the subthreshold behavior is no longer governed purely by source-side BTBT modulation but is increasingly limited by parasitic current components that broaden the apparent transition. Therefore, designs that most effectively suppress drain-side BTBT (via co-optimized underlap + barrier) also exhibit the lowest SS_{av}. Importantly, if further re-centering of the transfer curve is desired (e.g., to recover I_{ON} at a given I_{OFF}), work-function retargeting remains an additional design choice.

Finally, Figure 10f reports the peak cut-off frequency $f_{T,\mathrm{max}}$. Two counteracting trends dictate the behavior. Increasing underlap tends to reduce gate–drain coupling and therefore lowers the effective gate capacitance (favorable for RF). However, excessive underlap can weaken gate control and reduce g_m (unfavorable for RF). The data show that the 24 nm underlap case suffers a noticeable f_T degradation, indicating that the g_m penalty dominates at that larger underlap. In contrast, the moderate underlap (16 nm) combined with a moderate barrier length (18 nm) maintains a favorable f_T while still delivering strong ambipolar

suppression, reinforcing this point as a balanced DC/RF co-optimized design that is subsequently used as a reference corner for robustness analysis.

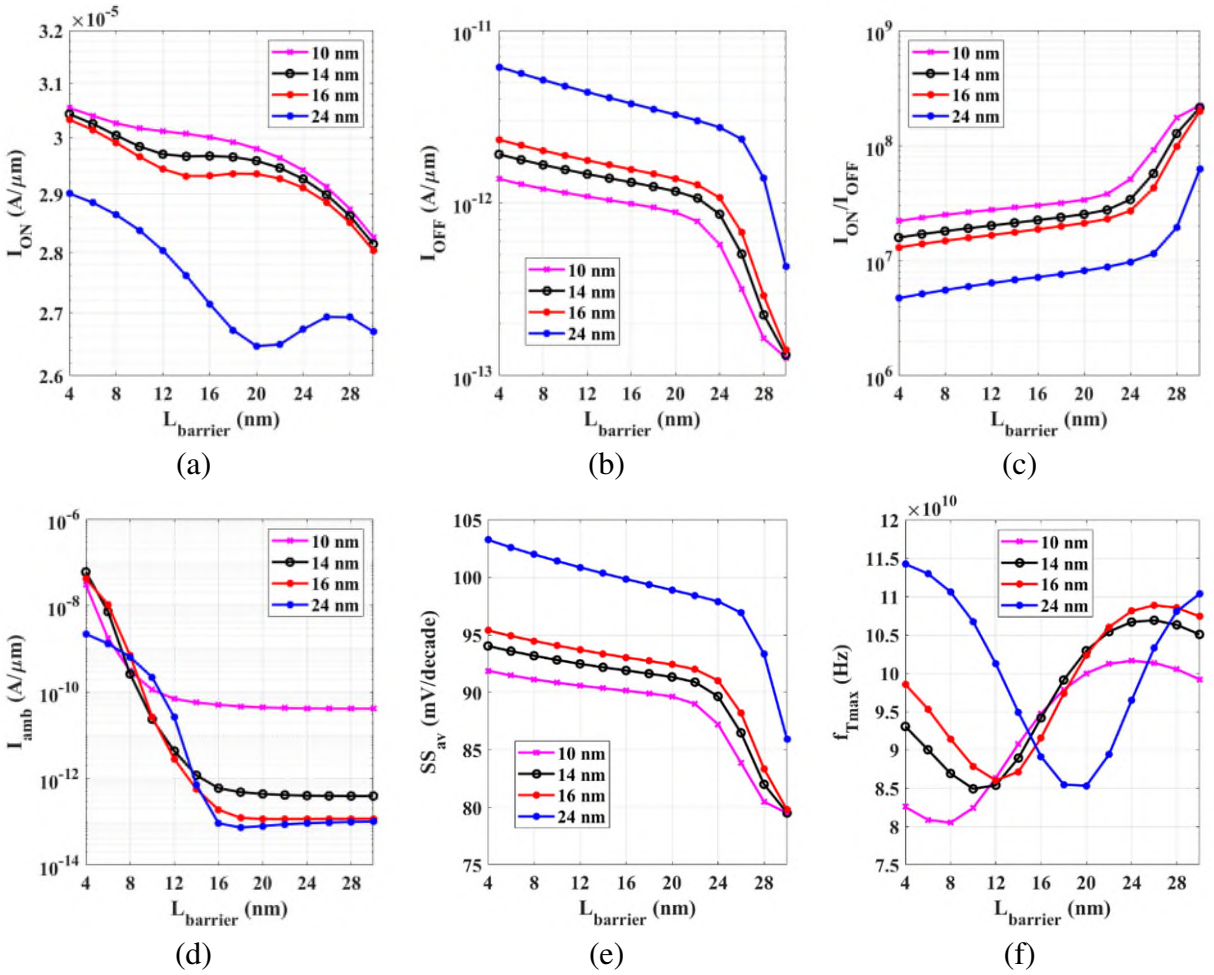


Figure 10. Impact of the barrier length on different metrics for different underlap lengths: (a) I_{ON}, (b) I_{OFF}, (c) ON/OFF ration, (d) I_{amb}, (e) SS_{av} and (f) f_{Tmax}.

The electrostatic screening discussed previously is directly evidenced by the electric-field profiles in Figure 11. When the gate is aligned with the drain (0-nm underlap), a strong gate–drain fringing field produces a highly localized field spike near the drain-side junction, with a peak on the order of 1.8×10^6 V/cm. As the drain-side underlap is increased (10–30 nm), the potential drop is redistributed over a longer ungated distance ($E \approx \Delta V/\Delta x$), and the maximum field at the drain-side tunneling region decreases markedly (down to 0.5×10^6 V/cm for the largest underlap). Because BTBT is exponentially sensitive to the local field (e.g., Kane-type behavior $G_{\mathrm{BTBT}} \propto E^2 \exp[-B/E]$), even a moderate reduction of the peak field yields a disproportionate suppression of drain-initiated BTBT, explaining the sharp drop in I_{OFF} and I_{amb} and the resulting rise in $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ observed in Figure 10b–d. Importantly, the source-side high-field region (responsible for forward BTBT in the ON-state) is far less affected by the

drain underlap/barrier placement. Therefore I_{ON} shows only a modest reduction, consistent with Figure 10a.

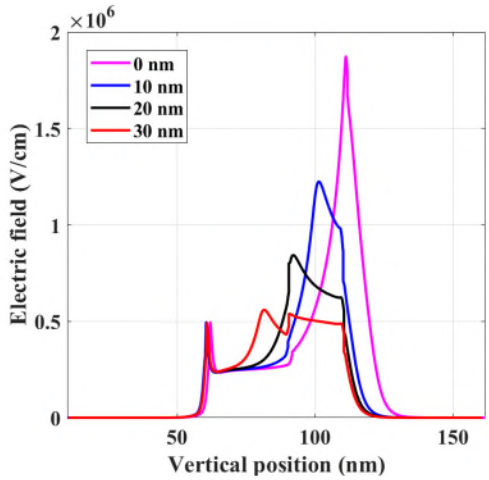


Figure 11. Electric-field magnitude along the transport direction (vertical position) under the OFF/ambipolar bias condition used in Figure 10, comparing drain-side underlap lengths $L_{under} = 0$, 10, 20, and 30 nm.

3.6. Robustness to fabrication

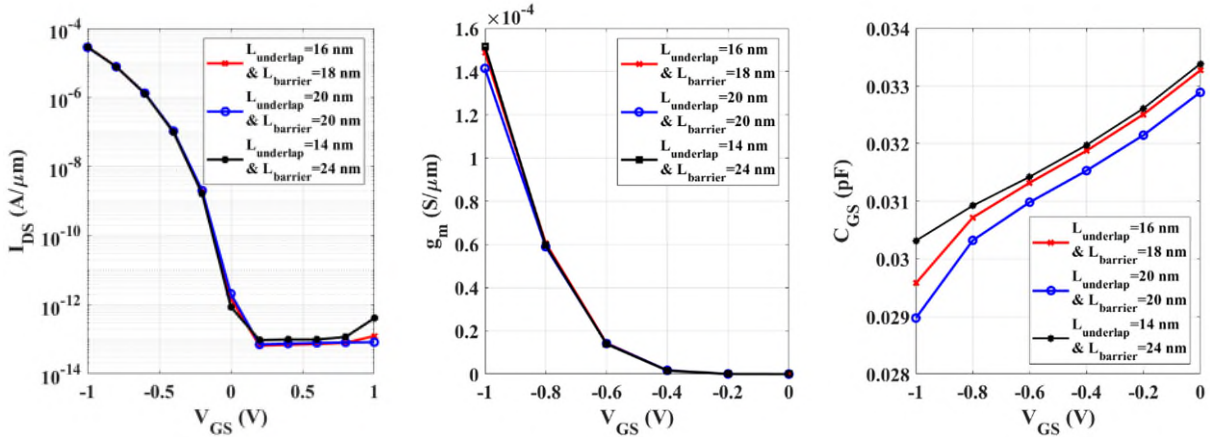
To assess tolerance to realistic process variations, we benchmark three co-optimized corners: A) $L_{\mathrm{underlap}} = 16$ nm and $L_{barrier} = 18$ nm; B) $L_{\mathrm{underlap}} = 20$ nm and $L_{barrier} = 20$ nm; and C) $L_{\mathrm{underlap}} = 14$ nm and $L_{barrier} = 24$ nm. Across these design points, the evolution of the transfer characteristic, transconductance, capacitance components, total gate capacitance, and cut-off frequency is smooth and monotonic, indicating that modest lithographic or etch-placement spreads at the drain side lead to gradual shifts in DC and RF behavior rather than abrupt failures (see Figure. 12).

Starting with the transfer characteristics, the ON branch at the operation bias $V_{\mathrm{GS}} = -1\ V$ is similar for all three case studies, confirming stable forward BTBT; differences appear primarily in the ambipolar branch at $V_{\mathrm{GS}} = +1$ V, where configuration C (shortest underlap) exhibits the largest reverse current, as shown in Figure 12a. This is consistent with stronger gate–drain coupling that tightens the drain-side field and partially re-opens a parasitic tunneling window. Configurations A and B (larger underlaps) relax the drain-side field and more effectively suppress the ambipolar conduction. By checking the transconductance at $V_{\mathrm{GS}} = -1$, the simulated g_m is essentially the same for configurations A and C, and both exceed B, as shown in Figure 12b. The longer underlap in B weakens gate leverage over the source-side tunneling junction, softening the modulation of the tunneling width with gate bias and thereby

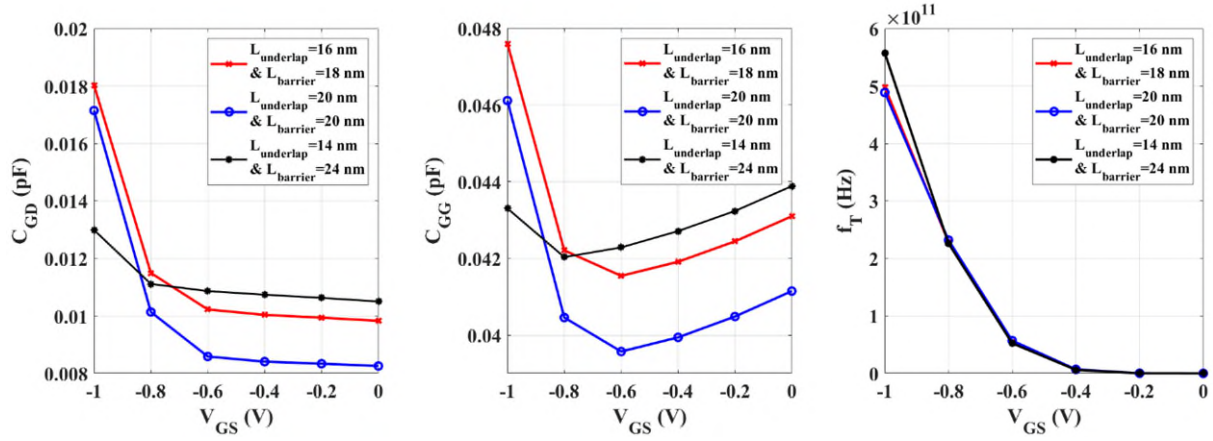
lowering g_m. In C, the long barrier would tend to reduce g_m via added tunneling resistance, but this is compensated by the short underlap that strengthens source-side control. Thus, the net result is $g_m(C) \approx g_m(A)$.

However, both the barrier length and the underlap length affect the gate capacitance. Configuration C shows the largest C_{GS} due to stronger gate control at the source junction with a short underlap; B has the smallest C_{GS} because the longer underlap weakens source-side coupling; A lies in between (see Figure 12c). At the same time, configuration C exhibits the lowest C_{GD} despite its short underlap, because the long barrier (24 nm) effectively depletes and decouples the drain-side segment from the gate fringe field, producing a pronounced Miller-capacitance reduction, as shown in Figure 12d. Configuration B also lowers C_{GD} via field relaxation from the longer underlap, while A shows the largest C_{GD} among the three. Considering the total gate capacitance $C_{GG} = C_{GS} + C_{GD}$, configuration C yields the lowest C_{GG}, while C_{GS} is relatively elevated due to the short underlap, the pronounced reduction in $C_{GD}$from the long barrier (24 nm) dominates, driving the total C_{GG} to its minimum. Configuration B achieves an intermediate C_{GG} because both C_{GS} and C_{GD} are reduced by the longer underlap, but not to the extent observed in C. Configuration A presents the largest C_{GG} among the three, owing to the combination of moderate C_{GS} and the largest C_{GD} as shown in Figure 12e.

Exploring the cut-off frequency, f_T, with $g_m(A) \approx g_m(C)$ and $C_{GG}(C)$ being the smallest (see Figure 12f), configuration C delivers the maximum f_T at the ON operating point $V_{GS} = -1$. Configuration B benefits from lowered capacitances but its reduced g_m limits f_T, whereas A ranks below C because of its larger C_{GG} reduces $\frac{g_m}{C_{GG}}$.



(a) (b) (c)



(d) (e) (f)

Figure 12. Comparative analysis of Ge-based NW-TFET performance for three selected cases: (a) I_{DS}, (b) g_m,(c) C_{GS}, (d) C_{GD}, (e) C_{GG}, and (f) f_T.

3.7. Non-Idealities effect

After considering the realistic process variations, the impact of oxide/semiconductor interface traps on the transfer characteristics is further investigated by sweeping the trap charge density. As the interface trap density increases, trap-assisted tunneling and the associated electrostatic perturbation shift the minimum-current point along the V_{GS} axis and raise the OFF-state floor. Physically, net interface charge modifies the flat-band/threshold condition, distorts the channel potential near the gate edge, and opens additional leakage paths. The result is a displacement of the minimum-current location and a broadening of the subthreshold region, as shown in Figure 13, with higher trap densities producing a larger shift and higher residual current at the valley.

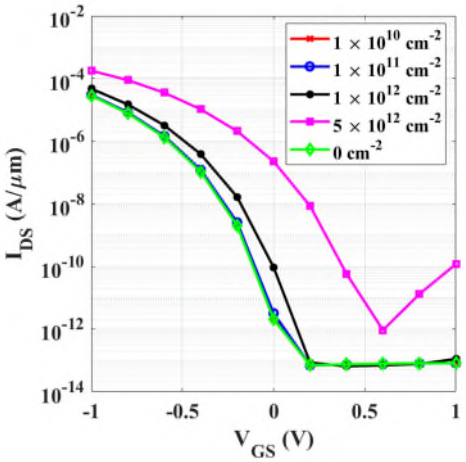
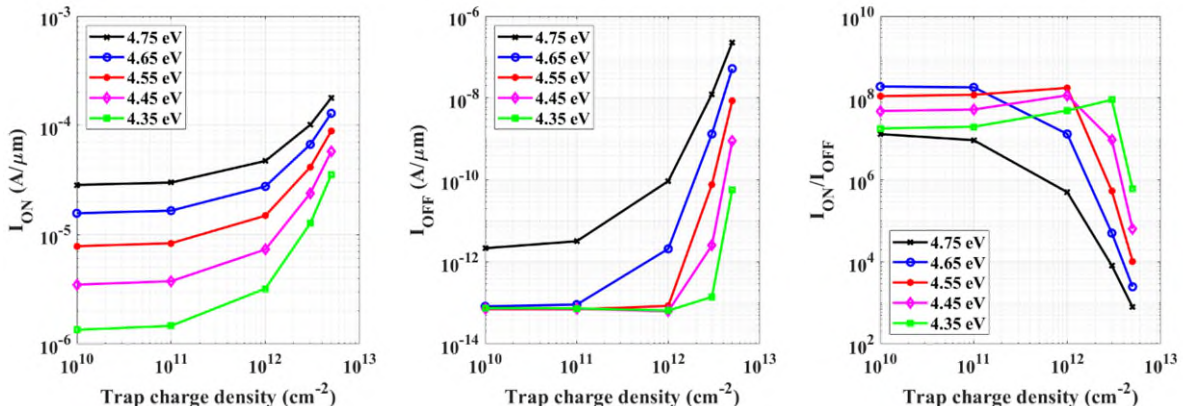


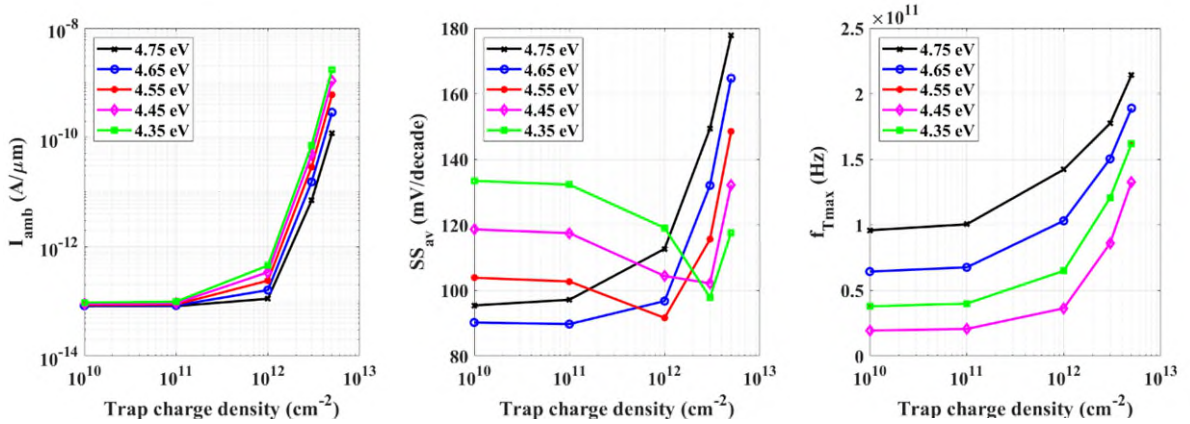
Figure 13. Impact of interface trap charge density on the I-V characteristics.

To counteract the trap-induced electrostatic shift, we tune the metal gate work function (WF) at $L_{\text{underlap}} = 20$ nm and $L_{barrier} = 20$ nm and study how traps and WF jointly affect the device key metrics. The results are summarized in Figure 14. Increasing the interface-trap density primarily perturbs the electrostatics and leakage paths, while WF retargeting re-centers the device and recovers performance across all key metrics at the relevant biases. Increasing the interface-trap density (D_{it}) raises the currents rather than keeping them constant. In Figure 14a, the ON current increases with D_{it} because trap-induced charge lowers the effective threshold and widens the source-side BTBT window, enhancing forward tunneling. In Figure 14b, the OFF current also increases mainly due to TAT. At WF = 4.55 eV counter-shifts the bands and suppresses I_{OFF}, notably yielding acceptable OFF leakage at $D_{\text{it}} \approx 10^{12}$ cm^{-2}. As a result, the ON/OFF ratio in Figure 14c improves under WF = 4.55 eV and $D_{\text{it}} \approx 10^{12}$ cm^{-2}, since I_{OFF} is pulled back more strongly than the modest rise in I_{ON}.

Figure 14d shows that the ambipolar current grows with traps as TAT re-opens drain-initiated tunneling windows. In Figure 14e, SS_{av} degrades with D_{it} because traps broaden the transition and pin the surface potential; by restoring the relative positions of V_{OFF} and V_T, WF = 4.55 eV steepens the slope and partially recovers SS_{av}. Finally, Figure 14f shows that $f_{T,\text{max}}$ recovers under WF = 4.55 eV at $D_{\text{it}} \approx 10^{12}$ cm^{-2}. Although traps tend to increase g_m (via larger I_{ON}) and can inflate $C_{GG} = C_{GS} + C_{GD}$, the WF re-centering preserves a favorable $\frac{g_m}{C_{GG}}$ ratio, so RF speed remains robust at $V_{\text{DS}} = 1$ V.



(a) (b) (c)



(d) (e) (f)

Figure 14. Impact of the trap charge density on different metrics for different metal work functions: (a) I_{ON}, (b) I_{OFF}, (c) ON/OFF ration, (d) I_{amb}, (e) SS_{av} and (f) f_{Tmax}.

3.8. Proposed design vs. TFET architectures reported in literature

To quantify the benefit of the co-optimized drain underlap along with the SiGeSn barrier strategy in the proposed Ge-based GAA NW-TFET, Table 3 benchmarks our device against representative TFET architectures reported in the literature, spanning Si nanowire TFETs, strained SiGe heterojunction TFETs, nanotube/junctionless concepts, and Ge-based vertical/doping-less heterojunction implementations. While an exact one-to-one comparison across different publications is inherently challenging because the reported devices differ in geometry, material systems, calibration level (experimental vs. simulated), biasing, and normalization, Table 3 still provides an informative order-of-magnitude view of how the proposed design sits within the current landscape of TFET performance tradeoffs.

As listed in Table 3, the proposed NW-TFET achieves $I_{\mathrm{ON}} = 1.49 \times 10^{-5}$ A/μm together with an ultra-low $I_{\mathrm{OFF}} = 8.44 \times 10^{-14}$ A/μm, yielding an ON/OFF ratio of 1.76×10^{8}. Importantly, the ambipolar current is strongly suppressed to $I_{\mathrm{amb}} = 2.4 \times 10^{-13}$A/μm, which directly reflects the intended design goal of closing the drain-initiated tunneling window. This leakage/ambipolar suppression is obtained while maintaining a high RF speed, with $f_{T,\mathrm{max}} = 6.4 \times 10^{10}$ Hz. These parameters are obtained after assuming that $D_{it} = 1 \times 10^{12}$ cm^{-2} and having a metal of WF = 4.55 eV, at $L_{underlap} = L_{barrier} = 20$ nm of $E_g = 0.92$ eV.

A key insight from Table 3 is that many TFETs reporting very aggressive drive or RF figures of merit often do so with a leakage/ambipolar penalty (or do not report ambipolarity explicitly). For example, some TFETs achieve very high I_{ON} and f_T, but their I_{OFF} and I_{amb} are orders of magnitude higher than the proposed device, illustrating a typical high-field/high-drive design

regime where drain-side parasitic tunneling is harder to suppress. Conversely, some ultra-low-leakage concepts (e.g., doping-less or strongly asymmetric junction approaches) can reach extremely small I_{OFF}, but may not simultaneously demonstrate strong RF operation (missing f_T) or may rely on more specialized structural features. In this sense, the co-optimization strategy provides a practical route to suppress ambipolarity without sacrificing the DC/RF operating envelope that is required for mixed-signal and high-speed low-power applications.

Table 3. Comparison of the principal DC and RF figures of merit of the proposed Ge-based NW-TFET with representative state-of-the-art TFETs reported in the literature.

Device Type & Reference	**I_{ON} (A/µm)**	**I_{OFF} (A/µm)**	**ON/OFF Ratio**	**I_{amb} (A/µm)**	**SS (mV/dec)**	**f_{Tmax} (Hz)**
Si NW-TFET [30]	~1×10^{-8}	~1×10^{-12}	~10^{3}	-	~240	~10^{8}
SiGe TFET (strained heterojunction) [31]	~1×10^{-5}	~1×10^{-11}	~10^{6}	-	~59	~10^{10}
Junctionless Si Nanotube TFET [32]	~6×10^{-6}	~1.5×10^{-12}	~4×10^{6}	1.14×10^{-14}	~55	~10^{10}
Vertical FET with Ge/Si doping-less heterojunction [33]	~3×10^{-5}	~4×10^{-13}	~7×10^{7}	-	~52	~10^{11}
Germanium Source L-Shaped Gate Dopingless TFET [34]	~8×10^{-6}	~1×10^{-15}	~8×10^{9}	8.6×10^{-16}	~19	-
SiGe/Si TFET [35]	3.05×10^{-4}	6.37×10^{-11}	4.79×10^{6}	3.16×10^{-11}	64.5	3.55×10^{11}
Proposed NW-TFET (This Work)	1.49×10^{-5}	8.44×10^{-14}	1.76×10^{8}	2.4×10^{-13}	91.6	6.4×10^{10}

Future work can extend the proposed TFET architecture toward integrated high-speed and electro-optic systems. Building on the promising RF performance demonstrated here (cut-off frequencies in the 10^{10} Hz range), these TFETs could be coupled with silicon photonics or electro-optic modulators, such as high-frequency monolithic silicon-on-silica modulators [36], to enable mixed-signal and optical-interconnect functions. Beyond high-speed links, TFETs are also attractive for sensing, including ultrasensitive low-power biosensors and enhanced temperature sensors enabled by band-to-band tunneling and engineered source structures. Realizing a unified electro-optic-sensing platform will require co-optimizing device electrostatics, sensing surface interactions, and optical confinement. Such integration could deliver ultra-low-power systems that combine high-speed signal processing, optical communication, and multifunctional sensing [37, 38]. Beyond sensing/photonic links,

integrating TFET front ends with emerging non-volatile memories, such as resistive-switching RRAM material platforms [39], could further enable ultra-low-power heterogeneous systems.

Conclusion

We demonstrated that ambipolar conduction in Ge NW-TFETs can be minimized most effectively by pairing a drain-side gate underlap with a Ge-matched SiGeSn barrier positioned directly beneath the underlapped region. Individually, underlap reduces gate–drain coupling (lowering C_{GD} and postponing reverse tunneling), while the barrier raises local band edges (widening the drain-side tunneling width). Together, they close the parasitic conduction window across bias and retain the forward BTBT path, yielding multi-order reductions in I_{amb} with minor impact on I_{ON}. For the proposed configuration (underlap = barrier = 20 nm), the device reaches an updated ambipolar current of 2.4×10^{-13} A/μm, maintains strong ON-state tunneling, and sustains high-frequency operation in the 10^{10} Hz class thanks to reduced Miller coupling. Sensitivity analyses across nearby length corners show smooth, monotonic shifts in transfer, g_m, and capacitances, indicating tolerance to practical lithographic placement at the drain. Under interface-trap perturbations, work-function retargeting recenters the electrostatics and recovers ON/OFF and f_T, demonstrating robustness of the co-optimized scheme. Overall, the results offer clear design guidance: (i) adopt moderate underlap to relax the drain field and lower C_{GD}, (ii) insert a Ge-matched SiGeSn barrier ($E_g \approx 0.92$ eV) under the underlapped segment, and (iii) apply WF retargeting to counter trap-induced shifts. Future work should experimentally validate SiGeSn barrier integration in vertical NW platforms.

Author Contributions

Mina Labib: Methodology, Software, Visualization, Validation, Investigation, Writing—original draft, Writing—review and editing; **Ahmed Shaker**: Conceptualization, Investigation, Validation, Software, Supervision, Writing—review and editing; **Michael Gad**: Conceptualization, Methodology, Investigation, Supervision, Writing—review and editing; **Yasmine Elogail**: Software, Validation, Visualization, Resources, Writing—original draft, Writing—review and editing

Funding

The authors declare that no funds, grants, or other support were received during the preparation of this manuscript.

Data availability

All data that support the findings of this study are included within the article.

Declarations

Competing interests

The authors declare that they have no competing interests.

References

[1] Sazalli, N.A.H., Kee, C.C., Osman, S.H., Goh, B.T., Ahmad, R., Jiwanti, P.K. and Wong, Y.H., 2025. Advances in ZrO2 gate dielectrics: materials, optimization strategies, and electronic applications. *Journal of Materials Science: Materials in Electronics*, *36*(20), p.1214.

[2] Krishnaraja, A., Svensson, J., Lind, E. and Wernersson, L.E., 2019. Reducing ambipolar off-state leakage currents in III-V vertical nanowire tunnel FETs using gate-drain underlap. *Applied Physics Letters*, *115*(14).

[3] Saeidi, A., Rosca, T., Memisevic, E., Stolichnov, I., Cavalieri, M., Wernersson, L.E. and Ionescu, A.M., 2020. Nanowire tunnel FET with simultaneously reduced subthermionic subthreshold swing and off-current due to negative capacitance and voltage pinning effects. *Nano letters*, *20*(5), pp.3255-3262.

[4] Dutt, A., Tiwari, S., Upadhyay, A.K., Mathew, R. and Beohar, A., 2022. Impact of drain underlap and high bandgap strip on cylindrical gate all around tunnel FET and its influence on analog/RF performance. *Silicon*, *14*(15), pp.9789-9796.

[5] Chen, S., An, Y., Wang, S. and Liu, H., 2025. A review of tunnel field-effect transistors: materials, structures, and applications. *Micromachines*, *16*(8), p.881.

[6] Abdi, D.B. and Kumar, M.J., 2014. Controlling ambipolar current in tunneling FETs using overlapping gate-on-drain. *IEEE Journal of the Electron Devices Society*, *2*(6), pp.187-190.

[7] Lin, Y.J., Liu, Y., Ting, T.T. and Shan, C., 2026. Design and Simulation of Reduced Ambipolar Effect for PNPN Tunnel Field-Effect Transistors Using Dual Cladding Layers. *physica status solidi (a)*, *223*(1), p.e202500862.

[8] Pandey, C.K., Dash, D. and Chaudhury, S., 2019. Approach to suppress ambipolar conduction in Tunnel FET using dielectric pocket. *Micro & Nano Letters*, *14*(1), pp.86-90.

[9] Panda, S., Jena, B. and Dash, S., 2022. Ambipolarity suppression of a double gate tunnel FET using high-k drain dielectric pocket. *ECS Journal of Solid State Science and Technology*, *11*(1), p.013014.

[10] Shaker, A., ElSabbagh, M. and El-Banna, M.M., 2019. Impact of nonuniform gate oxide shape on TFET performance: A reliability issue. *Physica E: Low-dimensional Systems and Nanostructures*, *106*, pp.346-351.

[11] Sahay, S. and Kumar, M.J., 2015. Controlling the drain side tunneling width to reduce ambipolar current in tunnel FETs using heterodielectric BOX. *IEEE transactions on electron devices*, *62*(11), pp.3882-3886.

[12] Eliwy, M., Elgamal, M., Shaker, A. and Fedawy, M., 2022. Impact of gate-on-drain overlap on the electrical characteristics of TFETs: Role of oxide material and drain spacer. *Pramana*, *96*(2), p.93.

[13] Kumar, K., Kumar, A., Kumar, V., Jain, A. and Sharma, S.C., 2023. Ambipolarity suppression of band gap and gate dielectric engineered novel $Si_{0.2}Ge_{0.8}$/GaAs JLTFET using gate overlap technique. *Silicon*, *15*(18), pp.7837-7854.

[14] Spano, C.E., Mo, F., Claudino, R.A., Ardesi, Y., Ruo Roch, M., Piccinini, G. and Vacca, M., 2022. Tunnel Field-Effect Transistor: Impact of the Asymmetric and Symmetric Ambipolarity on Fault and Performance in Digital Circuits. *Journal of Low Power Electronics and Applications*, *12*(4), p.58.

[15] Kumar, A. Investigation of Vertical Cylindrical Gate-All-Around TFET for Low Power Dielectric Modulation-Based Biosensor. *Silicon* (2026). https://doi.org/10.1007/s12633-025-03631-x

[16] Kim, G., Lee, J., Kim, J.H. and Kim, S., 2019. High on-current Ge-channel heterojunction tunnel field-effect transistor using direct band-to-band tunneling. *Micromachines*, *10*(2), p.77.

[17] Li, C., Yan, Z.R., Zhuang, Y.Q., Zhao, X.L. and Guo, J.M., 2018. Ge/Si heterojunction L-shape tunnel field-effect transistors with hetero-gate-dielectric. *Chinese Physics B*, *27*(7), p.078502.

[18] Wiśniewski, P. and Majkusiak, B., 2020. Modeling the Current–Voltage Characteristics of $Ge_{1-x}Sn_x$ Electron–Hole Bilayer TFET With Various Compositions. *IEEE Transactions on Electron Devices*, *67*(7), pp.2738-2744.

[19] Wang, H., Han, G., Liu, Y., Hu, S., Zhang, C., Zhang, J. and Hao, Y., 2015. Theoretical investigation of performance enhancement in GeSn/SiGeSn type-II staggered heterojunction tunneling FET. *IEEE Transactions on Electron Devices*, *63*(1), pp.303-310.

[20] Narwal, S., Yadav, P., Saproo, D., Kumar, R., Chauhan, S.S. and Kumar, R., 2025. Advancements in Tunnel Field-Effect Transistors: Material Innovations, Emerging Applications and Future Perspectives. *Silicon*, *17*(12), pp.2729-2770.

[21] Liu, M., Junk, Y., Han, Y., Yang, D., Bae, J.H., Frauenrath, M., Hartmann, J.M., Ikonic, Z., Bärwolf, F., Mai, A. and Grützmacher, D., 2023. Vertical GeSn nanowire MOSFETs for CMOS beyond silicon. *Communications Engineering*, *2*(1), p.7.

[22] Junk, Y., Frauenrath, M., Han, Y., Sun, J., Diaz, O.C., Bae, J.H., Hartmann, J.M., Grützmacher, D., Buca, D. and Zhao, Q.T., 2023, April. Vertical GeSn/SiGeSn GAA nanowire n-FETs with high electron mobility. In *2023 International VLSI Symposium on Technology, Systems and Applications (VLSI-TSA/VLSI-DAT)* (pp. 1-2). IEEE.

[23] Kaur, J., Verma, P., Sharma, A.K., Madan, J., Pandey, R. and Basu, R., 2026. SiGeSn Alloy Solar Cells: Noise, Recombination, and Performance Insights. *Micro and Nanostructures*, p.208568.

[24] Sant, S. and Schenk, A., 2015. Band-offset engineering for GeSn-SiGeSn hetero tunnel FETs and the role of strain. *IEEE Journal of the Electron Devices Society*, *3*(3), pp.164-175.

[25] Zhu, Z., Xiao, J., Sun, H., Hu, Y., Cao, R., Wang, Y., Zhao, L. and Zhuang, J., 2015. Composition-dependent band gaps and indirect–direct band gap transitions of group-IV semiconductor alloys. *Physical Chemistry Chemical Physics*, *17*(33), pp.21605-21610.

[26] Kwatra, P., Singh, S.V. & Nigam, K. Design and Performance Analysis of New Metal Strip Incorporated Dual Oxide Dual Tunnel FET Evaluating Trap Charges for Augmented Reliability. *Silicon* **17**, 3897–3916 (2025). https://doi.org/10.1007/s12633-025-03453-x

[27] Fariha, R., Das, S., Nida, L.T. *et al.* Dual-Material Double-Gate Source-Pocket Tunnel Field Effect Transistor with Homogeneous Gate Dielectric: Computational Analysis of Structural and Material Parameters for Enhanced Performance. *Silicon* **18**, 87–105 (2026). https://doi.org/10.1007/s12633-025-03548-5

[28] Bordallo, C. C. M., Victor B. Sivieri, Joao Antonio Martino, Paula GD Agopian, Rita Rooyackers, Anne Vandooren, Eddy Simoen, Aaron Thean, and Cor Claeys. "Influence of the Ge amount at source on transistor efficiency of vertical gate all around TFET for different conduction regimes." In *2016 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS)*, pp. 242-245. IEEE, 2016.

[29] Elogail, Y., Fischer, I.A., Wendav, T. and Schulze, J., 2018. Enhancement of Ge-based p-channel vertical FET performance by channel engineering using planar doping and a Ge/$Si_xGe_{1-x-y}Sn_y$ heterostructure model for low power FET applications. *Semiconductor Science and Technology*, *33*(11), p.114001.

[30] Bordallo, C.C., Sivieri, V.B., Martino, J.A., Agopian, P.G., Rooyackers, R., Vandooren, A., Simoen, E., Thean, A.V.Y. and Claeys, C., 2016. Impact of the NW-TFET diameter on the efficiency and the intrinsic voltage gain from a conduction regime perspective. *IEEE Transactions on Electron Devices*, *63*(7), pp.2930-2935.

[31] Choudhury, S., Niranjan, N.K., Baishnab, K.L. and Guha, K., 2020. Design and simulation of P-TFET for improved I_{ON}/I_{OFF} ratio and subthreshold slope using strained $Si_{1-x}Ge_x$ channel heterojunction. *Microsystem Technologies*, *26*(6), pp.1777-1782.

[32] Rajendiran, P., Justeena, A.N., Mrabet, J., Ramasamy, S., Selvam, P.D. and Nirmal, D., 2024. Sensitivity analysis of junctionless silicon NT-TFET and performance metrics comparison with the silicon NT-TFET. *Journal of Nanoparticle Research*, *26*(6), p.129.

[33] Cherik, I.C., Mohammadi, S. and Maity, S.K., 2023. Vertical tunneling FET with Ge/Si doping-less heterojunction, a high-performance switch for digital applications. *Scientific Reports*, *13*(1), p.16757.

[34] Cherik, I.C. and Mohammadi, S., 2022. Design insights into switching performance of germanium source L-shaped gate dopingless TFET based on cladding layer concept. *IEEE Transactions on Electron Devices*, *70*(2), pp.801-805.

[35] Labib, M., Shaker, A., Gad, M. and Elogail, Y., 2026. Numerical Simulation Study and Design Optimization of High-Performance SiGe/Si Heterostructure Nanowire Tunnel FETs. *Silicon*, pp.1-18.

[36] Mahrous, H., Fedawy, M., El Sabbagh, M., Fikry, W. and Gad, M., 2020. A compact 120 GHz monolithic silicon-on-silica electro-optic modulator. *Optical and Quantum Electronics*, *52*(2), p.111.

[37] Gopal, G., Kumawat, M. and Varma, T., 2024. Recent advancement in TFET-based biosensor addressing technique and outcome: A review. *Biosensors: Developments, Challenges and Perspectives*, pp.119-145.

[38] Singh, P., Raman, A., Yadav, D.S., Kumar, N., Dixit, A. and Ansari, M.H.R., 2024. Ultra thin finger-like source region-based TFET: Temperature sensor. *IEEE Sensors Letters*, *8*(5), pp.1-4.

[39] Shin, W., Jang, S. and Kim, H., 2025. Recent Advances in Resistive Switching Memory Devices Based on Diverse Material Platforms for Next Generation Electronics. *Journal of Science: Advanced Materials and Devices*, p.100960.