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Yin Chen

yfchenyin@126.com

Putian University

Minxin Lin

Fuzhou University

Haibin Li

Fuzhou University

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A Novel Cascaded Quadratic High Step-up DC/DC Converter for Vehicle-mounted Photovoltaics

Yin Chen [1,2], Minxin Lin [2,*], Haibin Li [2,*]

[1] School of Computer and Data Science , Putian University, Putian 351100, China;yfchenyin@126.com(Y.C.)
[2] School of Electrical Engineering and Automation, Fuzhou University, Fuzhou 350116, China
* Correspondence: yfchenyin@126.com(Y.C.); seashore_li@126.com(H.L.);

ABSTRACT

This article describes a non-isolated high step-up DC-DC converter. This converter uses a quadratic structure, two coupled inductors (CIs) combined with a switched capacitor (SC), voltage multiplier cells (VMC), and two power switches. The proposed converter achieves a high voltage gain at a lower turns ratio and lower duty cycle than conventional quadratic converters. The presence of a common ground between the input energy source and the load is more favorable for closed-loop control, making the converter suitable for vehicle-mounted PV applications. In addition, the proposed converter has the advantages of low voltage stress on the semiconductor components (switches/diodes), more compactness, and high efficiency. This article illustrates the principle of operation and steady state analysis of the proposed converter, followed by a discussion of the generalized induction method for voltage gain, and theoretical efficiency analysis, and a performance comparison with other converters. Finally, a prototype is made with an output voltage of 400V according to the design criteria, and the experimental results verify the accuracy of the theoretical analysis.

***Index Terms*—Non-isolated, high-order, DC-DC converter, vehicle-mounted PV.**

I. INTRODUCTION

The automotive industry is facing significant challenges due to the depletion of fossil fuels, soaring oil prices, and high carbon emissions [1]. In this context, hybrid electric vehicles (HEVs) have emerged as the most viable alternative for minimizing greenhouse gas emissions and promoting sustainable development [2],[3]. HEV technology has gained popularity in the automotive sector due to its environmental benefits and reduced reliance on fossil fuels [4]. Recent research has shown growing interest in hybridizing fuel cells, photovoltaics (PV), and batteries for HEVs, with various topologies proposed in [5]. One practical solution involves using PV-generated electricity to power the electric motor for propulsion or to charge the battery. Currently, the mainstream voltage platform for electric vehicles is 400V, while some high-end models adopt an 800V system [6]. However, the constrained installation space on vehicles makes it impractical to connect PV modules in series for high-voltage applications. Consequently, low-power onboard PV systems are commonly integrated with the 400V vehicle voltage platform through a high-gain DC-DC converter, as depicted in Fig. 1.

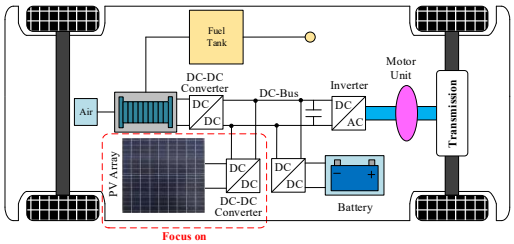


Fig. 1. Photovoltaic-based power systems for HEVs.

Although conventional boost converters are simple in structure and capable of achieving a certain boost effect, require a significant increase in duty cycle to achieve a high voltage gain. This leads to a significant increase in power consumption, which in turn reduces conversion efficiency [7]. To date, a variety of improved high-voltage gain DC-DC converter structures has been developed for generating high output dc voltages from low voltage sources. In these converters, varieties of techniques have been employed to improve the voltage conversion efficiency, including switched-inductor (SL), SC, cascade methods, segmentation techniques, VMCs, and combinations of these techniques [8]. The voltage-boosting capability of SL is limited, while SC can cause current surges [9], [10]. Cascaded boost units can increase the output voltage, but their potential impact on system stability must be considered [11]. The combination of CI techniques with other methods has attracted considerable attention, and appropriate voltage gain can be achieved by adjusting the suitable turns ratio [12]. However, in CI-based

topologies, active or passive clamping circuits are required to limit the high voltage spikes generated by leakage inductance across the power switches [13]. The combination of SC and SL is a commonly used technique in pursuit of achieving high voltage gain at low duty cycle conditions [14], [15]. A novel three winding CI high-boost quasi-Z-source DC-DC converter using a single core and voltage multiplier technology is proposed in Ref. [14]. However, quasi-Z-source based dc-dc converters not only have limited voltage gain and high voltage stress on the semiconductor, but also use more windings in their construction. Ref. [15] describes a converter incorporating both SC and CL techniques, utilizing a resonant circuit to absorb the energy from the leakage inductance and obtaining a high voltage gain at a low duty cycle. However, the voltage stress on some of the diodes is excessive in order to reduce the switching spikes and the voltage stress on the switch, which also leads to high current stress on the switch.

The quadratic structure is a very important technical route in the structure of DC-DC circuits, which is capable of producing high voltage gain with a small number of components. The voltage gain is an exponential function of the duty cycle, and smoother curve are more conducive to control. In recent years, many scholars have proposed various types of non-isolated quadratic converters with high voltage gain. A topology based on CI with high voltage gain and configured with subsidiary switches for soft switching is designed in Ref. [16]; the CI is replaced by a inductor and a in-built transformer, and active clamping is used to recover the leakage energy of the transformer while eliminating switching losses. Ref. [17] present a high boost DC-DC converter using multiple magnetic devices and switched-capacitor VMCs, along with CIs and built-in transformers, where the voltage gain can be flexibly increased with higher variability. A quadratic ultra-high voltage gain DC-DC converter based on CI has been proposed in Ref. [18], in which CI are combined with a quadratic circuit and a voltage doubling unit for increasing the boost gain. Ref. [19] illustrates an ultra-high boost DC-DC converter consisting of a stack of two boost stages, a CI and SCs. Ref. [20] introduces a CI and multiplier unit based on a cascaded quadratic type, where the secondary side of the CI is combined with the multiplier and the leakage inductance energy is recovered and transferred to the output. Ref. [21] builds a quadratic converter with a three-winding CI and a switch, however, the common ground is neglected in order to obtain high gain and results in high voltage stress. In the structure proposed in Ref. [22], an auxiliary circuit containing a CI and a VMC is integrated with the quadratic converter to obtain a higher voltage gain; where the two CIs are superimposed on the secondary side, and the auxiliary circuit is designed with an auxiliary switch with low voltage stress. However, this front-stage secondary type structure does not reduce the voltage stress on the main switch. A new high boost DC-DC converter with soft-switching capability is proposed in Ref. [23], where both the main and auxiliary switches are operated under soft-switching conditions, CIs and diode-capacitor VMCs are used in parallel to provide higher voltage gain. The unfortunate aspect of this topology is that with the high number of switches, the maximum diode voltage stress in the boost unit is high. Ref. [24] describes a new fully soft-switching ultra-high boost converter by integrating a secondary structure with auxiliary circuits consisting of CIs, SCs, and active clamping techniques. However, the three-winding coupled inductor is still slightly complex in terms of cost and process.

Based on the above discussion, this article proposes a novel quadratic high-boost DC-DC converter based on the combination of two CI and SCs. This converter uses two switches and incorporates a voltage clamp circuit along with the technique of VMC. By creatively combining the characteristics of quadratic, CI, and SC topologies, this converter effectively improves the voltage gain ratio at small turns ratios and low duty cycles. The main advantages of this structure are as follows:

1) High voltage gain and miniaturized design; the special SC+CI structure enables high voltage gain to be achieved at small turn ratios.

2) Reasonable duty cycle range and low loss; reasonable duty cycle range reduces conduction loss, and most semiconductor devices have achieved zero-voltage switching (ZVS) and zero-current switching (ZCS).

3) High efficiency and low voltage stress; A clamp circuit is used to effectively suppress voltage spikes on switches and absorb leakage inductance energy, while featuring low voltage stress, common ground design, and high efficiency.

This article is structured as follows: Section II outlines the operating principles of the proposed converter. Section III details the steady-state analysis and design guidelines. Section IV examines the efficiency analysis and performance comparison of the converter. Section V presents the experimental results from the laboratory prototype. Lastly, Section VI provides the conclusion.

II. Proposed Converter and Operation Principles

This section focuses on the derivation and operational principles of the proposed topology.

A. Converter Topology

The derivation of the proposed topology is shown in Fig. 2. The proposed topology is derived from the conventional quadratic structure combining two CIs, SC technology, and VMCs. Two inductors in the Two-switch quadratic circuit is coupled and modified, Switches S_1 and S_2 drive the primary side of the coupled inductors, respectively, and the secondary sides of the two coupled inductors are boosted in series. Considering the switch-off spikes caused by the leakage inductance and current size in the series boosting process of the coupled inductors, a voltage regulator diode D_2 and a buffer capacitor C_3 are designed. Finally a VMC is used to complete the rectifier boosting, it is clear that this part can be stacked to expand.

The proposed topology is further shown in Fig. 3. This topology consists of two power switches, six diodes (D_1, D_2, D_3, D_4, D_5, and D_0) and six capacitors (C_g, C_1, C_2, C_3, C_4, C_5, and C_0). These two coupled inductors are defined as ideal high frequency transformers with magnetizing inductors (L_{m1} and L_{m2}) and leakage inductors (L_{k1} and L_{k2}) The coupled inductors have primary windings (N_{11} and N_{21}) with N_1 turns, and their secondary windings (N_{12} and N_{22}) with N_2 turns. The turns ratio of the coupled inductors is equal to $n=N_2/N_1$.

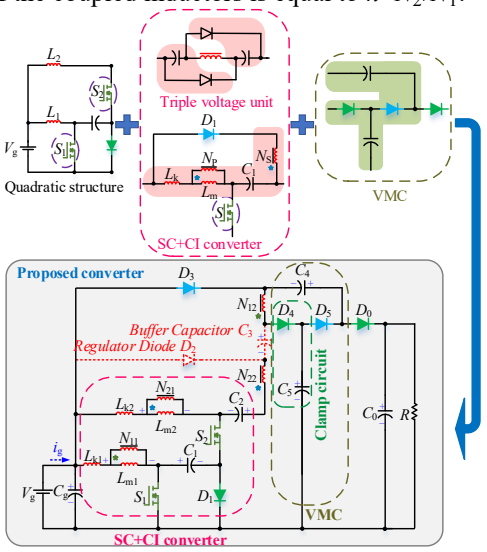


Fig. 2. Derivation of the proposed converter.

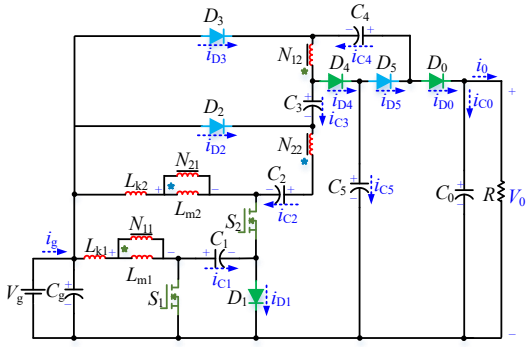


Fig. 3. Equivalent circuit with polarity definitions of voltage and current in the proposed converter.

B. Operating Principle of the Proposed Converter

To facilitate the circuit analysis, several simplifying assumptions are adopted: First, the capacitance value is sufficiently large to maintain a steady voltage across the capacitor throughout the switching period. Second, the input inductor is designed with adequate inductance to guarantee continuous current flow. Lastly, diodes are ideal devices, while the switch's parasitic capacitance is incorporated into the analysis. Despite these assumptions, the switching transitions of both the transistor and diode are instantaneous. The converter's operation during one complete switching cycle can be divided into eight modes, as shown in Fig. 4. Additionally, Fig. 5 presents the steady-state waveforms of the proposed converter.

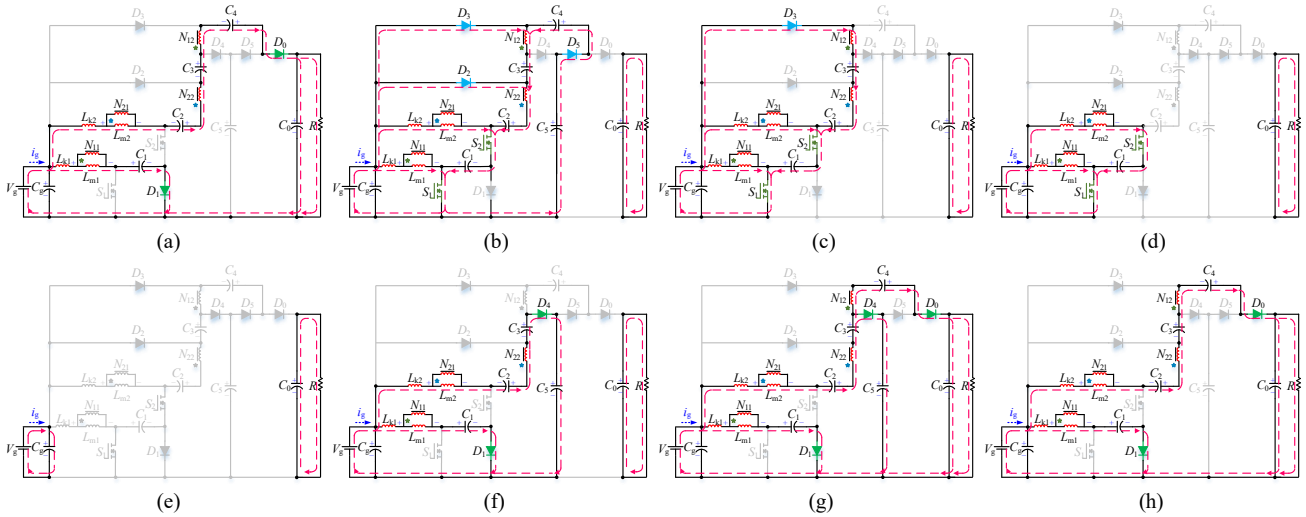


Fig. 4. Operating modes of the proposed converter. (a) Mode I. (b) Mode II. (c) Mode III. (d) Mode IV. (e) Mode V. (f) Mode VI. (g) Mode VII. (h) Mode VIII.

Mode I $[t_0, t_1]$: At the moment t_0, the driving signals for switches S_1 and S_2 have been issued, but due to the parasitic capacitance absorbing this energy, the switches S_1 and S_2 are not turned on in time, as shown in Fig. 4(a). At this time, the system continues to provide energy to C_0 and load R through N_{21}, C_2, N_{22}, C_3, N_{12}, and C_4 until the switches S_1 and S_2 are fully turned on to complete the mode switching. Obviously, the duration of this mode is very short and this time is completely affected by the parasitic capacitance of the switches.

Mode II $[t_1, t_2]$: In this mode, the switches S_1 and S_2 are turn on and the magnetizing inductances L_{m1} and L_{m2} start to accumulate energy and drive the secondary N_{12} and N_{22} to generate an induced current, as shown in Fig. 4(b). At this moment, both diodes D_3 and D_5 conduct, and diode D_2 supports the boost structure formed by N_{21}, C_2 and N_{22}; due to the high voltage on both sides of L_{m2}, the induced current formed by N_{22} is smaller than that of N_{12}, so D_2 mainly absorbs the current spikes of the system, and circulates very small currents and cuts off quickly. In this mode capacitor C_5 releases energy and transfers it to C_4, and power for load R is provided by C_0.

$$\begin{cases} i_{Lm1}(t) = i_{Lm1}(t_0) + \dfrac{V_g}{L_{m1} + L_{k1}} t, i_{Lm2}(t) = i_{Lm2}(t_0) + \dfrac{V_{Lm2}}{L_{m2} + L_{k2}} t \\ i_{N12}(t) = \dfrac{1}{n_1}\left(i_{Lm1}(t) - i_{Lk1}(t)\right), i_{N22}(t) = \dfrac{1}{n_2}\left(i_{Lm2}(t) - i_{Lk2}(t)\right) \end{cases} \tag{1}$$

Mode III $[t_2, t_3]$: At this moment, the energy in capacitor C_5 has been transferred to C_4, causing diode D_5 to cut off. Switches S_1 and S_2 continue to conduct, and the transformer second-side N_{12} and N_{22} continue to charge capacitors C_3 and C_2, respectively; diode D_3 continues to conduct, and as the charging of capacitors C_3 and C_2 is completed, the current in diode D_3 gradually decreases to zero, as shown in Fig. 4(c).

Mode IV $[t_3, t_4]$: During this time interval in Fig. 4(d), the current flowing in D_3 reduce to the diode's conduction threshold, and therefore diode D_3 cuts off. The secondary current of CIs in this mode is then zero, and the capacitor C_1 continues to release energy to maintain the magnetizing voltage of L_{m2} together with L_{m1}; the magnetizing currents of the primary magnetizing inductance L_{m1} and L_{m2} reach their maximum values in the final stage of this mode.

Mode V $[t_4, t_5]$: At the moment t_4, the switches S_1 and S_2 start to turn off, and at this time the diode D_1 has not yet conducted, and the whole system is in a stagnant state, as shown in Fig. 4(e). The load R energy is still provided by C_0. This modal time interval is very short and its effect can be neglected.

Mode VI $[t_5, t_6]$: As shown in Fig. 4(f), diode D_1 starts to conduct and the system charges C_5 through L_{m2}, C_2, N_{22} and C_3. At the beginning of this mode, the N_{12}, C_4, and D_0 currents are ignored due to the small induced current of N_{12}, which is unable to reach the on-current threshold of diode D_0. As the voltage of capacitor C_5 reaches its maximum value, the current of N_{12} will then increase into the next mode.

$$\begin{cases} i_{Lm1}(t) = i_{Lm1}(t_4) - \dfrac{V_{Lm1}}{L_{m1} + L_{k1}} t, i_{Lm2}(t) = i_{Lm2}(t_4) - \dfrac{V_{Lm2}}{L_{m2} + L_{k2}} t \\ i_{N12}(t) = \dfrac{1}{n_1}\left(i_{Lm1}(t) - i_{Lk1}(t)\right), i_{N22}(t) = i_{Lm2}(t) \end{cases} \tag{2}$$

Mode VII $[t_6, t_7]$: After entering this mode, as shown in Fig. 4(g), the current flowing through N_{12} gradually increases, capacitor C_4 releases energy and makes diode D_0 conductive, and the system begins to charge C_0; at this moment, the current through diode D_4 to charge C_5 gradually decreases.

Mode VIII [t_6, t_7]: At the moment t_6, capacitor C_5 finishes charging, diode D_4 cuts off, and the system supplies energy to the load R through N_{21}, C_2, N_{22}, C_3, N_{12}, and C_4 until the arrival of the switches S_1 and S_2 switching-off signals; the equivalent circuit of this mode is similar to that of the mode I as shown in Fig. 14(h).

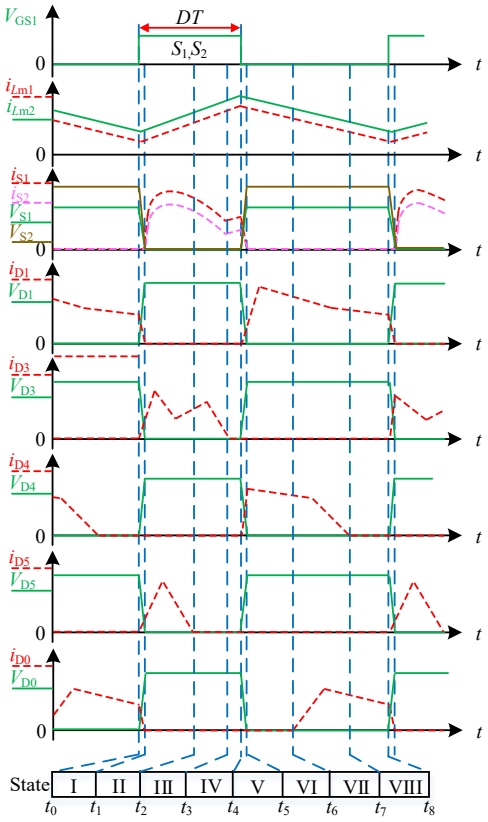


Fig. 5. Key waveforms of the proposed converter.

III. Steady-State Analysis and Design Considerations

This section details the steady-state analysis of the proposed converter topology. The analysis assumes magnetizing inductances (L_{m1} and L_{m2}) and leakage inductances (L_{k1} and L_{k2}), the coupling coefficients (k_1 and k_2) of the two coupled inductors can be expressed as:

$$\begin{cases} k_1 = \dfrac{L_{m1}}{L_{m1}+L_{k1}}, k_2 = \dfrac{L_{m2}}{L_{m2}+L_{k2}} \end{cases} \tag{3}$$

A. Voltage Gain

In order to simplify the calculation and ignore the effects of mode I and mode V, the time from t_1 to t_4 is summarized as DT, and the time from t_5 to t_8 is collated as $(1\text{-}D)T$.

When S_1 and S_2 are turn on, from Kirchhoff's voltage law(KVL) the following equation can be obtained:

$$\begin{cases} -V_g + L_{m1}\dfrac{di_{Lm1}}{dt} + V_{C1} = 0, V_{C3} - k_1 n_1 L_{m1}\dfrac{di_{Lm1}}{dt} = 0 \\ L_{m1}\dfrac{di_{Lm1}}{dt} + V_{C1} - L_{m2}\dfrac{di_{Lm2}}{dt} = 0 \\ -L_{m2}\dfrac{di_{Lm2}}{dt} - k_2 n_2 L_{m2}\dfrac{di_{Lm2}}{dt} + V_{C2} = 0 \\ V_{C1} - V_{C2} + k_2 n_2 L_{m2}\dfrac{di_{Lm2}}{dt} - V_{C3} + k_1 n_1 L_{m1}\dfrac{di_{Lm1}}{dt} - V_{C4} + V_{C5} = 0 \end{cases} \tag{4}$$

where V_{C1}, V_{C2}, V_{C3}, V_{C4}, and V_{C5} are the voltages of the corresponding capacitors.

During the (1-D)T time after S_1 and S_2 are turn off, the following equation can be written according to Kirchhoff's voltage law:

$$\begin{cases} -V_{\mathrm{g}} + L_{\mathrm{m1}} \dfrac{di_{Lm1}}{dt} + V_{\mathrm{C1}} = 0 \\ -V_{\mathrm{g}} + L_{\mathrm{m2}} \dfrac{di_{Lm2}}{dt} - V_{\mathrm{C2}} + k_2 n_2 L_{\mathrm{m2}} \dfrac{di_{Lm2}}{dt} - V_{\mathrm{C3}} + V_{\mathrm{C5}} = 0 \\ V_{\mathrm{g}} - L_{\mathrm{m2}} \dfrac{di_{Lm2}}{dt} + V_{\mathrm{C2}} - k_2 n_2 L_{\mathrm{m2}} \dfrac{di_{Lm2}}{dt} + V_{\mathrm{C3}} \cdots \\ -k_1 n_1 L_{\mathrm{m1}} \dfrac{di_{Lm1}}{dt} + V_{\mathrm{C4}} - V_{\mathrm{C0}} = 0 \end{cases} \tag{5}$$

In CCM mode, from the principle of volt-second balance for each inductor L_{m1} and L_{m2}, the following equations can be derived.

$$\int_0^{DT} V_{\mathrm{i,on}} dt + \int_{DT}^{T} V_{\mathrm{i,off}} dt = 0 \left(i = L_{\mathrm{m1}}, L_{\mathrm{m2}} \right) \tag{6}$$

Substituting (4) and (5) into (6), the output voltage can be expressed as:

$$V_{\mathrm{C0}} = \left[\frac{1 + (2-D)^2 + 2(2-D)k_2 n_2 + (2-D)(1-D)k_1 n_1}{(1-D)^2} \right] V_{\mathrm{g}} \tag{7}$$

The voltage gain of the proposed converter in CCM is obtained as follows:

$$G_{\mathrm{CCM}} = \frac{1 + (2-D)^2 + 2(2-D)k_2 n_2 + (2-D)(1-D)k_1 n_1}{(1-D)^2} \tag{8}$$

Assuming that the turns ratios n_1 and n_2 are equal and set to 1, the effect of k_1 and k_2 on the voltage gain under different duty cycle is plotted as shown in Fig. 6. As the duty cycle increases, the effect of the leakage coefficient on the voltage gain also increases; and it can be clearly seen that in the leakage coefficient of more than 0.9 in the case of the effect on the voltage gain is negligible, the ideal voltage gain equation can be obtained as follows.

$$G_{\mathrm{ideal,CCM}} = \frac{1 + (2-D)^2 + 2(2-D)n_2 + (2-D)(1-D)n_1}{(1-D)^2} \tag{9}$$

According to (8), the trend of voltage gain under different turns ratios is plotted as shown in Fig. 7. The results show that the effect of n_2 on the voltage gain is significantly larger than that of n_1. The difference between n_1 and n_2 is neglected and unified as n, as shown in Fig. 8. The voltage gain can be adjusted over a wide range by adjusting two parameters, including the duty cycle D and the turns ratio n of the winding CI. By designing the turns ratio of winding CI appropriately, excessive duty cycles can be avoided, thus greatly improving efficiency.

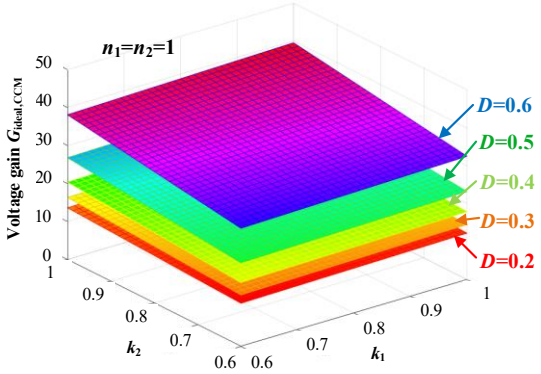


Fig. 6. Voltage gain versus coupled leakage coefficients k_1 and k_2.

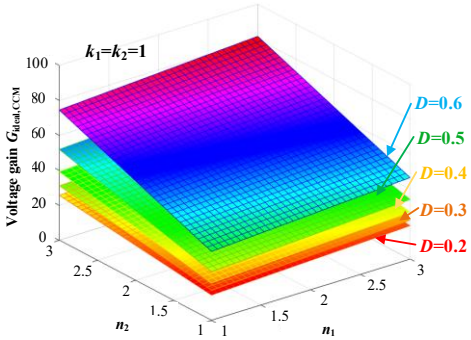


Fig. 7. Voltage gain versus turns ratios n_1 and n_2.

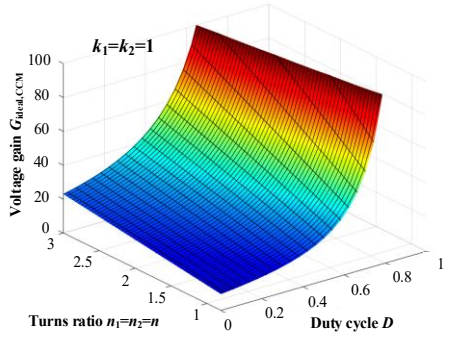


Fig. 8. Voltage gain versus duty cycle D and turns ratio n.

B. Stress Analysis of the Components

As mentioned before, the influence of the leakage coefficient is ignored to simplify the analysis. The voltage stresses of the switches and diodes can be represented as

$$V_{S1} = V_{D1} = \frac{1-D}{1+(2-D)^2+2(2-D)n_2+(2-D)(1-D)n_1} V_0 \tag{10}$$

$$V_{S2} = \frac{1}{1+(2-D)^2+2(2-D)n_2+(2-D)(1-D)n_1} V_0 \tag{11}$$

$$V_{D2} = \frac{(n_2+1)(2-D)}{1+(2-D)^2+2(2-D)n_2+(2-D)(1-D)n_1} V_0 \tag{12}$$

$$V_{D3} = V_{D0} = \frac{2-D+(1-D)n_1+(2-D)n_2}{1+(2-D)^2+2(2-D)n_2+(2-D)(1-D)n_1} V_0 \tag{13}$$

$$V_{D4} = \frac{(2-D)(D+n_2)}{1+(2-D)^2+2(2-D)n_2+(2-D)(1-D)n_1} V_0 \tag{14}$$

The maximum current through the switch is equal to the maximum current through the magnetized inductor. Kirchhoff's current law (KCL) also applies to the connection points of inductors, capacitors and diodes. Based on the KCL the individual semiconductor current stresses can be calculated as follows:

$$\begin{cases} I_{S1} = \dfrac{(2-D)\left[2+(1-D)n_1\right]+2Dn_2}{D(1-D)^2} I_0 \\ I_{S2} = \dfrac{2(2-D)+2Dn_2}{D(1-D)} I_0 \\ I_{D1} = \dfrac{2(Dn_2-D+2)}{(1-D)^2} I_0 \\ I_{D3} = I_{D5} = \dfrac{I_0}{D}, I_{D4} = \dfrac{I_0}{1-D} \end{cases} \tag{15}$$

C. Design Guideline

This section discusses design guidelines for key components of the proposed converter under CCM conditions.

1) Coupled inductor

Based on the current ripple characteristics of the magnetizing inductors L_{m1} and L_{m2} in CCM mode, the following constraints can be derived:

$$\Delta I_{Lm} \le 2I_{Lm} \tag{16}$$

The current ripple of the magnetizing inductance is:

$$\begin{cases} \Delta I_{Lm1} = \dfrac{V_{Lm1,on}D}{L_{m1}f_s} = \dfrac{V_g D}{L_{m1}f_s} \\ \Delta I_{Lm2} = \dfrac{V_{Lm2,on}D}{L_{m2}f_s} = \dfrac{V_g D(2-D)}{(1-D)L_{m2}f_s} \end{cases} \tag{17}$$

Using (16) and (17), the range of the magnetizing inductance can be derived as:

$$\begin{cases} L_{m1} \ge \dfrac{RD(1-D)^2}{2G_{ideal,CCM}\left[(1-D)n_1 + 2Dn_2 + 2(2-D)\right]f_s} \\ L_{m2} \ge \dfrac{RD(2-D)}{4G_{ideal,CCM}(1+n_2)f_s} \end{cases} \tag{18}$$

D. Capacitors

In order to keep the voltage ripple across the capacitors within an acceptable range, it is necessary to determine the minimum required capacitance. According to the charge balance principle $\Delta Q = C\Delta V_C = I_C\Delta T$, the capacitance of capacitors is derived as

$$C \ge \frac{DI_{C_on}}{r\%V_C f_s} \tag{19}$$

where I_{C_on} is the capacitor current, and r is the capacitor voltage ripple rate which usually is 2% of the capacitor voltage. Therefore, the suitable values of capacitors can be respectively chosen as

$$\begin{cases} C_1 \ge \dfrac{2(Dn_2 - D + 2)G_{ideal,CCM}}{r \cdot f_s \cdot R} \\ C_2 \ge \dfrac{2(1-D)G_{ideal,CCM}}{(2-D)(1+n_2)r \cdot f_s \cdot R}, C_3 \ge \dfrac{2G_{ideal,CCM}}{n_1 r \cdot f_s \cdot R} \\ C_4 \ge \dfrac{(1-D)^2 G_{ideal,CCM}}{\left[(2-D)(1+n_2) + (1-D)^2 n_1\right] r \cdot f_s \cdot R} \\ C_5 \ge \dfrac{(1-D)^2 G_{ideal,CCM}}{\left[2 - D + (1-D)^2 + (2-D)n_2 + (1-D)^2 n_1\right] r \cdot f_s \cdot R} \end{cases} \tag{20}$$

IV. Performance Analysis and Comparison

A. Theoretical Power Loss Analysis

In this section, the calculation of the losses associated with the components is presented. The total power losses in the proposed prototype include the energy dissipated by switches, diodes, windings, CIs and capacitors. The efficiency of the converter is affected by parasitic parameters. The parasitic parameters of components are listed in Table I.

Switching in a semiconductor device causes a change in the input voltage, and the change in the charge of the input capacitor affects the internal charge distribution in the device. This phenomenon is known as the Miller effect. As shown in Fig. 9, the Miller effect significantly affects the performance of a switching device by increasing the equivalent input and output capacitance of the switch, thereby reducing the bandwidth and operating speed. In addition, the Miller effect increases the input current of the switch, resulting in increased power consumption and heat dissipation. It is therefore essential to consider the Miller effect when calculating switching losses.

TABLE I
Drive and Component Parameters of The Prototype

Symbol	Value	Symbol	Value

MOSFET gate-to-source voltage, V_{GS}	15 V	Equivalent series resistance of C_g, r_{Cg}	136.79 mΩ
MOSFET gate threshold voltage, $V_{GS(th)}$	3 V	Equivalent series resistance of N_{21} and N_{22}, r_{N21} and r_{N22}	30.92/29.70 mΩ
MOSFET miller platform voltage, V_{GP}	6.3 V	Equivalent series resistance of N_{11} and N_{12}, r_{N11} and r_{N12}	42.62/40.28 mΩ
MOSFET drive turn-on resistance, R_{on}	10 Ω	Threshold voltage of $D_{2,3,4,5,0}$, $V_{FD2,3,4,5,0}$	1.07 V
MOSFET drive turn-off resistance, R_{off}	1 Ω	Threshold voltage of D_1, V_{FD1}	0.80V
MOSFET drive internal resistance, R_G	1 Ω	Forward resistance of $D_{2,3,4,5,0}$, $r_{D2,3,4,5,0}$	0.011 Ω
MOSFET input capacitance, G_{ISS}	10720 pF	Forward resistance of D_1, r_{D1}	0.0033Ω
MOSFET gate-to-drain (miller) charge, Q_{GD}	52 nC	Reverse recovery current of reverse diode $D_{2,3,4,5,0}$, $I_{rrD2,3,4,5,0}$	0.25 A
MOSFET static drain-to-source on-resistance, r_{DS}	0.008 Ω	Reverse recovery current of reverse diode D_1, I_{rrD1}	0.25 A
Forward voltage of reverse diode, V_{SD}	0.9 V	Reverse recovery time of reverse diode $D_{2,3,4,5,0}$, $t_{rrD2,3,4,5,0}$	50×10^{-9}s
Equivalent series resistance of $C_{1,2,3,4,5,0}$, $r_{C1,2,3,4,5,0}$	8 mΩ	Reverse recovery time of reverse diode D_1, t_{rrD1}	50×10^{-9}s

As shown in Fig. 9, V_{GS} is the output voltage of the PWM gate driver. The time t_B for the V_{GS} voltage to increase from $V_{GS(th)}$ to the Miller platform voltage V_{GP} is presented in (21). In the same way, t_F is the time for V_{GS} to decrease from the Miller platform voltage V_{GP} to $V_{GS(th)}$, as shown in (22).

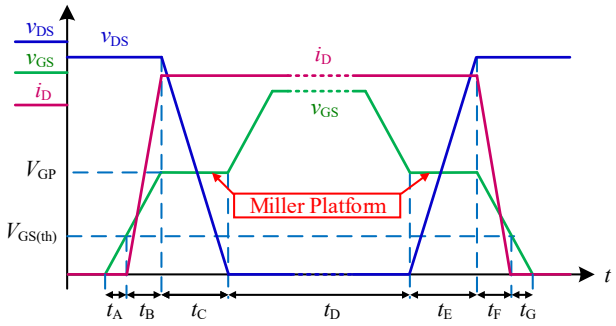


Fig. 9. Detailed process of the Miller platform.

$$\begin{aligned} t_B &= (R_G + R_{on}) \cdot C_{ISS} \cdot \left[\ln \frac{1}{1-\frac{V_{GP}}{V_{GS}}} - \ln \frac{1}{1-\frac{V_{GS(th)}}{V_{GS}}} \right] \\ &= (R_G + R_{on}) \cdot C_{ISS} \cdot \left[\ln \left(\frac{V_{GS} - V_{GS(th)}}{V_{GS} - V_{GP}} \right) \right] \\ &= 37.92\text{ns} \end{aligned} \tag{21}$$

$$\begin{aligned} t_F &= (R_G + R_{off}) \cdot C_{ISS} \cdot \left[\ln \frac{1}{1-\frac{V_{GP}}{V_{GS}}} - \ln \frac{1}{1-\frac{V_{GS(th)}}{V_{GS}}} \right] \\ &= (R_G + R_{off}) \cdot C_{ISS} \cdot \left[\ln \left(\frac{V_{GS} - V_{GS(th)}}{V_{GS} - V_{GP}} \right) \right] \\ &= 9.31\text{ns} \end{aligned} \tag{22}$$

The calculation of the maintenance time t_C and t_E is given as:

$$t_C = Q_{GD} \cdot \frac{R_G + R_{on}}{V_{GS} - V_{GP}} = 65.75\text{ns} \tag{23}$$

$$t_E = Q_{GD} \cdot \frac{R_G + R_{off}}{V_{GS} - V_{GP}} = 16.14\text{ns} \tag{24}$$

The switch power loss includes conduction loss and switching loss. The switching loss of single switch is expressed as:

$$\begin{aligned} P_{sw_S} &= \frac{1}{T}\left(\int_0^{t_r} V_S i_{Sr}\,dt + \int_0^{t_f} V_S i_{Sf}\,dt\right) = \frac{1}{2} f_s V_S (i_{Sr} t_r + i_{Sf} t_f) \\ &= \frac{1}{2} f_s V_S [i_{Sr}(t_B + t_C) + i_{Sf}(t_F + t_E)] \end{aligned} \tag{25}$$

where i_{Sr} and i_{Sf} are the switch rise and fall currents, respectively, and their values are the currents in mode II and IV, respectively. t_r and t_f are the rise and fall times of the switch.

The conduction loss of the switches is:

$$P_{cond_S} = \frac{1}{T}\int_0^T r_S i_S^2 \mathrm{dt} \ = r_S I_{S_RMS}^2 \tag{26}$$

where I_{S_RMS} is the current RMS value flowing through the switch.

Therefore, the switch power loss is given as:

$$\begin{aligned} P_{S_loss} &= \sum\left(P_{cond_S} + P_{sw_S}\right) \\ &= \frac{1}{2} f_s V_S [i_{Sr}(t_B + t_C) + i_{Sf}(t_F + t_E)] + r_S I_{S_RMS}^2 \end{aligned} \tag{27}$$

Diode power loss includes conduction loss and switching loss. Diode conduction loss

$$\begin{aligned} P_{cond_Di} &= \frac{1}{T}\int_0^T (V_{FDi} i_{Di} + r_{Di} i_{Di}^2)\mathrm{dt} \\ &= V_{FDi} I_{Di_ave} + r_{Di} I_{Di_RMS}^2 \ \ (i = 1,2,3,4,5,0) \end{aligned} \tag{28}$$

where V_{FDi} is the forward voltage drop, I_{Di_ave} and I_{Di_RMS} represent the current average and RMS value flowing through diode D_i.

Diode switching loss can be calculated as:

$$\begin{aligned} P_{sw_Di} &= \frac{1}{T}\int_0^{t_{rrDi}} P_{Di}(t)\mathrm{dt} \\ &= \frac{1}{2} f_s V_{Di} I_{rrDi} t_{rrDi} \ \ (i = 1,2,3,4,5,0) \end{aligned} \tag{29}$$

Where V_{Di} is the voltage stress of the diode, I_{rrDi} is the reverse recovery current, t_{rrDi} is the reverse recovery time.

There are eight diodes in this topology, and the total diode loss can be derived as:

$$\begin{aligned} P_{D_loss} &= \sum\left(P_{cond_Di} + P_{sw_Di}\right) \ \ (i = 1,2,3,4,5,0) \\ &= \sum\left(V_{FDi} I_{Di_ave} + r_{Di} I_{Di_RMS}^2 + \frac{1}{2} f_s V_{Di} I_{rrDi} t_{rrDi}\right) \end{aligned} \tag{30}$$

The power loss of capacitor can be determined as given below

$$\begin{aligned} P_{cond_Cj} &= \frac{1}{T}\left(\int_0^{DT} r_{Cj} i_{Cj_on}^2 dt + \int_{DT}^T r_{Cj} i_{Cj_off}^2 dt\right) \\ &= r_{Cj} I_{Cj_RMS}^2 \ \ \ (j = 1,2,3,4,5,0) \end{aligned} \tag{31}$$

where I_{Ci_RMS} is the current RMS value flowing capacitor C_j.

The total power loss of capacitors is obtained as

$$P_{C_loss} = \sum r_{Cj} I_{Cj_RMS}^2 \ \ (j = 1,2,3,4,5,0) \tag{32}$$

Losses related to high-frequency transformers and inductors are categorized as conduction losses and core losses. The conduction loss of the coupled inductors can be obtained as follows:

$$P_{CI_cond} = \sum_{i=1,j=1}^{2} r_{Nij} I_{Nij_RMS}^2 \ \ \ (i=1,2;j=1,2) \tag{33}$$

The hysteresis loss and the eddy current loss of the ferrite core are given by the Steinmetz equation in [25], as:

$$P_{core} = P_V V = F K f_s^{\alpha} B^{\beta} V \tag{34}$$

where P_V is the core loss power density; V is the core effective volume in the transformer; F is the flux waveform factor with a value of $\pi/4$, f_s is the switching frequency in the converter; and B is the flux density in the core; K, α and β are constants, for ferrite core materials, the values are 4.88×10^{-5}, 1.63 and 6.22, respectively.

In [26], the core flux density can be expressed by:

$$B = \frac{V_{N_on} D}{4 N A_e f_s} \tag{35}$$

where V_{N_on} is the voltage across the inductor when the switch turns on, and N is the number of turns.

Then, the loss of inductance can be summarized as:

$$P_{\mathrm{CI_loss}} = P_{\mathrm{CI_cond}} + P_{\mathrm{core}Lm} \tag{36}$$

There are two coupled inductors in this converter with four windings and six capacitors. The total losses of the proposed converter are expressed as:

$$P_{\mathrm{loss}} = P_{\mathrm{S_loss}} + P_{\mathrm{D_loss}} + P_{\mathrm{CI_loss}} + P_{\mathrm{C_loss}} \tag{37}$$

Thus, the conversion efficiency is calculated as:

$$\eta = \frac{P_0}{P_0 + P_{\mathrm{loss}}} \times 100\% \tag{38}$$

TABLE II
PARAMETERS OF THE EXPERIMENTAL PROTOTYPE

Parameter	Value	Parameter	Value
Input voltage	12-24V	Rated power	100W
Output voltage	400V	L_{m2} , L_{k2}	1.12mH, 1.04μH
L_{m1} , L_{k1}	466.96μH,0.70μH	n_1, n_2	1
MOSFETs	IRFP4668PbF	C_g , $C_{1,2,3,4,5,0}$	220μF, 5.6μF
D_1 , $D_{2,3,4,5,0}$	STTH6004CW STTH30R06W	Switch frequency	50 kHz

Some parameters of the converter in the experiment are presented in Table I and Table II, and substituted into (21)-(38). The efficiency is plotted against the output power as shown in Fig. 10. At low power, the theoretical efficiency increases rapidly with increasing output power. The theoretical efficiency reaches its maximum at an output power of 50W; at an output power of 100W, the theoretical efficiency is at its maximum at a duty cycle of 0.3. As the power increases, the losses also increase. Again, the trend of the theoretical efficiency curve remains constant for different duty cycle and gain conditions. The Fig. 11 reveals the theoretically efficient optimal duty cycle interval. Between a duty cycle D of 0.1 and 0.6, the theoretical efficiency is maintained at a high level; this interval narrows as the output power increases. The theoretical efficiency values are above 90% within a wide range of duty cycles. Hence, the proposed converter boasts the benefit of high efficiency.

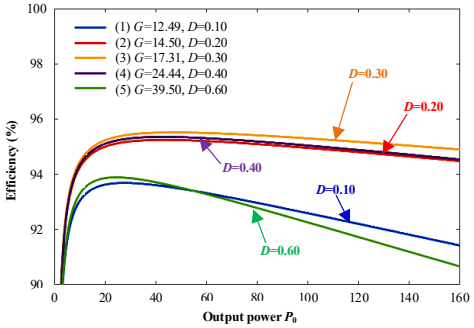


Fig. 10. Theoretical efficiency versus power output at different duty cycle D.

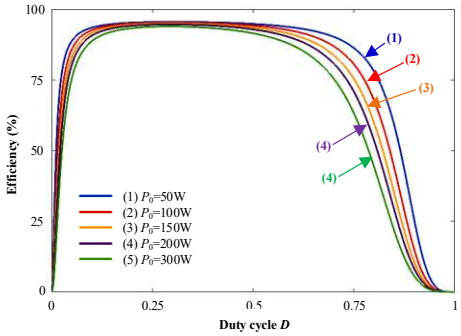


Fig. 11. Curve of theoretical efficiency at different output power P_0 with duty cycle D.

Based on the different output power, the percentage of loss of each device is calculated and plotted in Fig. 12. The power losses are mainly due to switches and diodes. However, as the power increases, the share of winding losses

and capacitor losses gradually increases.

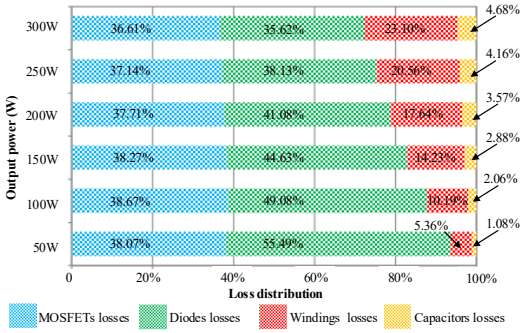


Fig. 12. Various loss ratios for different output powers. (D=0.30, f_s=50kHz).

B. Comparison With Other Converters

The quadratic high boost converter has been extensively studied by many scholars and various topologies have been proposed. In order to evaluate the advantages of the performance of the proposed topology, the topologies proposed in the recent years of references are compared. The comparison between the topologies and those presented in Ref. [18]-[26], as shown in Table III.

TABLE III
COMPARISON BETWEEN THE PROPOSED CONVERTER AND OTHER RELATED CONVERTERS

Converter	Number S/D/C/ W+L/T	Voltage gain	Maximum voltage stress on active switch	Maximum voltage stress on diodes	C.I.C.R	C.G
Ref. [18]	2/3/6/ 3+2/16	$\frac{D(n-1)+n+2}{1-D}$	$\frac{V_0}{D(n-1)+n+2}$	$\frac{nV_0}{D(n-1)+n+2}$	Yes	Yes
Ref. [19]	1/3/5/ 4+2/15	$\frac{n_2(n_1+1)(1+D)+2}{1-D}$	$\frac{V_0}{n_2(n_1+1)(1+D)+2}$	$\frac{[n_2(n_1+1)+1]V_0}{n_2(n_1+1)(1+D)+2}$	Yes	Yes
Ref. [20]	2/4/5/ 3+2/16	$\frac{3+2n-D(1+n)}{(1-D)^2}$	$\frac{V_0}{3+2n-D(1+n)}$	$\frac{[2+2n-D(1+n)]V_0}{3+2n-D(1+n)}$	Yes	Yes
Ref. [21]	2/5/6/ 3+2/18	$\frac{nD(1-D)+2n+2}{(1-D)^2}$	$\frac{V_0}{nD(1-D)+2n+2}$	$\frac{(1+2n-nD)V_0}{nD(1-D)+2n+2}$	Yes	Yes
Ref. [22]	2/5/6/ 3+2/18	$\frac{3+2n-D(3+n-D)}{(1-D)^2}$	$\frac{V_0}{3+2n-D(3+n-D)}$	$\frac{n(2-D)V_0}{3+2n-D(3+n-D)}$	Yes	Yes
Ref. [23]	1/6/6/ 3+1/17	$\frac{2+n_1+n_2+n_2D}{(1-D)^2}$	$\frac{V_0}{2+n_1+n_2+n_2D}$	$\frac{(1+n_1+n_2)V_0}{2+(n_1+n_2)+n_2D}$	Yes	No
Ref. [24]	2/2/6/ 5+3/18	$\frac{2+n_1+n_2}{(1-D)^2}$	$\frac{V_0}{2+n_1+n_2}$	$\frac{(1+n_1+n_2)V_0}{2+n_1+n_2}$	Yes	Yes
Ref. [25]	3/4/5/ 4+2/18	$\frac{(2-D)[n_1+n_2(1-D)]+(1-D)}{(1-D)^2}$	$\frac{V_0}{(2-D)[n_1+n_2(1-D)]+(1-D)}$	$\frac{[n_1+(1-D)n_2]V_0}{(2-D)[n_1+n_2(1-D)]+(1-D)}$	Yes	Yes
Ref. [26]	2/5/6/ 4+3/20	$\frac{3+2n_1(2-D)+n_2(1-D)-D}{(1-(1+n_2)D)(1-D)}$	$\frac{V_0}{3+2n_1(2-D)+n_2(1-D)-D}$	$\frac{(1+n_1+n_2)V_0}{3+2n_1(2-D)+n_2(1-D)-D}$	Yes	Yes
Proposed	2/6/7/ 4+2/21	$\frac{1+(2-D)^2+2(2-D)n_2+(2-D)(1-D)n_1}{(1-D)^2}$	$\frac{(1-D)V_0}{1+(2-D)^2+2(2-D)n_2+(2-D)(1-D)n_1}$	$\frac{[2-D+(1-D)n_1+(2-D)n_2]V_0}{1+(2-D)^2+2(2-D)n_2+(2-D)(1-D)n_1}$	Yes	Yes

Notes: S= Switch, **D**=Diode, **C**=Capacitor, **W**=Windings; **L**=Core, **T**=Total Device Count. **C.I.C.R**=Continuous Input Current Ripple, **C.G**=Common Ground.

For the fairness of the comparison, the turns ratio of the coupled inductor is normalized as n (n_1=n_2=n). It is evident in Fig. 13 that the voltage gains of the proposed converters are highly competitive over the full duty cycle interval; especially at low duty cycles, the gain advantage is significant. The voltage gains of Ref. [18] and Ref. [19] are not sensitive to the duty cycle, but the voltage gains increase sharply after the duty cycle D>0.6, which is obviously detrimental to the control system design. The maximum switch voltage stress for each type of topology is selected for comparison, as shown in Fig. 13(b).

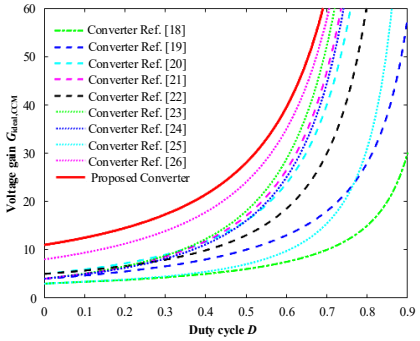


Fig. 13. Comparison with the converters when voltage gain G with n=1.0.

In Ref. [18]-[26], the switch voltage stress decreases with the increase of the turns ratio, and the maximum switch voltage stress of the proposed converter possesses an absolute advantage when the turns ratio n is small. Ref. [26] is second only to the proposed converter in terms of voltage gain and switch voltage stress. The voltage stress of the maximum diode is selected for comparison as shown in Fig. 14. The diode voltage stress of the proposed converter is at the mid-range level; however, with the gradual increase of the turns ratio n, after n>2.5, the diode voltage stress of the proposed converter is at the second dominant level, which is almost close to that of Ref. [26], which has the lowest diode voltage stress.

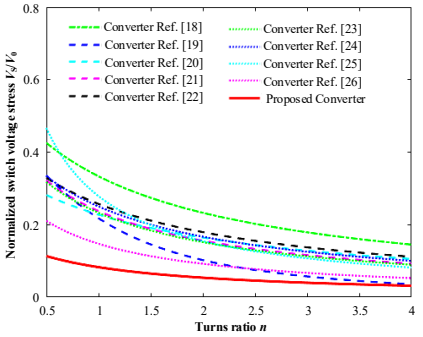


Fig. 14. Comparison with the converters when normalized switch voltage stress.

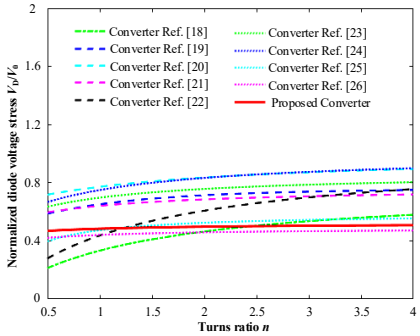


Fig. 15. Comparison with the converters when normalized diode voltage stress.

As evident from Table III, increasing the number of devices enhances the converter's performance. Therefore, the average individual device contribution to the voltage gain is plotted in Fig. 16. Although the number of proposed converters is high, the gain capability obtained with respect to a single device is still optimal in the duty cycle range between 0 and 0.7.

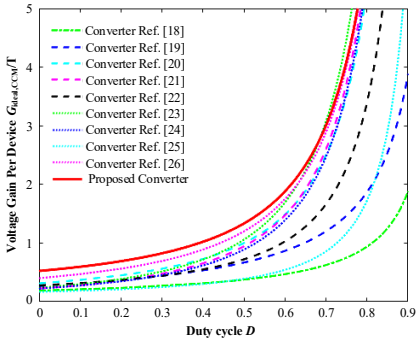


Fig. 16. Comparison with the converters when voltage gain per device *G*/T.

V. Experimental Verification

To evaluate the practicality of the suggested converter, tests are conducted on a laboratory prototype, as illustrated in Fig. 17. The parameters of the prototype converter are presented in Table II. The PWM gate pulses of the switches are generated by a DSP28335 with an appropriate dead time. The switching frequency and duty cycle are set to 50 kHz and 0.3, respectively. The captured experimental waveforms are illustrated in Fig. 18.

The experimental results are measured using a YOKOGAWA WT300E power analyzer. As shown in Fig. 18, at an output power of 100 W, the input voltage is 23.961V, the average input current is 4.64A, and the output voltage is 409.530V. The proposed converter has a voltage gain of 17.092, which is slightly lower than the theoretical value due to the parasitic parameters of the components. The collected data under different output power conditions indicate that the converter is highly efficient, with an output voltage of 409.530 V. In Fig. 18 (b) and (c), it can be clearly seen that the capacitors C_1 and C_2 maintain a stable voltage regardless of whether the switches are on or off and keep the voltage ripple low, which is the key to the connection between N_{11}, N_{21} and N_{22} of this converter. It can be seen that both switches S_1 and S_1 of this quadratic structure achieve ZVS turn-on. The voltage stresses on switches S_1 and S_2 are consistent with the calculations in Eq. 10 and the turn-off voltage spikes are at reasonable levels.

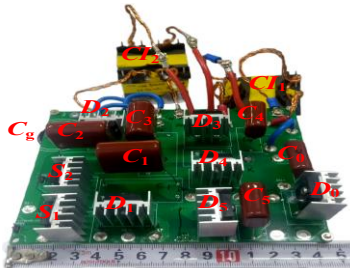
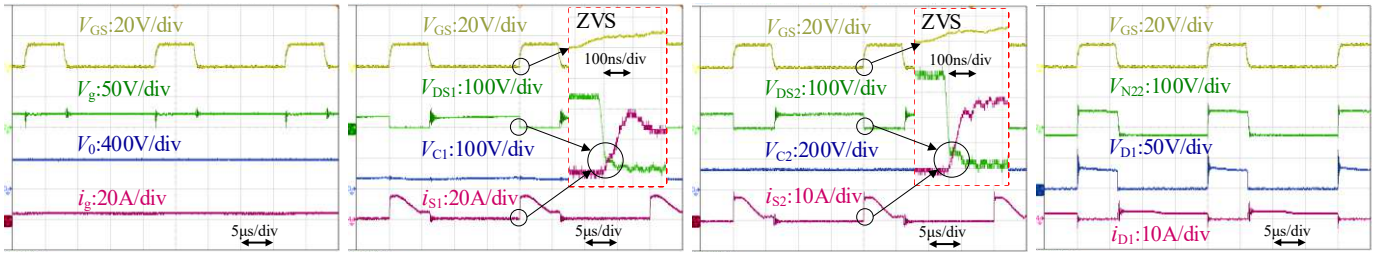


Fig. 17. Photograph of the proposed converter prototype.

Diodes D_1, and D_4 conduct at the same time, while diodes D_3 and D_5 conduct at the same time, as shown in Fig. 18(d), (e), (f) and (g). The current of diode D_1 is affected by the current of leakage inductor i_{Lk1}, making it difficult to achieve ZCS turn off. The diode D_4 can be turn off with zero current by fast charging and discharging of capacitor C_5. While during the test it is obvious that diodes D_3, and D_5 all obtain the effect of ZCS. After charging capacitor C_5, capacitor C_4 starts releasing energy to C_0, so the effect of ZVS turn-on of D_0 can be achieved. In Fig. 18, it is evident that the voltages stresses of diodes D_1, D_2, D_3, D_4, D_5, and D_0 are maintained at about 34V, 166V, 200V, 166V, 200V and 200V, respectively, which is consistent with the results calculated in Eq. (11)-(14). Experimental results demonstrate that the prototype complies with the design requirements and confirms the stability of the proposed topology.



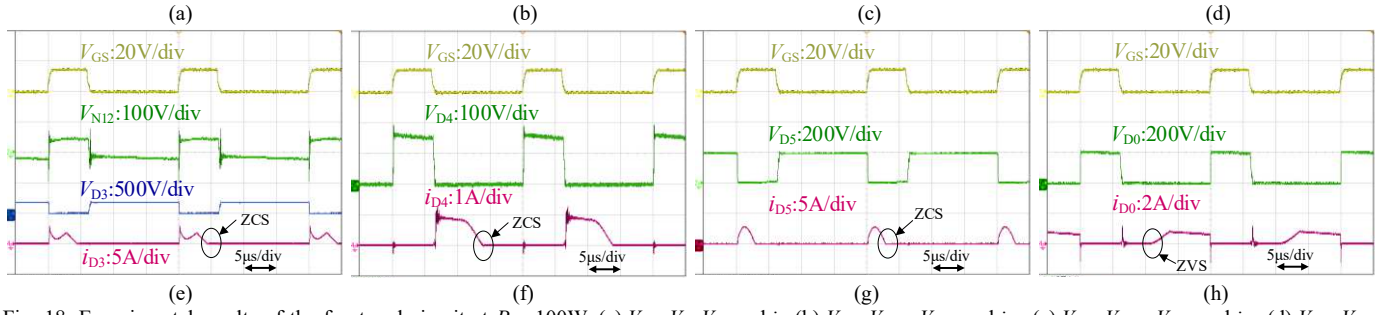


Fig. 18. Experimental results of the front-end circuit at P_0 =100W. (a) V_{GS}, V_g, V_0, and i_g. (b) V_{GS}, V_{DS1}, V_{C1}, and i_{S1}. (c) V_{GS}, V_{DS2}, V_{C2}, and i_{S2}. (d) V_{GS}, V_{N22}, V_{D1}, and i_{D1}. (e) V_{GS}, V_{N12}, V_{D3}, and i_{D3}. (f) V_{GS}, V_{D4}, and i_{D4}. (g) V_{GS}, V_{D5}, and i_{D5}. (h) V_{GS}, V_{D0}, and i_{D0}.

Fig. 19 compares the theoretical and measured efficiencies across different output power levels while maintaining a constant output voltage of 400 V. The difference between the two is mainly due to other parasitic parameters generated during the PCB manufacturing process as well as accuracy errors in the measurement equipment. As shown in Fig. 19, the efficiency of the converter shows a decreasing trend with the gradual increase of the output power. At an output power of 60 W, the measured maximum efficiency obtained is 95.288%; while at the rated load P_0=100 W; the efficiency is about 94.818%. In summary, the feasibility of the proposed converter and its advantages are successfully verified by the experimental results.

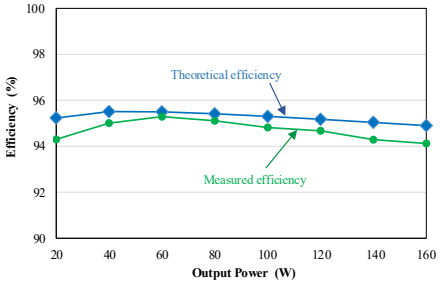


Fig. 19. Theoretical and measured efficiency curve.

VI. Conclusion

This article presents an innovative non-isolated high-boost DC-DC converter that combines a quadratic structure, SC, CIs and VMCs. Thanks to the special construction of SC+CI, the converter is able to achieve high voltage gain with a small turns ratio. The converter also has a reasonable duty cycle range, which reduces conduction loss and prevents saturation of the inductor with a small duty cycle. The clamping circuit is used to efficiently suppress voltage spikes on switches and to absorb leakage energy from the inductor. In addition, the overall compactness of the converter is improved due to less energy stored in the components. At the same time, the converter offers many advantages such as common ground design, low voltage stress on power switches and diodes, and high efficiency. In this paper, the theoretical efficiency of the converter is analyzed and discussed in detail. The paper also presents a comprehensive comparative analysis of the converter with other similar topologies that have been proposed recently. Finally, experimental tests on a 100 W prototype fully validate the excellent performance of the proposed converter. The results demonstrate its strong potential for application in hybrid electric vehicles (HEVs).

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Data availability

The datasets generated and/or analyzed during the current study are not publicly available but are available from the corresponding author on reasonable request.

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Competing interests

All authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest. The authors declare no conflicts of interest.