Supplementary information for

Reconfigurable Optical Arithmetic Logic Unit and Its Applications

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Supplementary Note 1: Basic principles of tuning state for microring modulator.

In the proposed device, microring modulators (MRMs) serve as fundamental components for executing various basic logic operations through the application of different electrical signals. As detailed in the manuscript, each microring modulator operates in two distinct states—pass/block and block/pass—enabling flexible signal routing and logic reconfiguration. The operational principles underlying these states are elaborated as follows. The add-drop configuration of the microring resonators produces complementary responses at different output ports. At the through port, the resonant characteristic appears as a transmission dip, exhibiting a spectral profile that initially decreases then increases with wavelength. As illustrated in Figure S1a, in pass/block mode, the application of a high-level voltage induces a red-shift in the resonant wavelength, leading to increased optical transmission intensity at the operating wavelength. Conversely, in block/pass mode (Figure S1b), the same voltage condition results in decreased transmission intensity.

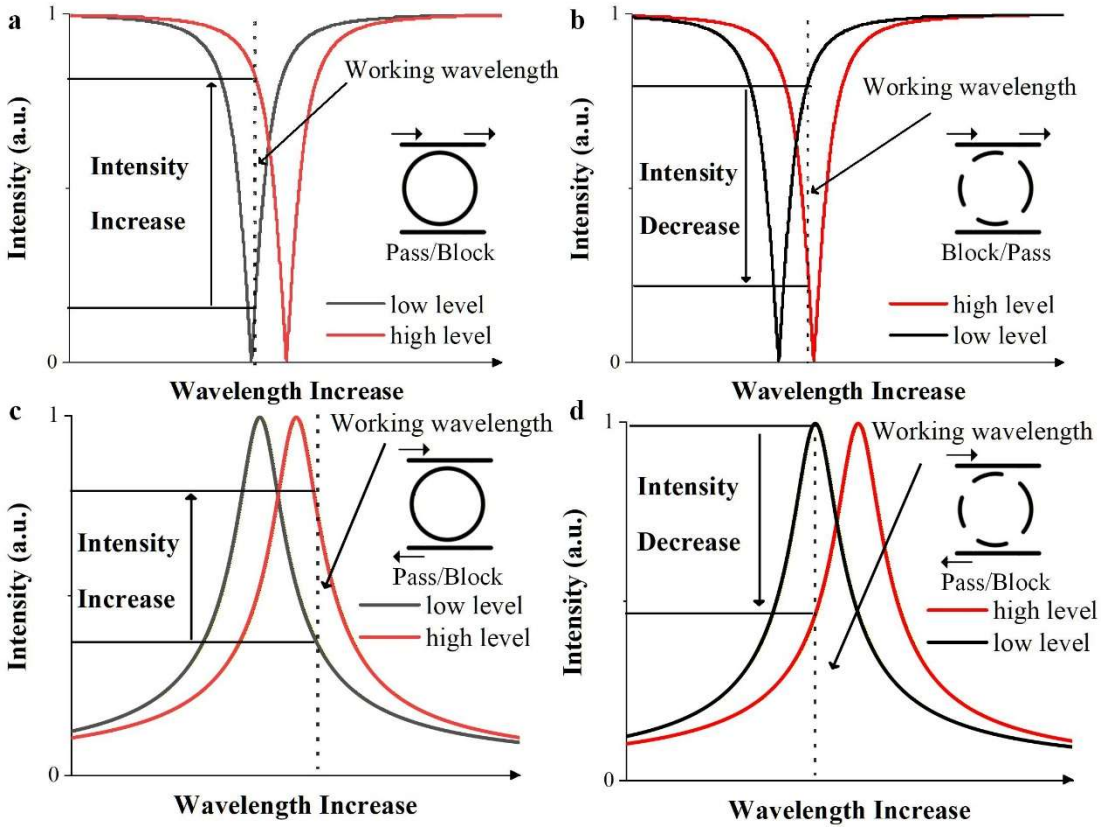

Figure S1 Different state at different port of MRM. **a** Pass/block at through port. **b** Block/pass at through port. **c** Pass/block at drop port. **d** Block/pass at drop port.

At the drop port, the resonant behaviour is inverted, manifesting as a transmission peak rather than a dip. Consequently, the voltage-dependent intensity variations at the drop port are opposite to those observed at the through port, as demonstrated in Figures S1b-c. This complementary response between the output ports forms the physical foundation for implementing reconfigurable logic functions, whereby assigning different operating wavelengths to individual microring resonators enables diverse logic outputs, while tuning facilitates switching between the two operational states of a single resonator.

Supplementary Note 2: Verifying the feasibility of AND operations in electric domains

Owing to the limited availability of a four-channel arbitrary waveform generator (AWG) during high-speed testing, the experimental characterization of basic logic operations was performed using a two-channel AWG configuration. To implement the required AND operations between different basic logic outputs, these logical combinations are subsequently processed in the electrical domain. To validate this methodological approach, we conducted comparative experiments using a four-channel AWG operating at lower speeds to physically generate the AND operations between various basic logic functions. The resulting waveforms were systematically compared with those obtained through electrical-domain AND processing of two-channel AWG measurements. This comparative analysis confirms the functional equivalence between direct multi-channel AWG generation and electrical-domain signal processing, thereby verifying the reliability of our experimental methodology for implementing combinational logic operations.

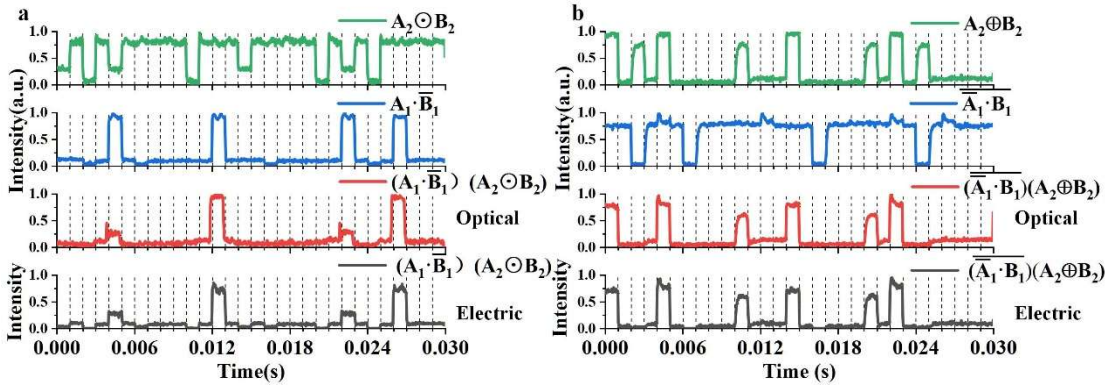

Figure S2 a The results of $(A_2 \odot B_2)$, $(A_1 \bullet \overline{B_1})$, $(A_2 \odot B_2)(A_1 \bullet \overline{B_1})$ which execute AND operation in optical domain, and $(A_2 \odot B_2)(A_1 \bullet \overline{B_1})$ which execute AND operation in electrical domain, respectively. **b** The results of $(A_2 \oplus B_2)$, $(\overline{\overline{A_1} \bullet B_1})$, $(A_2 \oplus B_2)(\overline{\overline{A_1} \bullet B_1})$ which execute AND operation in optical domain, and $(A_2 \oplus B_2)(\overline{\overline{A_1} \bullet B_1})$ which execute AND operation in electrical domain, respectively.

To validate the methodology, we examined the cases of $(A_2 \odot B_2)(A_1 \bullet \overline{B_1})$ and

$(A_2 \oplus B_2)(\overline{\overline{A_1} \bullet B_1})$ at 100 bit/s as representative examples. As shown in Figure S2a, the measured waveforms demonstrate: the green trace represents $(A_2 \odot B_2)$, the blue trace shows $(A_1 \bullet \overline{B_1})$, the red trace displays the result obtained by applying four different pseudorandom sequences to the thermal tuners to achieve AND operation in the optical domain, while the black trace corresponds to the electrical-domain AND operation performed on the two basic logic outputs. The close agreement between the black and red waveforms demonstrates that executing the AND operation in the electrical domain preserves signal integrity and produces equivalent results to the optical implementation. This conclusion is further supported by the additional comparative data presented in Figure S2b, which shows consistent behavior across different operational conditions and parameter variations. The comprehensive comparison confirms the viability of electrical-domain signal processing as a reliable alternative for implementing combinational logic operations in photonic computing systems, particularly when facing equipment limitations in experimental setups.

Supplementary Note 3: DSP description.

The raw waveform data acquired from the digital communications analyzer (DCA) cannot be directly interpreted as conventional digital signals composed of discrete 0 and 1 levels, necessitating additional processing for accurate signal reconstruction. To address this requirement, we developed a customized digital signal processing (DSP) algorithm that transforms the analog waveform measurements into standardized digital outputs. This comprehensive processing workflow comprises several key stages:

1. Locate the starting position of the data

The initial step in the digital signal processing workflow involves accurately locating the starting position of the data sequence within the captured waveform. Since the arbitrary waveform generator (AWG) outputs periodic signals while the digital communications analyzer (DCA) does not necessarily capture data beginning precisely at the signal's initiation point, synchronization between the ideal and measured waveforms becomes essential. This alignment is achieved through a cross-correlation-based method that compares the experimentally acquired waveform with the ideal computational reference. The algorithm identifies the position of the first deviating digital bit by detecting the initial mismatch between the measured and expected bit sequences. Subsequently, it calculates the precise starting offset by accounting for both the operating data rate and the specific bit position within the sequence, thereby establishing temporal alignment for all subsequent processing stages. This synchronization procedure ensures accurate interpretation of the logically encoded information within the optically measured signals.

2. Determine the rising and falling edges

The second processing stage involves detecting rising and falling edges in the captured analog waveforms for digital signal reconstruction. As the raw data from the digital communications analyzer (DCA) consists of discrete analog samples, conversion to digital signals requires precise edge detection. The developed algorithm employs a dynamic threshold detection mechanism that scans through predetermined amplitude ranges to identify potential transition points. Within each scanning window, the algorithm analyzes the power variation trend to classify edge types: when the optical

intensity demonstrates a consistent increasing trajectory exceeding the established threshold, it is registered as a rising edge; conversely, a sustained decreasing trend below the threshold is identified as a falling edge. This slope-based classification approach effectively discriminates between genuine signal transitions and noise-induced fluctuations, ensuring robust digital signal recovery even in the presence of waveform distortion and amplitude variations characteristic of optically measured data.

3. Assign a value to each bit

The third processing stage performs bit assignment based on the temporal segmentation of the synchronized waveform. Following the establishment of the starting position and total data length in the time domain, the algorithm partitions the continuous waveform into discrete bit intervals corresponding to the transmitted bit sequence. Each segment undergoes a dual-threshold evaluation process to determine its logical value. When a time segment is bounded by a rising edge at its beginning and a falling edge at its conclusion, it is categorically assigned as logic high (1). For more complex waveform patterns where edge transitions don't align perfectly with segment boundaries, the algorithm employs a duty-cycle-based decision metric, calculating the proportion of high-level duration within each bit interval. To ensure comprehensive coverage of possible waveform variations, the classification system incorporates over seventy distinct scenario patterns, accounting for various edge placement configurations, noise artifacts, and signal distortion cases. This sophisticated multi-criteria approach enables robust bit determination across diverse operating conditions and signal quality levels, effectively handling the non-ideal characteristics often present in optically acquired digital waveforms.

Supplementary Note 4: Power consumption analysis of the device.

This section presents a comprehensive analysis of power consumption in the proposed photonic computing architecture. Through implementation of state-of-the-art fabrication techniques, the microring modulator (MRM) achieves an exceptional power efficiency of 1.03 fJ/bit, with 0.79 fJ/bit allocated to dynamic modulation and 0.24 fJ/bit dedicated to thermal compensation. The architecture employs varying numbers of MRMs depending on the complexity of the implemented reconfigurable functions, with detailed power consumption specifications systematically documented in Supplementary Table 1 and corresponding schematic representations provided in Figure 1 of the main text.

Supplementary Table 1. Power consumption and other parameter of the device

Reconfigurable function	Number of MRMs	Frequency	Power consumption (per bit)	Power consumption (per second)	Note
Basic logical operation	2	20 GHz	2.06 fJ	0.0412 mW	/
		80 GHz	0.52 fJ	0.0103 mW	Potential
Adder	12	20 GHz	12.36 fJ	0.247 mW	/
		80 GHz	3.09 fJ	0.062 mW	Potential
Subtractor	12	20 GHz	12.36 fJ	0.247 mW	/
		80 GHz	3.09 fJ	0.062 mW	Potential
Comparator	6	20 GHz	6.18 fJ	0.123 mW	/
		80 GHz	1.55fJ	0.031 mW	Potential

Supplementary Note 5: The details of different amplification for image application.

While other demonstrated applications achieve 100% calculation accuracy with straightforward functional implementation, the differential amplification for image processing requires special consideration of its reconstruction principles. As a 2-bit subtractor, the output encompasses seven discrete decimal values ranging from -3 to +3. To transform these computational results into visual representations, multiple grayscale mapping schemes have been developed. For 7-bit grayscale reconstruction, we establish a direct linear mapping between the seven subtractor outputs (-3 to +3) and corresponding intensity levels. The 4-bit grayscale scheme employs the absolute values of the subtraction results, creating a one-to-one correspondence with reduced grayscale resolution. In the 3-bit implementation, grayscale assignment follows a ternary classification based on the result's sign: positive, zero, or negative values. The most compact 2-bit representation utilizes a binary classification that distinguishes between zero and non-zero outcomes, effectively replicating the functionality of an equality comparator. These graduated reconstruction techniques enable flexible trade-offs between image resolution and processing complexity, demonstrating the architecture's adaptability across various application requirements while maintaining mathematical consistency between computational outputs and their visual representations.

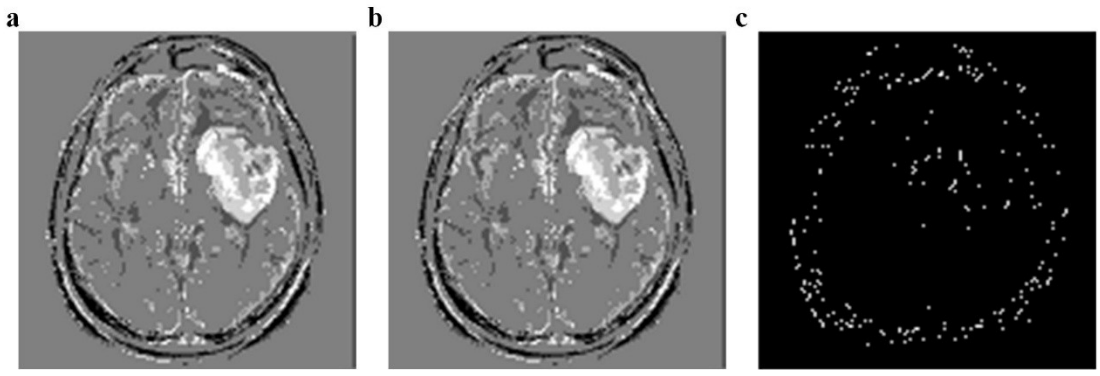

Figure S3 a 7-bit grayscale image of electric domain computation. **b** 7-bit grayscale image of optical domain computation. **c** the different results of the above images.

The differential amplification application achieves a calculation accuracy of 98.6% for 7-bit grayscale image reconstruction, representing the lowest accuracy among all

evaluated methods despite still demonstrating high operational reliability. A comparative analysis of the reconstructed images reveals three key results: the reference image generated through software simulation, the corresponding output produced by our photonic device, and a detailed difference map highlighting the discrepancies between them. The primary discrepancies are predominantly concentrated along the cranial boundaries, where edge enhancement effects amplify minor alignment variations, while the tumor region exhibits significantly lower displacement due to its structural homogeneity and consistent optical properties. This spatial distribution of errors confirms the system's stronger performance in processing continuous-tissue regions compared to high-contrast boundary transitions, providing insights for future optimization of biomedical image processing algorithms. The maintained accuracy across all functional implementations validates the architectural robustness for practical image processing applications.