Supplementary Information: A 3D-integrated BiCMOS-silicon photonics high-speed receiver realized using micro-transfer printing

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1 Transimpedance amplifier chiplet

The simplified schematic of the transimpedance amplifier (TIA) chiplet is shown in Fig. 1. The TIA input stage (TIS) utilizes a typical shunt feedback structure to convert the AC current signal of the PD into a voltage signal. Two electrostatic discharge (ESD) diodes, with a total of 51 fF parasitic capacitance, are placed at the input of the TIS to protect the internal circuits. Q_1 serves to alleviate the Miller effect of the parasitic base-collector capacitor of Q_0. A shunt inductor L_1, with 25×25 μm^2 area, is used to increase the phase margin of the TIA loop. The feedback resistor R_F, implemented as NMOS transistors and a polysilicon resistor, can be adapted by digital bits to compensate for the process variation. M_1 in the input DC current cancellation (IDCC) is used to absorb the DC current of the PD and the DC current of R_F. C_1 is used to compensate for the IDCC loop and alleviate the baseline wander. $R1 = 4k\Omega$, placed close to the base of Q_2, is used to prevent the parasitic capacitance of the IDCC from affecting the high-speed path. As $R_{Ref} = 6 \times R_{C0}$, the Q_0 collector current $I_{C,Q_0} \approx 6 \times I_{ref} = 5.4mA$, which impacts the overall bandwidth and input-referred noise current of the TIA. I_{ref} is designed to be tunable and controlled by digital registers. R_{Ref} and R_{C0} are placed close to each other in the layout for matching.

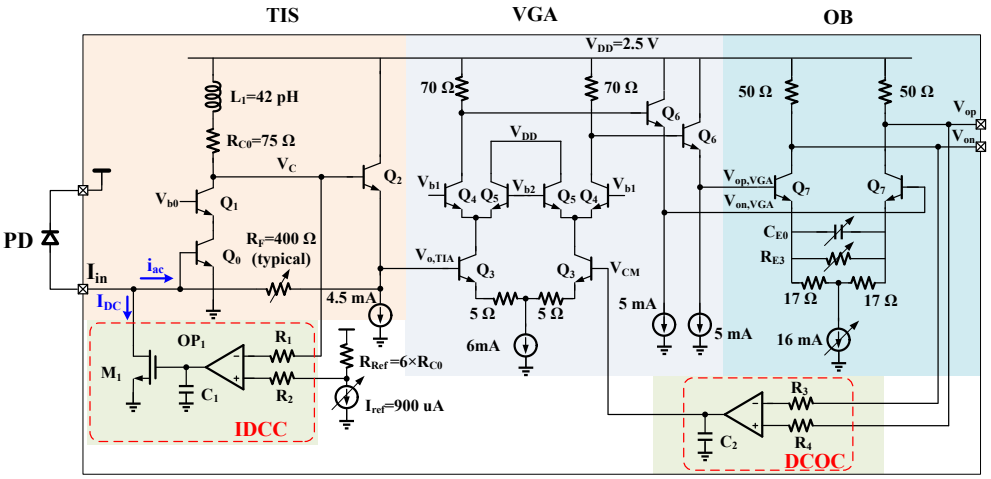

Fig. 1 Simplified schematic of the TIA chiplet.

The DC voltage at the input of the TIS is equal to one base-emitter forward bias voltage $V_{be,Q_0} \approx 0.75V$. The PD cathode bias voltage can be chosen to be the same as the main supply voltage of 2.5 V, so that the PD is reversely biased with a ∼1.75 V voltage difference.

The TIS is followed by the variable gain amplifier (VGA) stage, which also serves as a single-to-differential converter. One input of the VGA is connected to the output of the TIS, the other input is connected to a reference voltage generated by the DCOC. The gain of the VGA can be fine-tuned by changing V_{b1} and V_{b2} through digital bits.

Two 50 Ω resistors are used for impedance matching in the output buffer (OB) stage. The OB stage has a tunable CTLE, realized by a tunable capacitor C_{E0} and a tunable resistor R_{E3}. The R_{E3} is realized using NMOS transistors in the triode region, whose resistance is programmable by tuning their gate voltages. The C_{E0} is realized using PMOS varicaps, which can be fine-tuned by digital registers. The differential outputs of the OB are also protected by ESD diodes.

2 Comparison with current state-of-the-art optical receivers using different integrations

Table 1 shows the comparison with the state-of-the-art IMDD optical receivers using different integration methods. This μTP based optical receiver achieves the lowest power consumption of 0.51 pJ/b and the smallest EIC area of 0.06 mm^2.

Table 1 Comparison with current state-of-the-art PAM-4 optical receivers using different integrations.

ref.	Integration	EIC technology	Data rate (Gb/s)	R_T (dBΩ)	R (A/W)	Sens. @KP4 (dBm)	pJ/b	EIC Area (mm^2)	DSP
[1]	Wire-bonding (2D)	130nm BiCMOS	160	65	0.8	-7	0.99	0.82[1]	5-tap FFE
[2]	Wire-bonding (2D)	55nm BiCMOS	224	57.3	0.89	-4.8	2.2	1.38[1]	10-tap FFE
[3]	Flip-chip (3D)	N/A	160	N/A	0.85	-2.7	1.2	N/A	51-tap FFE
[4]	Flip-chip (3D)	16nm FinFET	106.25	77	N/A	-13.97	0.98	0.64	12-tap FFE + 1-tap DFE
[5]	Direct-bonding (3D)	130nm BiCMOS	264	60	0.9	N/A	1.45	0.6	6-tap FFE
[6]	Monolithic	45nm CMOS	112	68	0.245	N/A	1	N/A	N/A
This work	uTP (3D)	130nm BiCMOS	224	53.6	0.9	-5.2	0.51	0.06	6-tap FFE

[1] *data path core of one channel.*

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