Supplementary Information

Digital Twin Platform for Accelerating Optimization of Oxide Semiconductor Transistors to Overcome Fundamental Performance-Reliability Trade-off

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S1. Details of Digital Twin Platform

Fig. S1 gives an overview of the digital twin platform for across-the-stack co-optimization. In each iteration, the current dataset consisting of inputs (material, process & device parameters) and outputs (device-to-application characteristics) is used to train GP-based surrogate models to capture complex multi-scale input-output relationships. Multiple GP models are then combined to form a multi-objective function, which can be optimized using Bayesian active learning to determine the parameters for performing next optimum experiment and/or simulation. Using the predicted parameters, new experiments and simulations are performed and the dataset is updated for the next iteration. Over successive iterations, the platform converges to the most optimum material, process and device parameters that enables across-the-stack co-optimization.

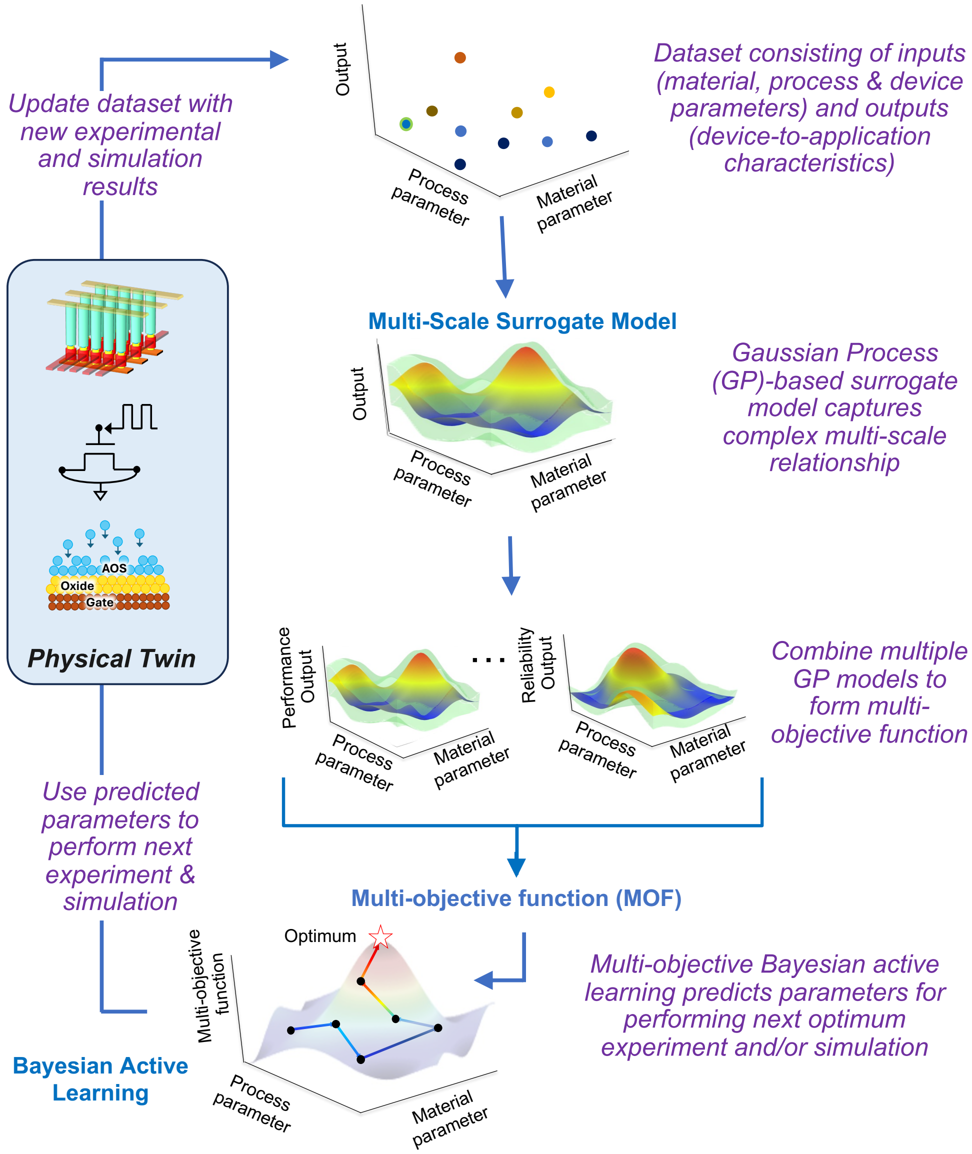


Fig. S1. Overview of the digital twin platform for across-the-stack co-optimization.

S2. AOS Transistor DC Characteristics for Single Objective Optimization

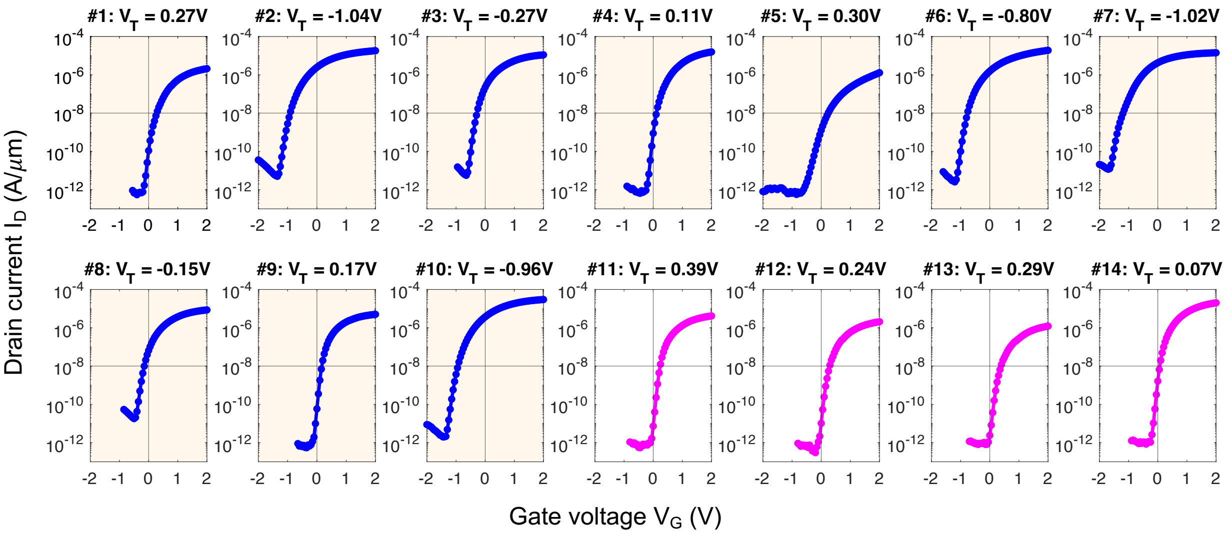


Fig. S2. Measured I_D-V_G characteristics of AOS transistors fabricated using single objective active learning. The threshold voltage (V_T) is extracted at ID=10-8 A/µm using constant current method. First 10 data points were used to train the GP model, and the last 4 were obtained using active learning.

S3. Trade-off Challenge During Performance Optimization

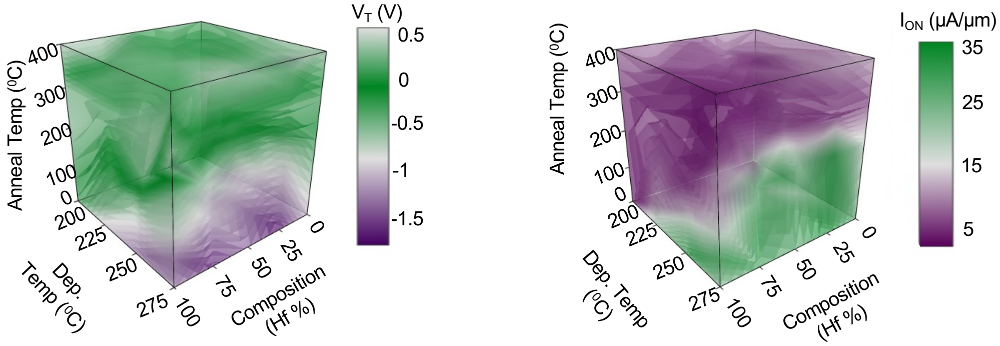


Fig. S3. Volumetric plots of the GP-model for extracted V_T and I_{ON} across all 80 combinations, illustrating different optimum regions for each and highlighting the challenge of simultaneous co-optimization.

S4. AOS Transistor DC Characteristics for Device Performance Optimization

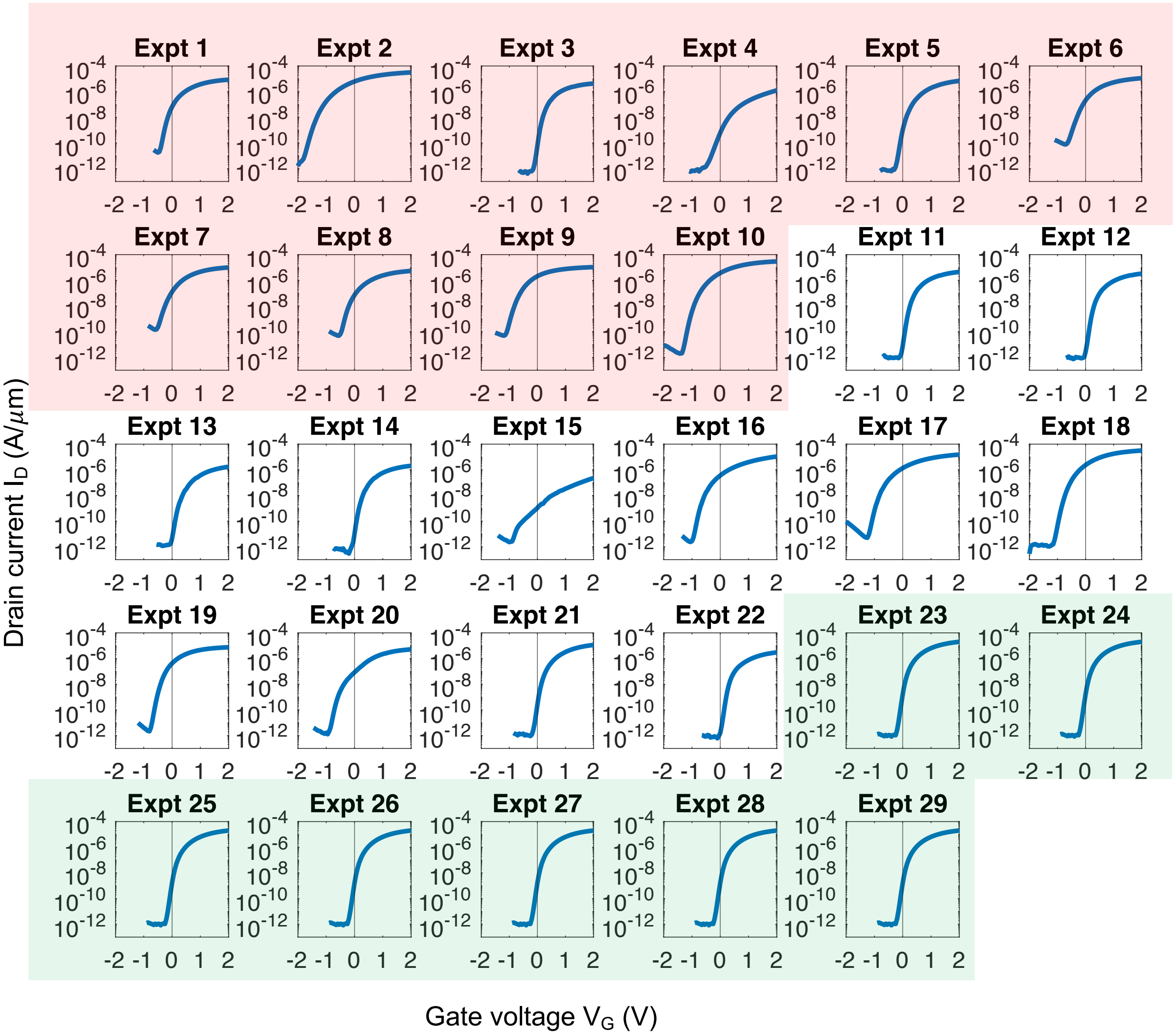


Fig. S4. Measured I_D-V_G characteristics of AOS transistors fabricated during device performance optimization using active learning. First 10 experiments in red shading were used to train the GP model. The model converges after 23 experiments which is shown in green shading.

S5. Transistor Characteristics for Multi Objective Performance and Reliability Co-Optimization

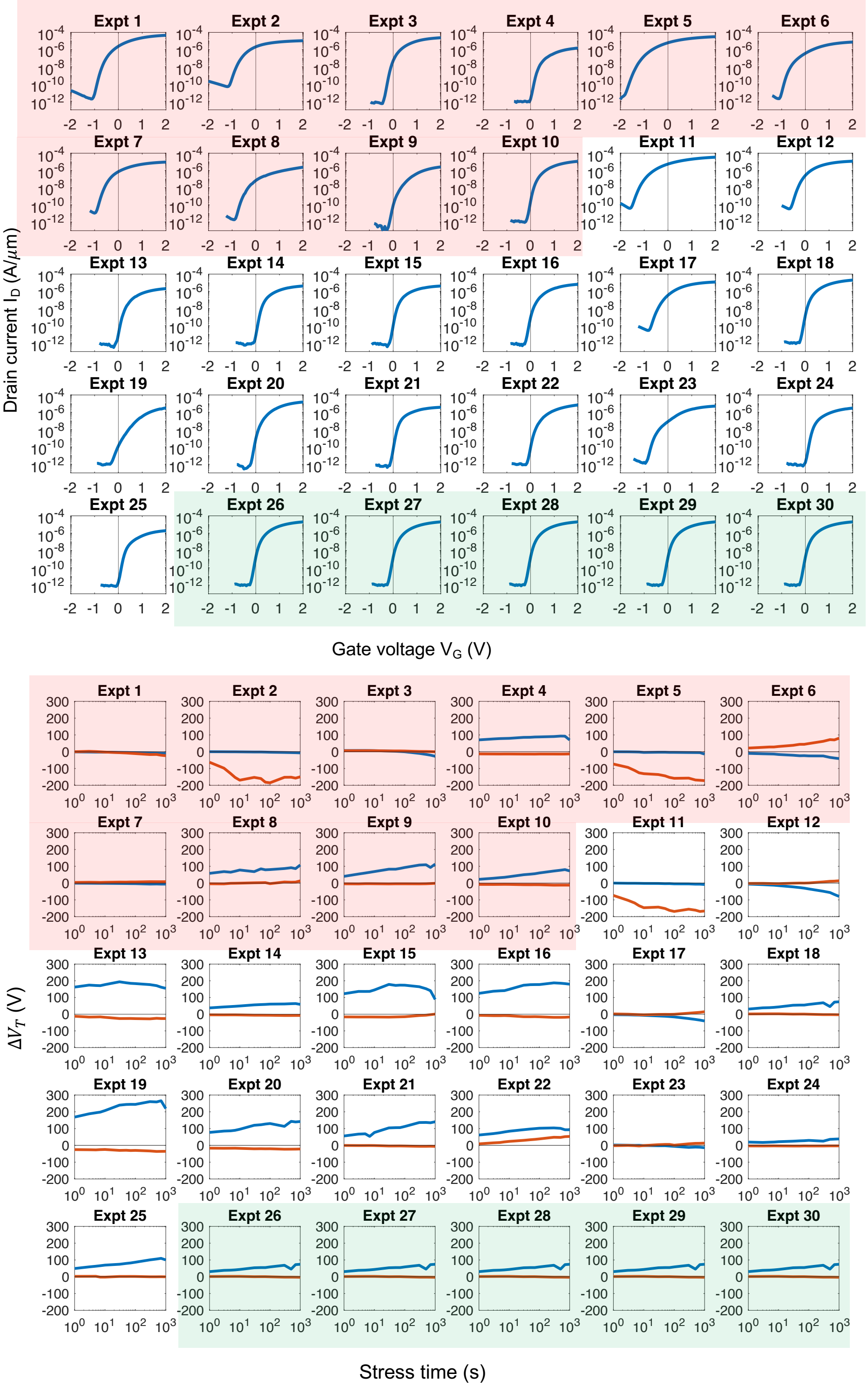
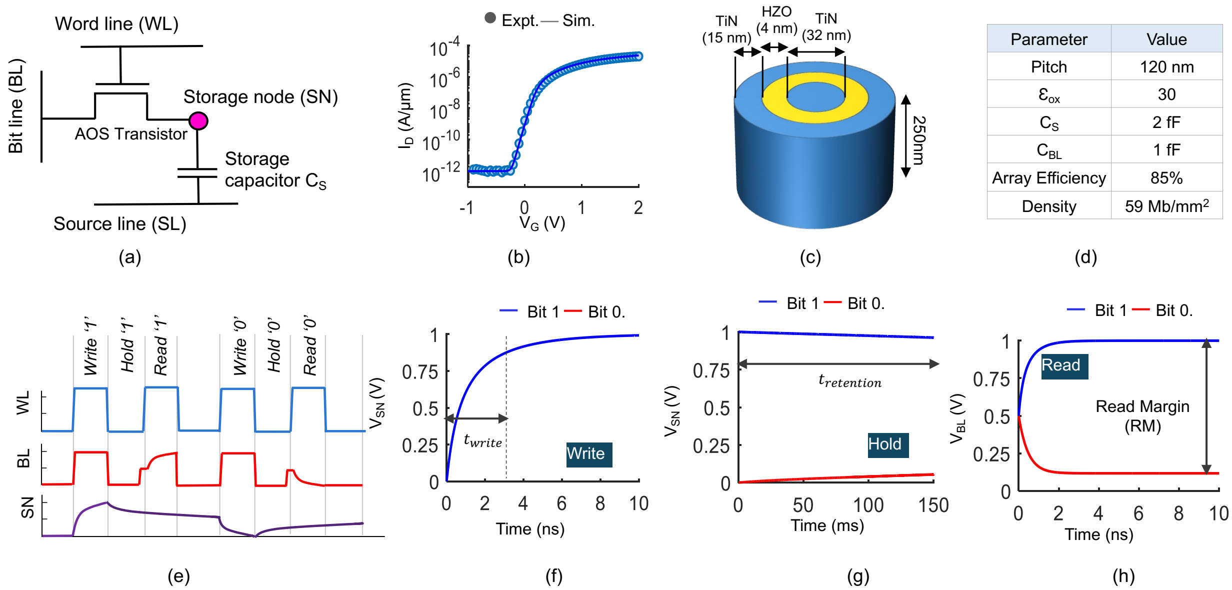


Fig. S5. Measured characteristics of AOS transistors fabricated using device performance and reliability co-optimization using active learning. First 10 experiments in red shading were used to train the GP model. The model converges after 26 experiments which is shown in green shading. The blue and red lines in reliability characteristics correspond to PBS and NBS, respectively.

S6. Details of 1T-1C DRAM Circuit Simulation

Fig. S6(a) shows an overview of the 1T-1C DRAM bit cell where the AOS transistor acts as the access transistor. We used an experimentally calibrated Virtual Source-based AOS transistor model as shown in Fig. S6(b) to simulate AOS-based DRAM circuit. For capacitor, we consider a circular trench capacitor shown in Fig. S6(c) with 15nm TiN bottom metal electrode, 4nm HZO as the dielectric with dielectric constant of 30 and an inner TiN metal filling of 32nm diameter. The capacitor height is considered to be 250nm, giving us a total storage capacitance of around 2fF. The total bit line capacitance (C_{BL}) is considered to be around 1 fF for a reasonable memory array size. Assuming a spacing of 50nm between the capacitors and thus pitch of 120nm, this can effectively enable a memory density of ~59 Mb/mm^2 with an assumed 85% array efficiency. The parameters are listed in Fig. S6(d).



Parameter	Value
Pitch	120 nm
ε_{ox}	30
C_S	2 fF
C_{BL}	1 fF
Array Efficiency	85%
Density	59 Mb/mm^2

(a) (b) (c) (d)

(e) (f) (g) (h)

Fig. S6. (a) Schematic of a 1T-1C DRAM cell. (b) Experimentally calibrated Virtual Source-based AOS transistor model. (c) Schematic of a cylindrical trench capacitor architecture, consisting of a TiN bottom electrode, a conformal HZO dielectric layer and an inner TiN top electrode. (d) The table summarizes the key geometric and array parameters used in the circuit simulations. (e) Voltage waveforms for BL, WL and SN during DRAM operation. Simulation results showing change in V_{SN} during (f) write, (g) hold and (h) read operation.

Next, we describe the operation of the 1T-1C memory bitcell. Fig. S6(e) shows the voltage waveforms for BL, WL and SN during DRAM operation. During write operation, the word line (WL) is kept high with a boosted voltage of 1.5V (i.e., V_{DD}+0.5V) to turn on the AOS access transistor. The bit line (BL) is toggled between 1V or 0V to charge or discharge the storage node (V_{SN}) to 1V or 0V for writing a bit '1' or bit '0'. The simulated transient voltage response of V_{SN} during write is shown in Fig. S6(f). We define the write time (t_{write}) as time to charge V_{SN} from 0V to 0.9V (i.e., 90% V_{DD}). During the hold operation, the WL and BL are kept low so that V_{SN} stores the written bit. However, owing to the leakage through the off AOS transistor, V_{SN} shows slow degradation as shown in Fig. S6(g). Retention time ($t_{retention}$) is defined as time during which V_{SN} can keep 100mV difference between stored bit '1' and '0' states, i.e., V_{SN}(bit 0) - V_{SN}(bit 1) = 100mV. After the hold operation and prior to reading the memory state, BL is pre-charged to V_{DD}/2. During read operation, WL is kept high and BL is charged to 1V or discharged to 0V depending on the stored bit in V_{SN} as shown in Fig. S6(h). Read margin (RM) is defined as BL readout voltage difference between bits '1' and '0', i.e., RM = V_{BL}(bit 0) – V_{BL}(bit 1). Note that for when the device performance becomes negative due to a negative V_T of the transistor, the leakage current becomes high. This in turn lowers RM and $t_{retention}$of the DRAM memory and can cause bit failure. We define bit error failure to occur when RM becomes lower than 200mV and difficult for a sense amplifier to distinguish between bits '1' and '0'.