Response to the Reviewers

We sincerely thank the Editor and the Reviewers for their thorough evaluation of our manuscript and for their insightful and constructive comments. All comments have been carefully considered and fully addressed, as detailed below.

Reviewer Comment:

"We strongly encourage all authors to share their raw data, either by providing it in a supplementary file or depositing it in a public repository and providing the details on how to access it in this section. If you do not wish to share your data, please clearly state this in this section along with a justification."

Response:

We thank the Reviewer for this important and constructive suggestion. In full compliance with the journal's data-sharing policy, we have now submitted supplementary material to the journal. The supplementary material includes two files entitled **"HSPICE 2008.03"** and **"The Electric VLSI Design System 9.07"**. It should be explicitly noted that these file names precisely correspond to and indicate the exact versions of the simulation and layout tools used in this study.

All data generated and analyzed during this study—including transimpedance gain, bandwidth, input-referred noise, and power consumption—are explicitly reported within the manuscript. Given the complete disclosure of the circuit topology and the number of carbon nanotubes used, any knowledgeable reader can independently regenerate the proposed circuits and reproduce the reported results.

Furthermore, the supplementary files provide comprehensive simulation and design resources. Specifically, the functional performance simulations were carried out using HSPICE 2008.03 with the Stanford University S-CNTFET model in 32-nm technology. The HSPICE codes corresponding to the three proposed topologies—namely, the inverter-based transimpedance amplifier (TIA), the limiting amplifier, and the optical receiver—are included in the supplementary file labeled "HSPICE 2008.03". In addition, the physical layout designs of these three topologies were developed using The Electric VLSI Design System 9.07, and the corresponding layout files are provided in the supplementary file with the same name.

Technical Note (Supplementary Information):

Before executing the HSPICE simulation codes, the CNFET library file must be placed in the directory 'C:\CNFET.lib'. Moreover, in the inverter-based circuit file, the commands related to eye-diagram analysis are marked with an asterisk (*). To activate the eye-diagram simulation, the asterisks preceding the eye-diagram commands should be removed, and an asterisk should instead be placed before the 'Iin' command.