Supplementary information:
Quantum circuit simulation with a local time-dependent variational principle

A. Generators of quantum gates

We list the generators of quantum gates used in our experiments. Here, θ denotes the rotation angle parameter. The generators are provided in the convention $U(\theta) = \exp(-i\theta H)$, where H is the generator. Note that we only use the generators of two-qubit gates,

$$R_{zz}(\theta) = \exp\left(-i\,\frac{\theta}{2} Z \otimes Z\right), \quad R_{yy}(\theta) = \exp\left(-i\,\frac{\theta}{2} Y \otimes Y\right), \tag{1}$$

$$R_{xx}(\theta) = \exp\left(-i\,\frac{\theta}{2} X \otimes X\right), \quad \text{CNOT} = \exp\left(-i\,\frac{\pi}{4}(I - Z) \otimes (I - X)\right). \tag{2}$$

since single qubit gates are contracted directly into the corresponding site tensors without using TDVP.

B. Benchmark circuits

In this work, we benchmark local TDVP on four classes of quantum circuits that reflect a broad range of structures found in many-body simulation and variational quantum algorithms. These include: (1) the one-dimensional Heisenberg model with open and periodic boundary conditions, (2) the two-dimensional Ising model on a square lattice, (3) quantum approximate optimization algorithm (QAOA) circuits using R_x and R_{zz} gates, and (4) hardware-efficient ansatz (HEA) circuits with random single- and two-qubit gates. All circuits were constructed to exhibit nontrivial entanglement dynamics and include both local and non-local interactions. For the Hamiltonian circuits, standard first-order Trotterization techniques are used, while the variational circuits follow common layouts from quantum algorithm design.

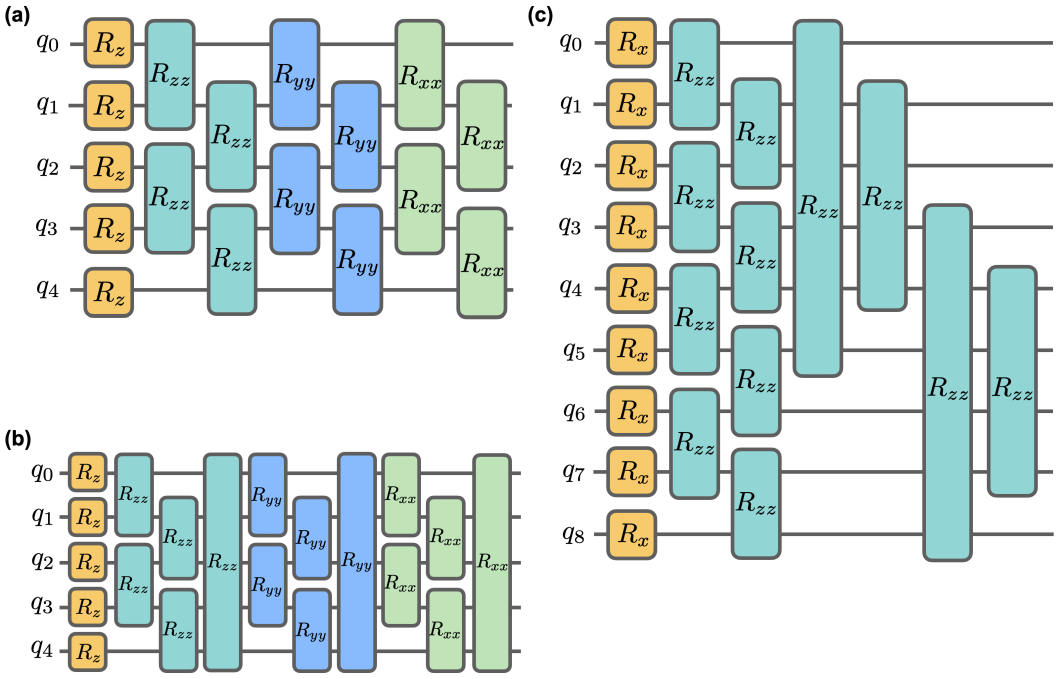

FIG. 1. **Trotterized quantum circuits for the models benchmarked in this work.** **(a)** Circuit for the open boundary one-dimensional Heisenberg model. **(b)** Circuit for the periodic one-dimensional Heisenberg model. **(c)** Circuit for the 3×3 two-dimensional Ising model, mapped to a one-dimensional snaking MPS layout.

1. One-dimensional Heisenberg model

The simulated circuit corresponds to the Trotterized evolution under the one-dimensional XXX Heisenberg Hamiltonian (with open and periodic boundaries)

$$H_{\text{Heis}} = \sum_{\langle i,j \rangle} J \left(X_i X_j + Y_i Y_j + Z_i Z_j \right) + h \sum_i Z_i, \tag{3}$$

where the sum is over nearest neighbors (and includes a term connecting $L-1$ and 0 for periodic boundary conditions). These are performed at the critical point $J = h = 1$ with a timestep $\delta t = 0.1$. Each Trotter step consists of the following gates, parameterized as

$$R_z = \exp\left(-i\delta t\, hZ\right), \quad R_{xx} = \exp\left(-i\delta t\, JX \otimes X\right), \quad R_{yy} = \exp\left(-i\delta t\, JY \otimes Y\right), \quad R_{zz} = \exp\left(-i\delta t\, JZ \otimes Z\right). \tag{4}$$

The gates are applied in an even-odd/odd-even decomposition across the chain. R_z rotations are applied to all qubits, followed by R_{zz}, R_{xx}, and R_{yy} gates acting on all nearest-neighbor pairs in two sweeps (even-odd and odd-even); for periodic boundaries, gates are additionally applied between sites $(L-1, 0)$. The non-periodic and periodic Heisenberg circuit for 5 sites is illustrated in Fig. 1**(a)** and Fig. 1**(b)**.

2. Two-dimensional Ising model

The simulated circuit corresponds to the Trotterized evolution under the two-dimensional Ising Hamiltonian on a rectangular $N = n_{\text{rows}} \times n_{\text{cols}}$ lattice

$$H_{\text{Ising}} = J \sum_{\langle i,j \rangle} Z_i Z_j + g \sum_i X_i, \tag{5}$$

where $\langle i, j \rangle$ denotes all nearest-neighbor pairs on the grid. This is simulated at the critical point $J = g = 1$ with a timestep $\delta t = 0.1$. Each Trotter step consists of the following gates, parameterized as

$$R_x = \exp\left(-i\delta t\, g\, X\right), \qquad R_{zz} = \exp\left(-i\delta t\, J\, Z \otimes Z\right). \tag{6}$$

A snaking (serpentine) mapping of the two-dimensional grid to a one-dimensional qubit ordering is used for efficient MPS simulation. R_x rotations are applied to all qubits, followed by R_{zz} gates acting on all horizontally and vertically adjacent pairs, using even-odd and odd-even decompositions within each row and column which is illustrated for 9 sites in Fig. 1**(c)**.

3. QAOA circuits

To benchmark performance on variational quantum algorithms, we simulate the Quantum Approximate Optimization Algorithm (QAOA) for a 1D Ising cost Hamiltonian. Each circuit consists of p layers of alternating unitaries derived from a cost Hamiltonian and a mixing Hamiltonian:

$$U(\vec{\gamma}, \vec{\beta}) = \prod_{l=1}^{p} \left[\exp\left(-i\beta_l \sum_i X_i \right) \exp\left(-i\gamma_l \sum_{\langle i,j \rangle} Z_i Z_j \right) \right]. \tag{7}$$

Each layer is implemented with a sequence of single-qubit $R_x(\beta_\ell) = \exp(-i\beta_\ell X)$ gates, followed by two-qubit $R_{zz}(\gamma_\ell) = \exp(-i\gamma_\ell Z \otimes Z)$ gates applied to all nearest-neighbor pairs, using even-odd and odd-even sweeps as in the Trotterized models. The angles $(\vec{\gamma}, \vec{\beta})$ are randomly sampled from a uniform distribution (such that each gate's rotation angle is uniquely defined) to create diverse and entangling circuits, rather than optimized for a specific problem instance. This setup allows us to probe TDVP's behavior on variational, non-Hamiltonian circuits with structured but non-integrable dynamics.

4. Hardware-efficient ansatz (HEA) circuits

We also benchmark the method on *hardware-efficient ansatz* (HEA) circuits, which are widely used in variational quantum algorithms due to their shallow depth and compatibility with quantum hardware constraints. Each HEA layer consists of arbitrary

single-qubit rotations followed by entangling two-qubit gates between neighboring qubits

$$U_{\text{HEA}} = \prod_{l=1}^{d} \left[\bigotimes_{i} U_3^{(i)}(\theta_l) \right] \cdot \left[\prod_{\langle i,j \rangle} \text{CZ}_{i,j} \right], \tag{8}$$

where $U_3(\theta) = R_z(\theta_1)R_y(\theta_2)R_z(\theta_3)$ is a universal single-qubit gate, and CZ is the controlled-Z gate. We use a brickwork entangling pattern, alternating between even-odd and odd-even layers. The single-qubit parameters are sampled randomly from a uniform distribution, generating circuits with high expressivity and low regularity. This circuit class serves as a stress test for TDVP under irregular, high-depth gate sequences and random entanglement growth.