Supplementary Information

SAT-Attack Resistant Hardware Obfuscation using Camouflaged Two-Dimensional Heterostructure Devices

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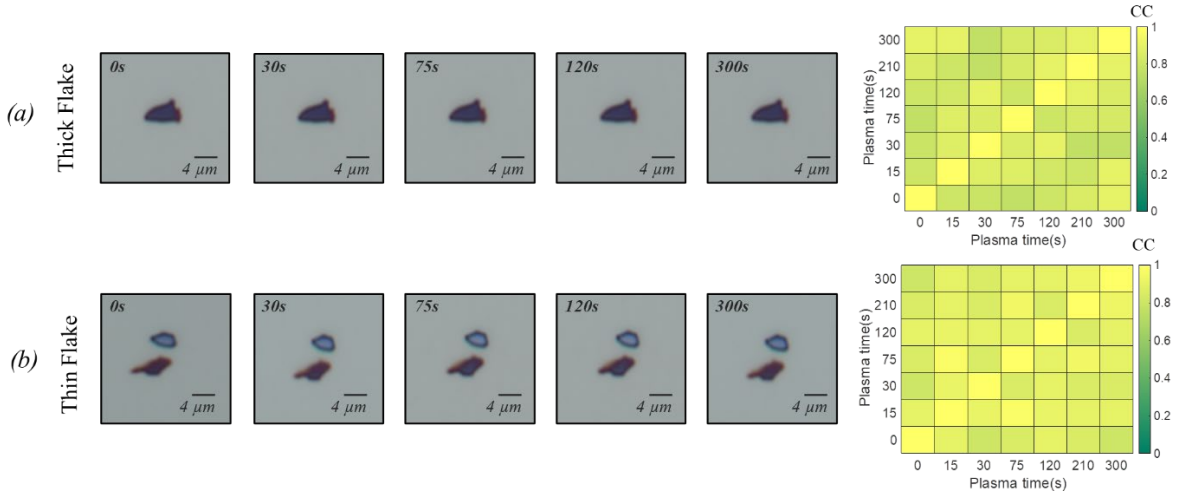
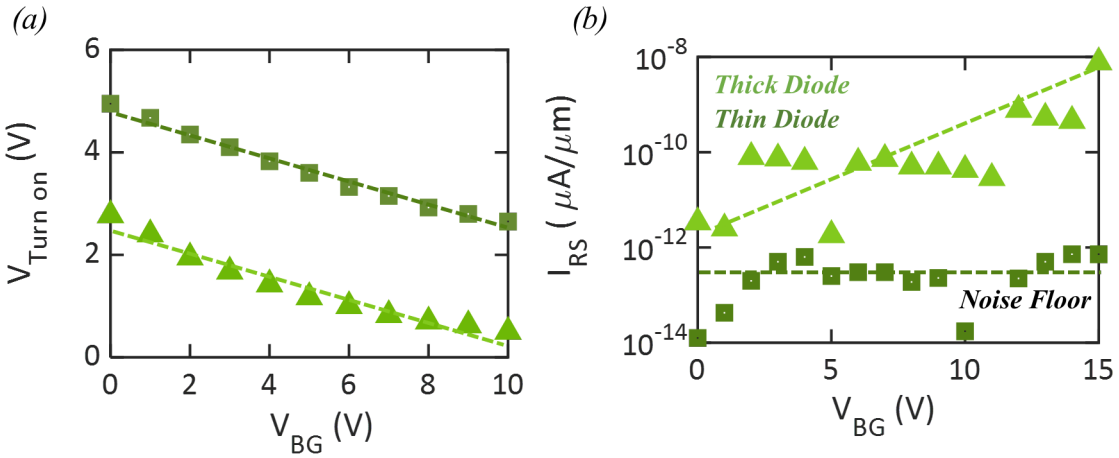
Supplementary Information 1

Evolution of optical images of WO_{3-y}/WSe_2 hetero-stacks of two different thicknesses as a function of the plasma exposure time and corresponding correlation coefficients (CC) between the binarized images. The CC values close to '1' indicate perfect similarity between the images.



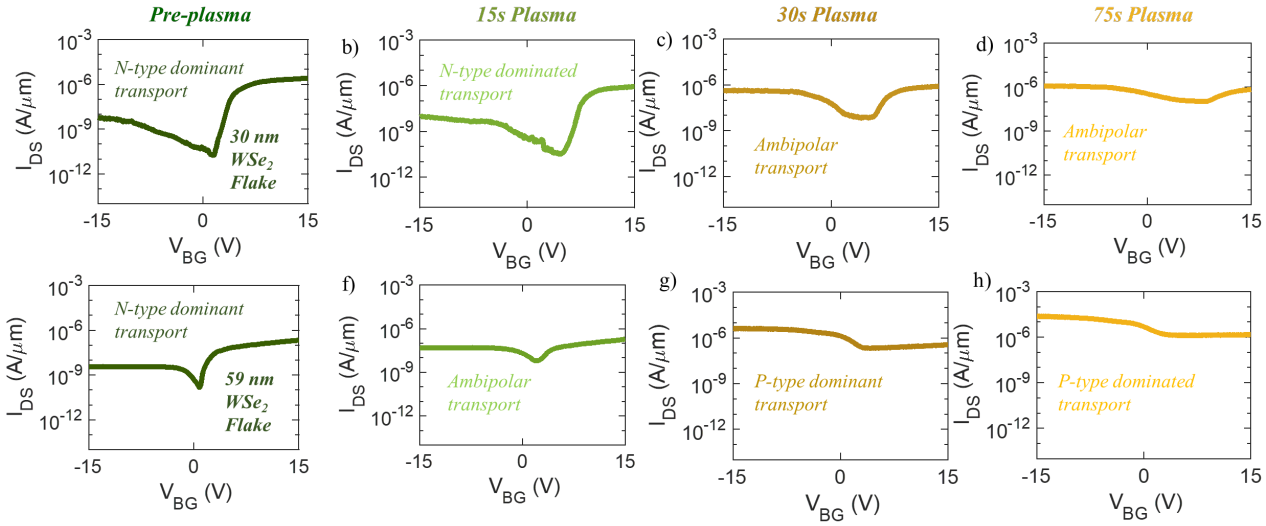
Supplementary Information 2

Tunability in a) diode turn-on voltage and b) reverse saturation current using V_{BG} for thin and thick WO_{3-y}/WSe_2 stacks.



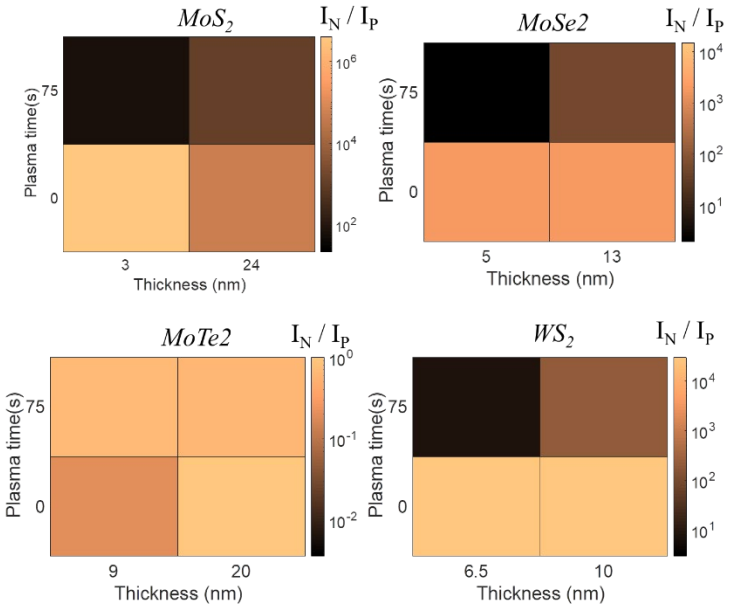
Supplementary Information 3

The evolution of the transfer characteristics for 30 nm and 59 nm thick WSe_2 flakes as a function of the plasma exposure times.



Supplementary Information 4

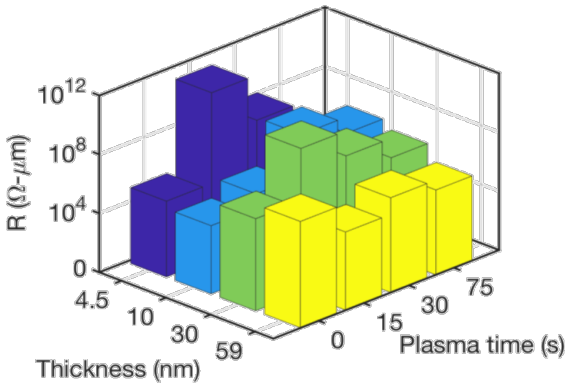
The relative strength of electron and hole conduction in various TMO/TMD hetero-stacks pre- and post-plasma exposure.



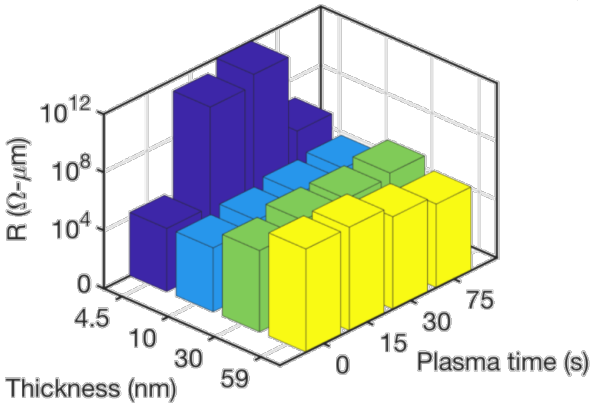
Supplementary Information 5

Gated camouflaged resistors.

WO_{3-y}/WSe_2 Camouflaged Resistor V_{BG} @ 5V



WO_{3-y}/WSe_2 Camouflaged Resistor V_{BG} @ 10V



WO_{3-y}/WSe_2 Camouflaged Resistor V_{BG} @ 15V