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A design of SP6T and SP8T RF switch chips with high isolation and low insertion loss based on SOI CMOS technology

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***Abstract*—A high-performance RF(Radio Frequency) switch chip integrating a CMOS front-end control driver module is designed in this paper based on the 0.11μm SOI CMOS process. This chip integrates the SP6T and SP8T switches for the first time, and the two switches operate in different frequency bands respectively. This RF switch chip is designed for use in RF front-end transceiver systems, mainly for channel selection at the receiving end (Rx). Meanwhile, a series-parallel structure design is adopted by the chip, and the overall performance is further enhanced through negative pressure bias technology. The SP6T switch in this chip operates in the Low-Band frequency band below 0.9GHz. The insertion loss is 0.44dB, the isolation is 38.22-47.60dB, the input P0.1dB compression point is 30.61dBm, the second harmonic is 97.12dBm, and the third harmonic is 99.73dBm. The switch switching time is 200.89ns. The SP8T switch in this chip operates in the High-Band frequency band below 2.7GHz and also takes into account the Mid-Band frequency band below 2GHz. The insertion loss is 0.90dB, the isolation is 30.82-34.95dB, and the input P0.1dB compression point is 33.65dBm. The second harmonic is 93.77dBm, the third harmonic is 95.49dBm, the switching time is 205.55ns, and the current consumption of the CMOS front-end control drive module is approximately 100μA. The size of the proposed RF switch chip is 730μm×730μm.**

***Index Ter*ms—SOI CMOS, RF Switch, SP6T, SP8T, insertion loss, isolation**

I. INTRODUCTION

As a key component for signal routing, RF switches need to meet requirements such as high frequency, low loss, high isolation, and multi-band compatibility. Although traditional RF switch processes (such as GaAs and PIN diodes) have high-frequency advantages, they face bottlenecks such as high cost, low integration, and high power consumption, making it difficult to meet the demands of 5G large-scale MIMO technology, OFDM technology, and CA technology. The pHEMT process has excellent insertion loss due to its high bandgap width and high carrier mobility, but its performance in the low-voltage region is very poor and it cannot be integrated with some other components.[1] The bulk silicon CMOS process performs well in the low-voltage region and has a high degree of integration, but it is limited in high-power scenarios and also has the disadvantages of high parasitism and high loss. Moreover, it has the disadvantages of high parasitism and high loss. The SOI process integrates the advantages of the three and has become the preferred process for RF switch design due to its unique physical properties. By embedding an oxygen layer (BOX) to achieve dielectric isolation between the device and the substrate, SOI can significantly reduce parasitic capacitance by more than 50% compared to traditional silicon-based processes, enhancing high-frequency performance and linearity, while supporting high-density integration and low-power design.[2] The SP6T and SP8T RF switches designed in this paper achieve the characteristics of low insertion loss and high linearity by adopting series-parallel topology design and positive and negative voltage bias and other methods.

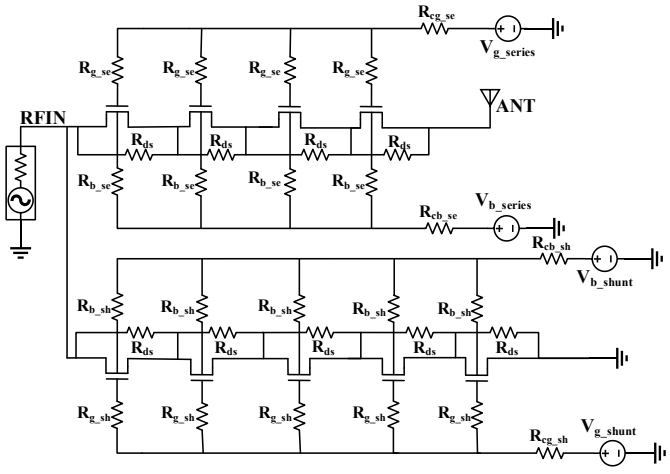


Fig. 1. Schematic diagram of a single SPST switch unit module.

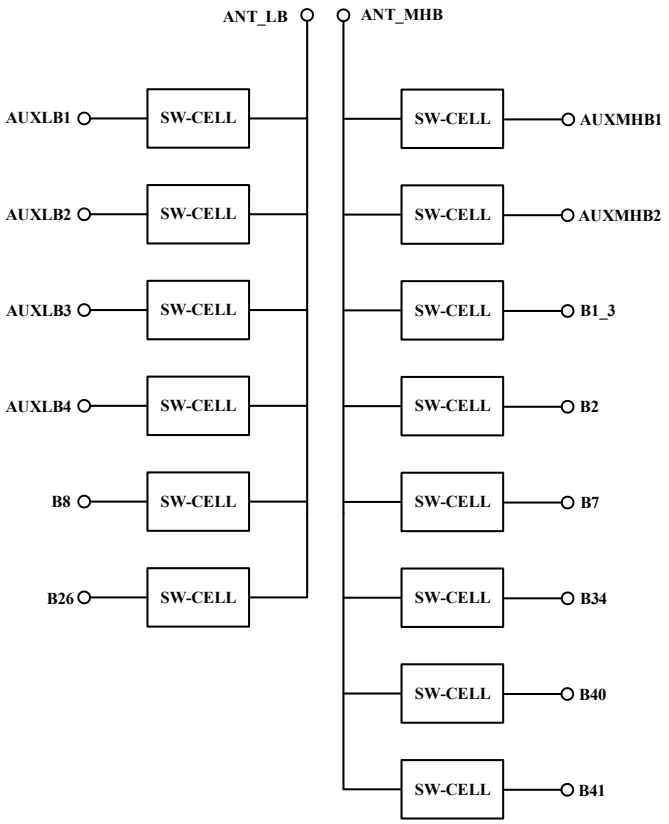


Fig. 2. Main architecture of the SP6T and SP8T RF switches.

II. Proposed Architechture

A series-parallel topology structure design is adopted by the switch designed in this paper. Compared with the series structure, the series-parallel structure can not only achieve low insertion loss but also improve isolation.[3] Transistor stacking technology is adopted to enhance power capacity and linearity. By connecting multiple transistors in series to evenly distribute the RF signal voltage across each transistor, the power processing capability can be significantly improved.[4] However, this will lead to an increase in the on-resistance Ron of the conducting branch, causing the insertion loss performance of the RF switch to deteriorate. Therefore, the sizes of the series and parallel transistors have been optimized. Positive pressure charge pumps and negative pressure charge pumps are used to provide positive and negative biases to obtain the required VDD and -VDD voltages. Through this method, the non-ideal working state of the switch tube in the off branch is effectively suppressed, harmonic distortion is reduced, and thereby the power handling capacity and linearity of the RF switch are improved. By adopting AC floating bias technology, adding high-resistance floating bias resistors at the gate and body ends of series and parallel branch transistors can effectively improve insertion losses. [5]

As shown in Figure 1, it is the schematic diagram of a single SPST switch unit module. When this switch is on, the series path RFIN-ANT is on and the parallel path RFIN-GND

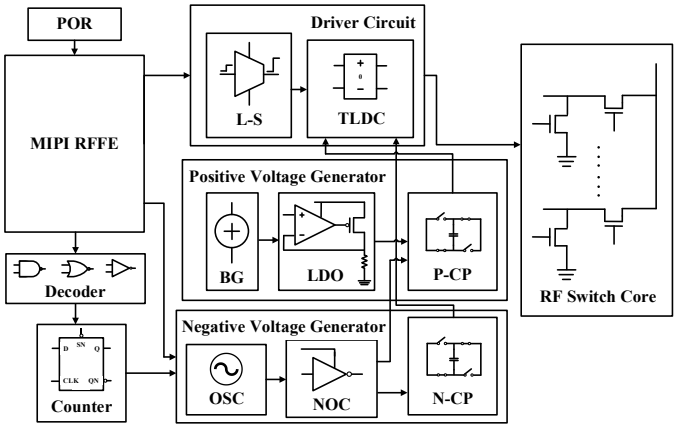


Fig. 3. Overall architecture block diagram of the RF front-end CMOS control driver module.

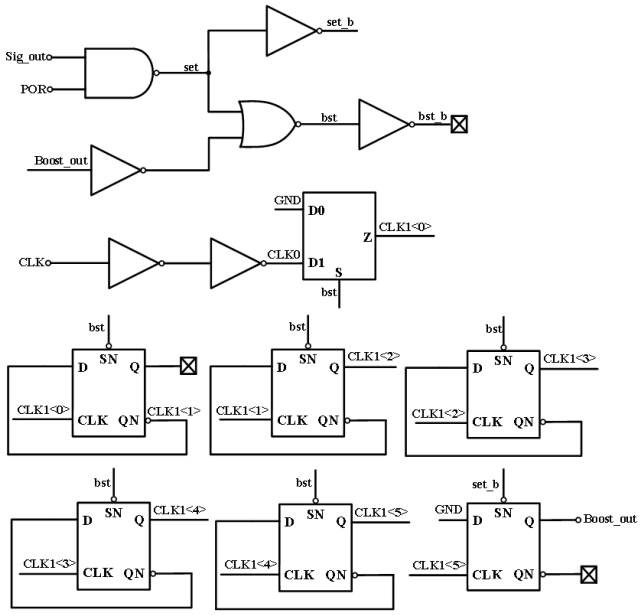


Fig. 4. Schematic diagram of the counter delay frequency reduction circuit.

is off. When this switch is off, the series path RFIN-ANT is off and the parallel path RFIN-GND is on.

As shown in Figure 2, the main architecture of the SP6T and SP8T RF switches is presented. The SW-CELL switch unit in the figure is a single SPST switch unit module. Each receiving unit is composed of MOS transistors stacked in series and in parallel. When one receiving port is connected, the series path is in the conducting state, while the parallel path is in the off state. For other receiving ports, the series path is off, while the parallel path is on.

The RF front-end CMOS control driver module designed in this paper mainly consists of the MIPI control protocol, driver circuit, positive pressure generator and negative pressure generator. The drive circuit is mainly composed of a level conversion circuit and a four-output three-value logic circuit, which perform positive and negative voltage biasing for the SP6T and SP8T RF switches. The positive voltage generator mainly consists of a bandgap reference source, an LDO and a positive voltage charge pump, which is used to generate the positive voltage of the VDD. The negative pressure generator

mainly consists of an oscillator, a non-overlapping clock circuit and a negative pressure charge pump, which is used to generate a negative voltage of -VDD. The RF switch section is formed by the combination of SP6T and SP8T RF switches. The POR circuit is used for the digital logic initialization of the MIPI control protocol. The Decoder part is a double-edge monostable trigger circuit, which is used to detect the RF signal jump at the MIPI end and generate a pulse output. The Counter section is a counter delay frequency reduction circuit, which effectively enhances the driving capacity of the charge pump, reduces power consumption, and minimizes the influence of high-order harmonics. As shown in Figure 3, it is the overall architecture block diagram of the RF front-end CMOS control driver module designed in this paper.

In the RF front-end CMOS control driver module designed in this paper, a counter delay frequency reduction circuit is innovatively proposed as the counter module. The charging speed of the charge pump is directly related to the switching speed of the switch. When the switch is switched, there will be some leakage of charge in the charge pump. The recovery time for the charge pump to be re-established is limited by its charging capacity. The traditional approach is to use a fixed clock frequency, but a low clock frequency has a slow establishment process, while a high clock frequency will lead to a significant increase in power consumption. As shown in Figure 4, this paper designs a counter delay frequency reduction circuit for the first time, which effectively improves the above situation. This circuit only keeps the output at a high level when the switch is switched, keeping the subsequent OSC at a high clock frequency. During steady-state operation, the switch is switched at a low level, keeping the subsequent OSC at a low clock frequency. This can effectively accelerate the establishment speed of the charge pump and quickly stabilize it during switch switching, which can effectively reduce certain power consumption and lower the interference of high-order harmonics on the RF switch. This circuit also provides a switching delay when the switch is switched, which can effectively prevent the charge pump from starting the state transition before it is fully charged.

In the above figure, the input CLK signal is provided by the OSC output terminal Voutp. When a pulse signal generated by the double-edge monostable trigger circuit has not yet arrived, that is, when the switch is still in a steady state, at this time, the Sig_out at the input end is at a high level, and the POR signal at the other end is also at a high level. After passing through the NAND gate, the set signal is generated at a low level, and the set signal then passes through an inverter to obtain the set_b signal at a high level. When the set_b signal is used as the reset signal of the D flip-flop at the output terminal, it can be obtained that the output signal Boost_out is at a low level when the switch is in a steady state. The Boost_out signal then passes through an inverter to obtain a high level, and the previous set signal passes through the NOR gate to obtain a bst signal with a low level. This signal serves as the reset signal for other D flip-flops.

When the pulse signal generated by the double-edge monostable trigger circuit arrives, the set signal is at a high level and the set_b signal is at a low level. The D flip-flop at the Boost_out end is reset, and Boost_out is at a high level. After passing through an inverter, it reaches a low level, and then passes through the NOR gate with the set signal to obtain the bst signal at a low level. At this point, other D flip-flops are still in the reset state.

Before entering the next steady state after the pulse signal ends, a delay will be generated due to the frequency division effect of the counter structure. This delay is related to the number of D flip-flops and the input clock frequency of the D flip-flop, as shown in Equation (1) :

$$t_{delay} = \frac{2^{N-2}}{f} \tag{1}$$

In the above formula, t_{delay} represents the delay generated by the counter structure, f is the input frequency of the D flip-flop, and N is the number of D flip-flops. In this design, the value of N is 7. It can be found that within the delay interval, the frequency of each D flip-flop will drop by half. The OSC designed in this paper is in the switching steady state when the output at the Boost_out terminal of this circuit is low level, and the operating frequency of the OSC is 8M. When the output at the Boost_out terminal is high level, it is in the switching state. The operating frequency of OSC has been raised to 16M. Therefore, the tdelay obtained in this design is approximately 4us.

When the delay ends and the next switch enters a steady state, the input terminal IN is at a high level, resulting in a set signal at a low level and a set_b signal at a high level. At this point, the D flip-flop at the Boost_out terminal enters the reset state again. The output signal Boost_out is obtained to be at a low level. The Boost_out signal then passes through the inverter to reach a high level and connects with the set signal through the NOR gate to obtain the bst signal, which is at a low level. At this point, the other D flip-flops enter the reset state again. The Boost_out output terminal is connected to the SC1 control terminal of the oscillator, effectively controlling its oscillation frequency.

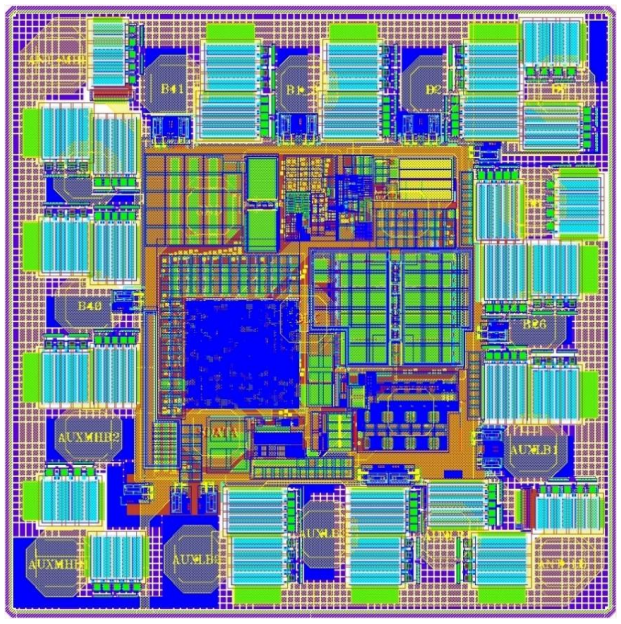


Fig. 5. Single-chip design layout of the SP6T and SP8T RF switches.

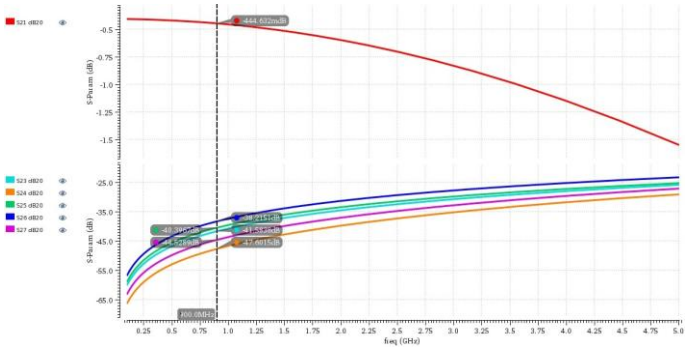


Fig. 6. Post-simulation results of the insertion loss and isolation of the SP6T RF switch.

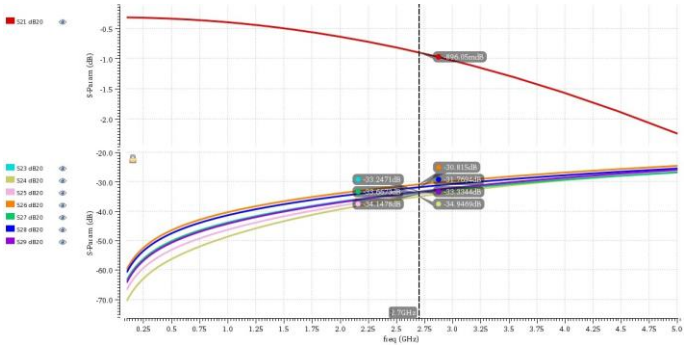


Fig. 11. Post-simulation results of the insertion loss and isolation of the SP8T RF switch.

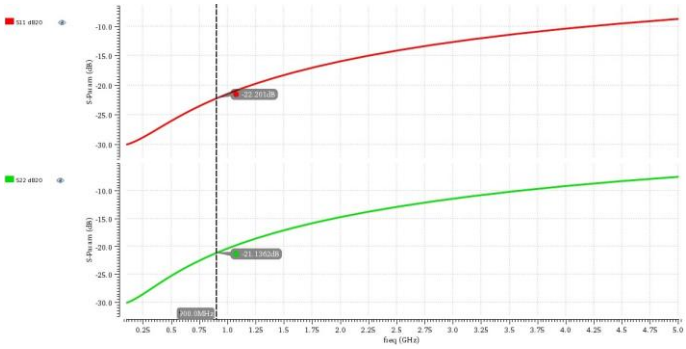


Fig. 7. Post-simulation results of the return loss of the SP6T RF switch.

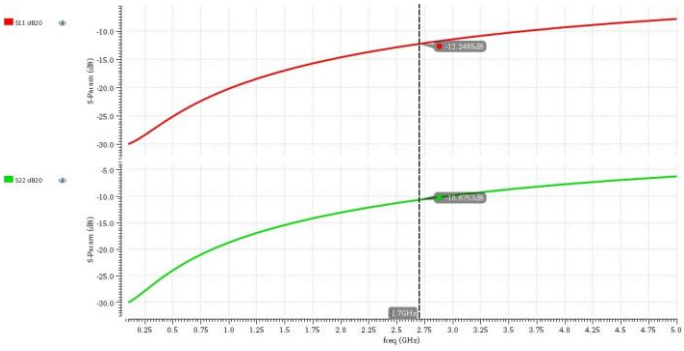


Fig. 12. Post-simulation results of the return loss of the SP8T RF switch.



Fig. 8. Post-simulation results of the input $P_{0.1}$dB of the SP6T RF switch.

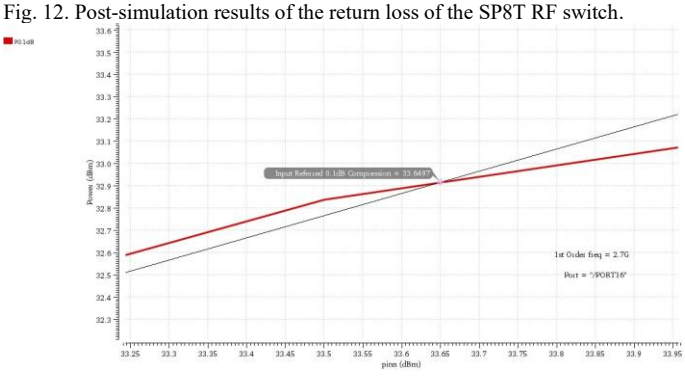


Fig. 13. Post-simulation results of the input $P_{0.1}$dB of the SP8T RF switch.

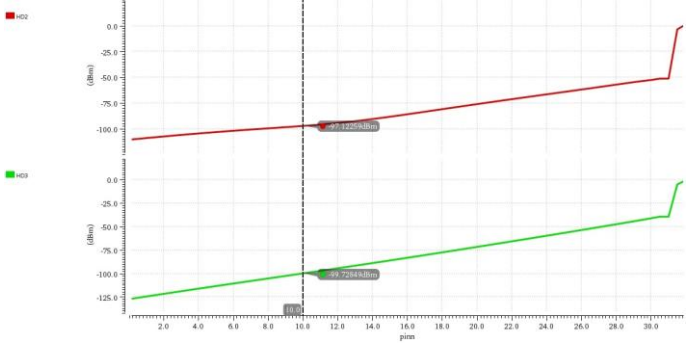


Fig. 9. Post-simulation results of the second and third harmonics of the SP6T RF switch.

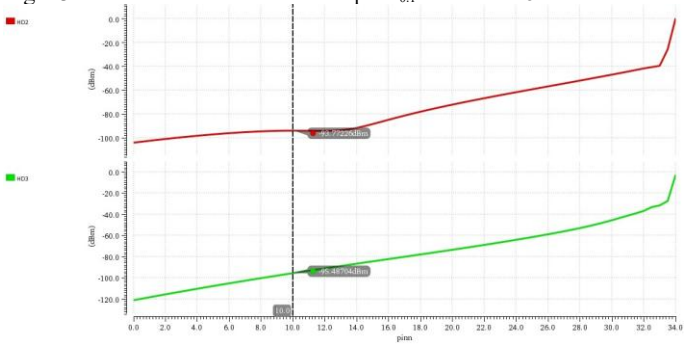
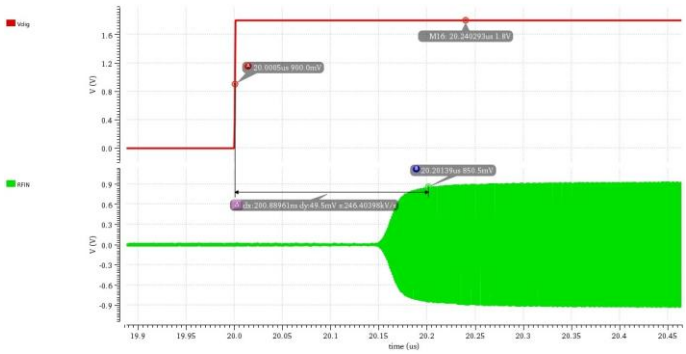
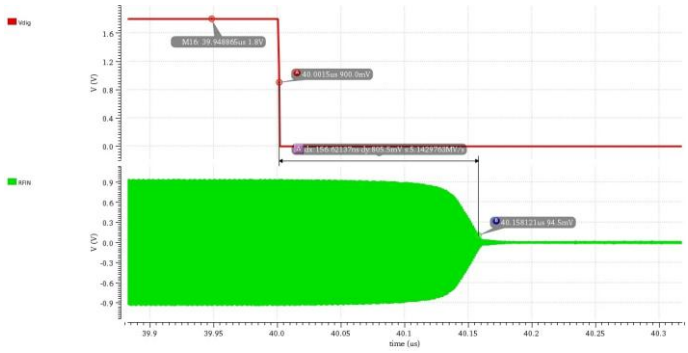


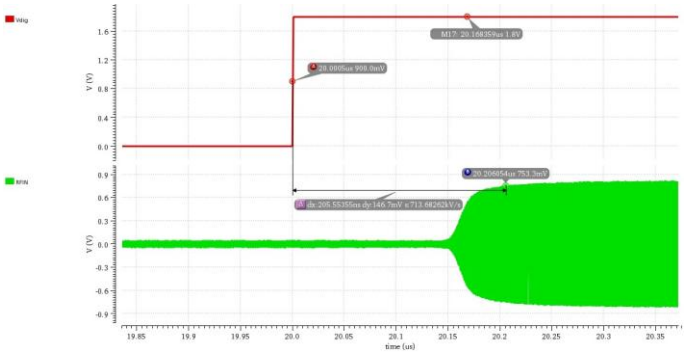
Fig. 14. Post-simulation results of the second and third harmonics of the SP8T RF switch.



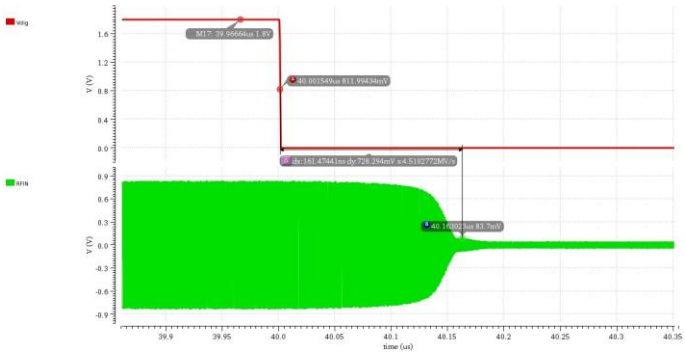
(a) Post-simulation of the on-time of the SP6T RF switch.



(b) Post-simulation of the off-time of the SP6T RF switch.
Fig. 10. Post-simulation results of the switching time of the SP6T RF switch.



(a) Post-simulation of the on-time of the SP8T RF switch.



(b) Post-simulation of the off-time of the SP8T RF switch.
Fig. 10. Post-simulation results of the switching time of the SP8T RF switch.

III. Implementation Result

As shown in Figure 5, it is the complete design layout of this high-performance RF switch single-chip. This layout is manufactured based on 0.11μm SOI CMOS process. The main body of the layout is mainly composed of SP6T and SP8T RF switch circuits and CMOS front-end control drive circuits. The middle part of the entire chip is the MIPI control protocol and CMOS control drive circuits. The CMOS control driver circuitincludes modules such as LDO, Bandgap, OSC, CP and Driver. The surrounding parts are the SP6T and SP8T RF switches. This design integrates the SP6T and SP8T RF switches and the CMOS front-end control drive circuit on a single chip for the first time. The SP6T and SP8T RF switches occupy 75% of the entire chip due to the large size of the high-power switch tubes and the large number of stacks. The overall area of this RF chip layout is 730um×730um.

(1) Post-simulation analysis of the SP6T RF switch

As shown in Figure 6, under the simulation conditions of TT process Angle and a temperature of 27℃, the insertion loss of the SP6T RF switch in Rx mode at the 0.9GHz frequency point is 444.63mdB, and the isolation to each port is between 38.22 and 47.60dB.

As shown in Figure 7, under the simulation conditions of TT process Angle and a temperature of 27℃, the input return loss of the SP6T RF switch in Rx mode at the 0.9GHz frequency point is 22.20dB, and the output return loss is 21.14dB.

As shown in Figure 8, under the simulation conditions of TT process Angle and a temperature of 27℃, the input P0.1dB of the SP6T RF switch in Rx mode at the 0.9GHz frequency point is 30.61dBm.

As shown in Figure 9, under the simulation conditions of TT process Angle, temperature of 27℃, and input power of 10dBm, the second harmonic suppression of the SP6T RF switch in Rx mode at the 0.9GHz frequency point is 97.12dBm, and the third harmonic suppression is 99.73dBm.

As shown in Figure 10, under the simulation conditions of TT process Angle, temperature of 27℃, and input power of 10dBm, the on-time of the SP6T RF switch in Rx mode at the frequency point of 0.9GHz is 200.89ns, and the off-time is 156.62ns. Therefore, the switching time of the SP6T RF switch is 200.89ns.

(2) Post-simulation analysis of the SP8T RF switch

As shown in Figure 11, under the simulation conditions of TT process Angle and a temperature of 27℃, the insertion loss of the SP8T RF switch in Rx mode at the 0.9GHz frequency point is 896.05mdB, and the isolation to each port is between 30.82 and 34.95dB.

As shown in Figure 12, under the simulation conditions of TT process Angle and a temperature of 27℃, the input return loss of the SP8T RF switch in Rx mode at the 0.9GHz frequency point is 12.25dB, and the output return loss is 10.68dB.

As shown in Figure 13, under the simulation conditions of TT process Angle and a temperature of 27℃, the input P0.1dB of the SP8T RF switch in Rx mode at the 0.9GHz frequency point is 33.65dBm.

As shown in Figure 14, under the simulation conditions of TT process Angle, temperature of 27℃, and input power of 10dBm, the second harmonic suppression of the SP8T RF

switch in Rx mode at the 0.9GHz frequency point is 93.77dBm, and the third harmonic suppression is 95.49dBm.

As shown in Figure 15, under the simulation conditions of TT process Angle, temperature of 27℃, and input power of 10dBm, the on-time of the SP8T RF switch in Rx mode at the frequency point of 0.9GHz is 205.55ns, and the off-time is 161.47ns. Therefore, the switching time of the SP8T RF switch is 205.55ns.

IV. Conclusion

This paper primarily introduces a CMOS control and driver module for the RF front-end, along with two SP6T and SP8T RF switches designed for high-power applications. The main innovation of this design is the proposal of a counter delay frequency reduction circuit as the Counter module, which effectively accelerates the establishment speed of the charge pump, reduces power consumption to some extent, and mitigates the interference of higher-order harmonics on the RF switches.In terms of chip architecture, this design integrates the RF front-end CMOS control and driver module with the RF switches into a single chip, which is fabricated using a 0.11 μm SOI CMOS process. To optimize the performance of the RF switches, a negative biasing technique is employed, achieving low insertion loss and high linearity. Specifically, for the SP6T RF switch, the insertion loss is maintained below 0.5 dB, the isolation is above 35 dB, and the harmonic distortion is better than 90 dB. For the SP8T RF switch, the insertion loss is kept below 1 dB, the isolation is above 30 dB, and the harmonic distortion is also better than 90 dB.

TABLE I
SUMMARY OF SWITH MEASUREMENT RESULT

Parameters	This work		[6]	[7]
	SP6T	SP8T	SP6T	SP8T
Technology	0.11μm SOI CMOS		0.18μm SOI CMOS	90nm SOI CMOS
Supply Voltage [V]	1.8	1.8	1.8	1.8
Frequency [GHz]	0~0.9	0.9~2.7	0~0.9	0.9~2.7
Insertion Loss [dB]	0.44	0.90	0.51~0.56	0.38~0.75
Isolation [dB]	38.22~47.60	30.82~34.95	49	40
Return Loss [dB]	21.14	10.68	22	-
2nd Harmonics [dBm]	97.12	93.77	43	66
3rd Harmonics [dBm]	99.73	95.49	52	62
Input $P_{0.1dB}$ [dBm]	30.61	33.65	40	34
Switching Time (μs)	0.2	0.2	-	1.4
Current Consumption (μA)	100	100	-	120
Die Size [mm^2]	0.53		-	0.76

References

[1] Steighner J B, Yuan J S. Examination of hot carrier effects of the AlGaAs/InGaAs pHEMT through device simulation[J]. Microelectronics Reliability, 2012, 52(12): 2932-2940.

[2] El Ghizlane L C, Yasser M, Maya L, et al. Study of the SOI layer's impact on the electrical properties of the Heterojunction Bipolar Transistor BiCMOS55nm[C]//2024 International Conference on Advances in Electrical and Communication Technologies (ICAECOT). IEEE, 2024: 1-6.

[3] Rack M, Nyssens L, Courte Q, et al. Impact of device shunt loss on DC-80 GHz SPDT in 22 nm FD-SOI[C]//ESSDERC 2021-IEEE 51st European Solid-State Device Research Conference (ESSDERC). IEEE, 2021: 195-198.

[4] Gianesello F, Monroy A, Vialla V, et al. Highly linear and sub 120 fs Ron× Coff 130 nm RF SOI technology targeting 5G carrier aggregation RF switches and FEM SOC[C]//2016 IEEE 16th Topical Meeting on Silicon Monolithic Integrated Circuits in RF Systems (SiRF). IEEE, 2016: 9-12.

[5] Hejazi A, Rad R E, Asl S A H, et al. A High-Power 3P3T Cross Antenna Switch with Low Harmonic Distortion and Enhanced Isolation Using T-Type Pull-Down Path for Cellular Mobile Devices[J]. Sensors, 2022, 22(14): 5461.

[6] Blaschke V, Zwingman R, Hurwitz P, et al. A linear-throw SP6T antenna switch in 180nm CMOS thick-film SOI[C]//2011 IEEE International Conference on Microwaves, Communications, Antennas and Electronic Systems (COMCAS 2011). IEEE, 2011: 1-4.

[7] Kim D, Lee K Y. A Design of High Power SP7T and SP8T RF Switches using SOI CMOS Technology[C]//2021 18th International SoC Design Conference (ISOCC). IEEE, 2021: 35-36.