Investigating Diffusion in Silicon Wafers: A Study of Doping and Sheet Resistance Measurement.

Jyotirmoy Sarker

jxs7713@mavs.uta.edu

University of Texas at Arlington

Short Report

Keywords:

Posted Date: October 20th, 2025

DOI: https://doi.org/10.21203/rs.3.rs-7884440/v1

Additional Declarations: The authors declare no competing interests.

Investigating Diffusion in Silicon Wafers: A Study of Doping and Sheet Resistance Measurement.

Jyotirmoy Sarker, Nazifa Tabassum Khan

Department of Electrical Engineering, University of Texas at Arlington, Arlington, TX 76019, USA

Abstract

The main objective of the experiment is to calculate junction depth of a silicon wafer after pre deposition and two drive-in steps at 1000 ºC and 1100 ºC. Experimental values were compared with the calculated values and percentage differences were evaluated. Four-point probe was used to measure the sheet resistance. Spin on dopants were used, besides the tube furnace for heating purposes. Resistivity of silicon as a function of dopant concentration and Irvin's curves were used for the calculations, besides the other formulas mentioned in the report. Predeposition was done for 900 seconds, and drive-in steps were done for further 900 and 1800 seconds at 1000 ºC and 1100 ºC respectively. The wafers were cleaned using acetone and IPA, and HF dip. Predeposition and drive-in 2 values have percentage difference between calculated and experimental 33.9% and 36.9% respectively due to presence of native oxide layers, impurities or possibly for considering a fixed constant value of dopant concentration of P505 to be $0.45*10^{20}$ atoms/cm^{-3}. Drive-in 1 had percentage difference of 11.6%, which is within acceptable range for variation between the calculated and experimental results. The results were tabulated and graphed using origin pro to give a better visual representation of the results.

I. INTRODUCTION

Diffusion is a process in semiconductor fabrication where dopant atoms are introduced into silicon wafer to modify its electrical properties. Movement of atoms from high to low concentration is involved, embedding them into silicon lattice to create p-type or n-type regions. Controlled areas of positive and negative charge carriers are created, which allows the formation of components like transistors, diodes, and integrated circuits. Diffusion adjusts the conductivity of silicon, enabling it to function as a controllable semiconductor rather than an insulator.

Diffusion in semiconductor fabrication is important because it plays a role in precisely defined regions of charge carriers, which is important for device performance. Engineers can design circuits with desired characteristics like switching speeds, current capabilities, and energy efficiency, by controlling concentration and distribution of dopants. It would be difficult to produce modern electronic devices without the process of diffusion, as it plays an important role in the electrical behavior of a device.

In the laboratory, diffusion was done on a smaller scale, making it easier to study junction depth, dopant concentration and resistivity changes. The processes are discussed in detail in the experimental methods section. In the real world, due to technological advancements, diffusion is done by ion implantation, which is a more precise and efficient doping method. In this process, dopants are accelerated into silicon using an electric field, allowing more accurate placement and concentration without the need for high

temperature furnaces. Wafers are annealed to activate the dopants and repair damage to the silicon lattice after ion implantation is done. Ion implantation provides more control over dopant concentration and placement, which enables finer device features, which is important for highly miniaturized devices.

Diffusion is a straight-forward process and can be performed with relatively simple equipment. The process is effective for shallow doping profiles. It is suitable for education purposes and small-scale applications due to its low complexity. However, diffusion provides less control over the depth and concentration profiles compared to ion implantation, which makes it less efficient in the fabrication process for complex, high precision devices. While ion implantation is more expensive, it provides greater accuracy, lower thermal stress, and better suitability for fine, miniaturized semiconductor structures.

In the doping procedure used in the experiment, predeposition and drive-in were involved. It was assumed to have infinite dopant source in predepositon, which resulted in a constant surface dopant concentration, C_s. The junction depth is given by the following equation[1].

$$x_j = 2\sqrt{Dt}\,erfc^{-1}\left[\frac{C_B}{C_s}\right] \quad (1)$$

In the equation, D is diffusion coefficient, commonly known as diffusivity; t is the time of diffusion; background substrate dopant concentration is denoted by C_B, and C_s is the surface dopant concentration. Resistivity can be calculated using the formula:

$$\rho = R_s \cdot t \quad (2)$$

In equation 2, R_s is the sheet resistance and t is the initial thickness of silicon wafer which is 275 μm. Background concentration, C_B, can be found from figure 1, which gives expected resistivity as a function of dopant concentration for both p and n type dopants[2].

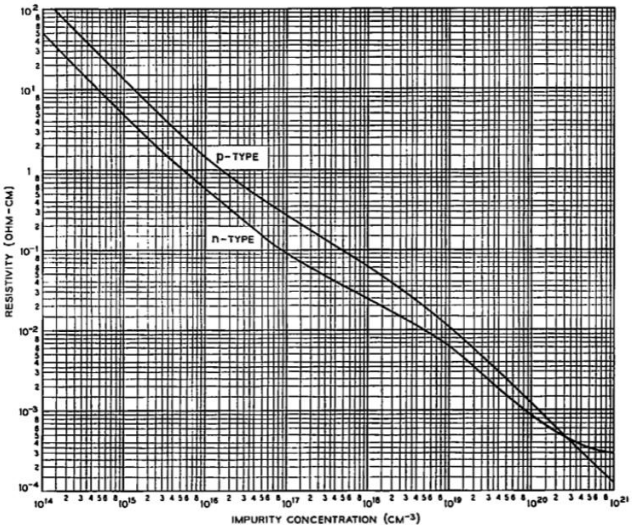

Fig 1. Graph showing resistivity of silicon as a function of dopant concentration[2].

Then, D, the diffusion coefficient, should be calculated. Phosphorous diffusion occurs through both vacancies and silicon self-interstitials[3].The process is made complicated by using boron doping (p-type), which generally slows down phosphorous diffusion[4]. It is assumed in the lab that intrinsic diffusion was performed, so the following equation[3] is used:

$$D_P^{Si} = 8 \cdot 10^{-14} e^{-\frac{2.74}{kT}} \quad (3)$$

Due to using different temperatures in predeposition and drive-in steps, values would be calculated separately for D.

Theoretically, C_s should be easy to determine, but addition of spin-on dopants make the process complicated. Ideally, it is expected that the dopants would serve as unlimited source, making the surface concentration equal to solid solubility of phosphorous in silicon. The spin-on dopants contain high amount of SiO_2, which slows down the diffusion of phosphorous through its layer, limiting the availability of dopant at the silicon interference. Also, a thin native oxide layer on the silicon wafer further hampers diffusion and reduces surface concentration[6]. It was experimentally determined by Mathiot et.al that the dopant

concentration of P505, the spin on dopant used in the experiment, to be $0.45*10^{20}$ atoms/cm^{-3}. This value is used in the experiment.

Getting the values mentioned would make it possible to calculate junction depth using equation 1.

The spin on dopant was removed after predeposition and several drive-in steps were performed. The junction depth for drive-in can be calculated using[1]:

$$x_j = \sqrt{4Dt\ ln[\frac{C_B}{C_s}]} \quad (4)$$

Where C_B is the substrate background concentration, C_S is the surface concentration, and D is diffusion coefficient. It should be kept in mind that equation[1] 4 is only valid when:

$$\sqrt{Dt_{predep}} \ll \sqrt{Dt_{drive-in}} \quad (5)$$

This would ensure the boundary condition that after predeposition the dopant is confined to an extremely thin surface layer which could be modeled with a delta function. It would indeed give a good approximation. It is important to confirm that the condition is satisfied by the diffusion conditions stated, as otherwise equation 4 cannot be used. C_B should remain the same as found from figure 1, and D should be calculated using equation at the specific drive-in temperature. C_S is not constant after the spin on dopant is removed. It would change as per the equation below:

$$C_s = C(0,t) = \frac{Q_T}{\sqrt{\pi Dt}} \quad (6)$$

In equation 6, Q_T is the total dopant dose during predeposition and can be calculated by:

$$Q_T = 2 \cdot C_0 \sqrt{\frac{Dt}{\pi}} \quad (7)$$

Where C_0 is the surface concentration, D is diffusion coefficient and t is the time for predeposition.

The junction depth could be estimated using equations 4, 6 and 7. The process will be done for each drive-in step separately using total drive-in time associated with each step for calculation. A table would be constructed with the calculated and measured values of junction depth and see the percentage difference in the values.

Measured sheet resistances should be used to get the experimental values for the junction depth. Irvin's curves[2] in Figure 2a and 2b were used. They show the relationship between the surface concentration of the dopant and the average resistivity of the doped region (R_s*x_j) at varying background concentrations. The surface concentration of a n-type dopant in a uniformly doped p-type silicon as a function of average resistivity is given in figures 2 (a and b)[8]. The Irvin curve for erfc diffusion corresponding to predeposition is shown in figure 2a and Irvin curve for gaussian diffusion corresponding to drive-in process is shown in figure 2b.

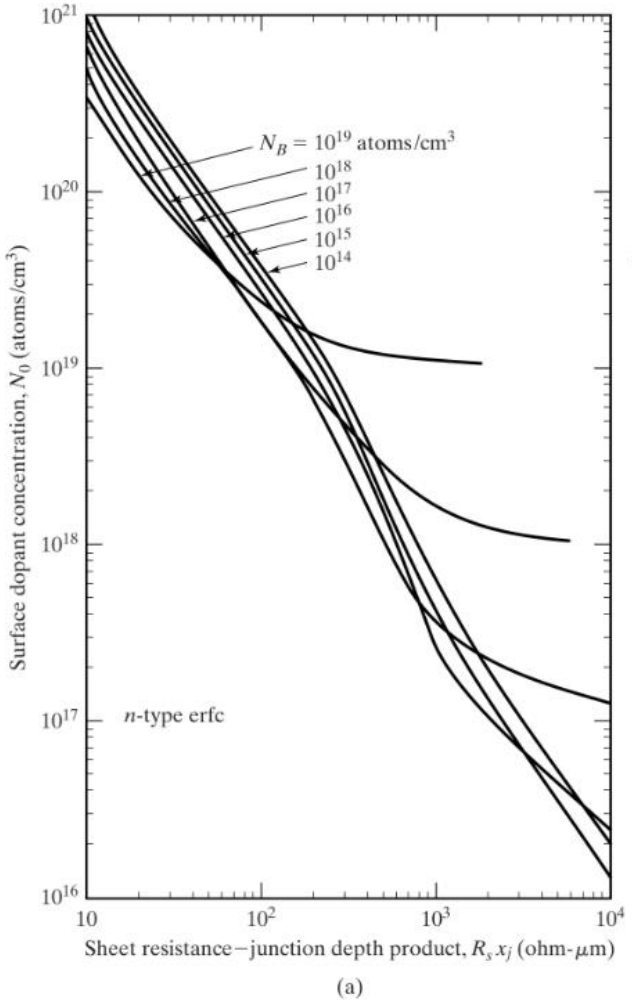

Figure 2a: The graph showing Irvin's curves for the surface dopant concentration of n-type erfc[8].

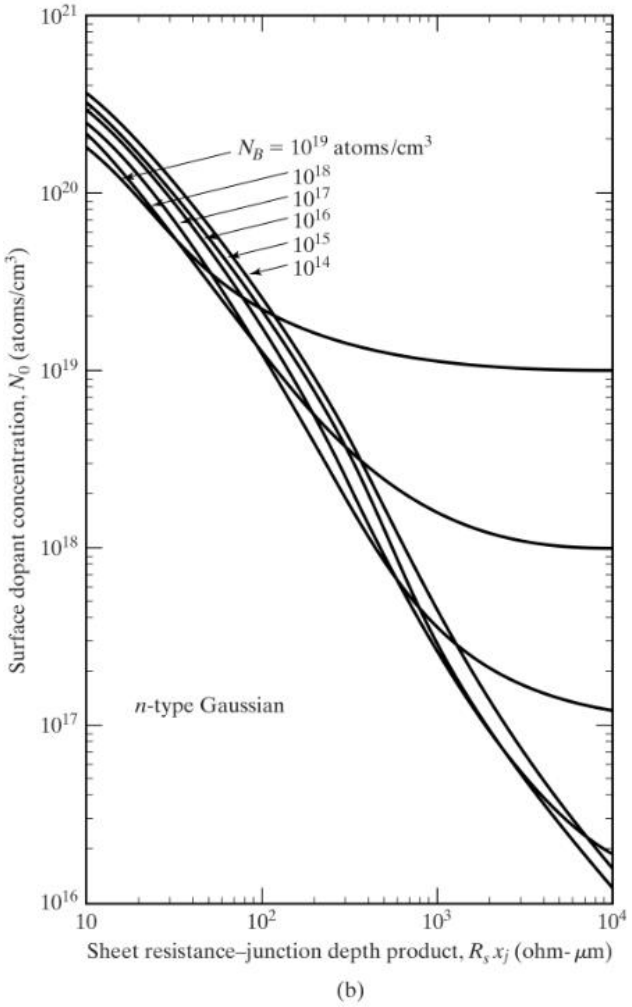

Figure 2b: The graph showing Irvin's curves for the surface dopant concentration of n-type gaussian diffusion in uniformly doped p-type silicon as a function of average resistivity at varying background concentrations[8].

X_j could be calculated using the measured value of R_s and the knows values of surface concentration.

To give visual analysis of the results, the net concentration, which is the concentration of phosphorus minus the background concentration would be plotted. The net impurity equation[1] after predeposition is given by:

(8) $$|C(z,t) - C_B| = |C_s erfc\left(\frac{z}{2\sqrt{Dt}}\right) - C_B|$$

Drive-in was graphed using the equation:

(9) $$C(z,t) = C_s e^{-\frac{z^2}{4Dt}}$$

In both equations 8 and 9, C_s is the surface concentration, D is the diffusivity, t is the diffusion time and z is the distance from the sample surface. Origin Pro would be used to draw the graph.

II. EXPERIMENTAL METHODS

The chemicals used in the experiment consist of deionized (DI) water, acetone, isopropyl alcohol (IPA), hydrofluoric acid (HF), and P505 Spin-On Dopant (SOD). All these components have specific purposes in wafer cleaning and diffusion processes. For helping in removing organic contaminants and photoresists from silicon wafer surface, acetone was used. The strong solvency of acetone helps to break down and get rid of these materials, providing an initial thorough clean for the wafers. IPA is miscible with both acetone and water. It helps removing any acetone and also evaporates quickly, reducing the possibility of having any residue on the wafer. IPA is also useful in removing nonorganic substances from the surface of the wafers.

Hydrofluoric acid, which is a highly reactive chemical, is used in diluted form (2%) to etch, and remove the native oxide layer on silicon surface, leaving a clean, hydrophobic surface necessary for proper diffusion. Since HF is highly corrosive, and contact with skin can cause severe damage, it should be handled with extreme care. P505 SOD contains an organic solvent dopant, which is used in introducing impurities to wafer during diffusion process, that is important for changing electrical properties of silicon. The dopant

should be handled carefully as it is volatile and toxic. Well-ventilated areas and protective gear should be used. Every chemical contributes to achieving precise control over the surface of the wafer and its doping properties, important for proper semiconductor fabrication.

A. Wafer Pre-Diffusion Surface Treatment and Sheet Resistance Measurement

For sheet resistance measurement, the wafers should be transferred carefully to the bench equipped with Jandel four-point probe. The sheet resistance for each of the wafers should be measured in five different locations, focusing on the center of the wafer to avoid edge effects which can skew the readings. The initial sheet resistance (R_0) values would serve as the baseline for the next measurements. For each wafer, measured values were then recorded in the lab notebook.

Next, HF dip process was performed. 2% hydrofluoric acid (HF) solution was then diluted by mixing with DI water in 1:98 ratio. The wafers were then immersed into HF solution for 30 seconds using a Teflon wafer dipper. The purpose of the step is to remove native silicon oxide layer from the surface of the wafer. After dipping, the wafers were immediately rinsed with DI water and blow-dried using nitrogen. It was verified that the wafer surface was hydrophobic by observing water beading on the surface, indicating that oxide layer was successfully removed.

B. Application of the Spin-On Dopant

The spin-coater was lined with aluminum foil, ensuring that the foil covered the area from spindle to the outer rim to avoid contamination. The spinner chuck was cleaned with acetone and securely attached to the spindle.

The wafer was placed on the spinner chuck and turned the vacuum on to hold the wafer in place. Gradually the speed of spin increased to 3000 RPM, and the centering of wafer was checked. If there was wobbling, the spinner was turned off, the wafer was repositioned, and the process was repeated until it was correctly centered. When centered, the spinner was turned off.

Using a 1mL graduated polyethylene dropper, approximately 0.5 mL of P505 Spin-On Dopant (SOD) onto the surface of wafer, giving uniform coverage. For 5 seconds, the wafer was spun at 3000 RPM to evenly distribute dopant across wafer surface. After 40 seconds, the spinner and vacuum were turned off, and the wafer was carefully removed.

The dopant-coated wafer was then transferred to a preheated hot plate at 200°C. The wafer was then baked for 10 minutes to solidify the dopant layer. For at least 20 minutes, the wafer was cooled after being removed when baking was done. If necessary, the baked wafers could be stored in a nitrogen-purged cabinet with a humidity level below 40% until further use.

C. Predeposition

The doped wafers were placed on a quartz diffusion boat. A quartz "V" boat with 3mm spacing between wafers was used. It was made sure that the coated sides of the wafers faced each other to minimize deviations in sheet resistance during the diffusion process. It was estimated the deviation would be around 1%.

The nitrogen valve was then opened, and the flow rate was set to 0.75 liters per minute (LPM). The furnace was then preheated to 1000°C while maintaining nitrogen flow rate to prevent contamination from external gases.

The oxygen flow rate was adjusted to 0.25 LPM to create a 3:1 nitrogen-to-oxygen environment. After the correct flow rates were ensured, oxygen flow was turned off and nitrogen flow was continued to maintain furnace atmosphere.

The quartz diffusion boat with wafers was slowly inserted into the center of the tube furnace using a quartz rod. The furnace was then closed, and the oxygen flow was turned on. The wafers were then heated for 15 minutes in the furnace. The oxygen valve was closed after heating, the quartz boat was removed, and the wafers were allowed to cool for 15 minutes.

Another HF dip was performed using the same processes as stated in A for removing any remaining phosphorous silicate formed during predepositon process. The sheet resistance was measured in five locations on each wafer, and the values were recorded as $R_{predepositon}$.

D. Drive-In Process

The tube furnace was preheated to 1100°C.The drive-in process was set to take place in a nitrogen-only environment. For that, it was ensured that the oxygen valve remained closed.

The furnace was opened, and the wafers were reintroduced into the tube furnace. The wafers were heated for 15 minutes and then carefully removed from it. The wafers were then cooled down to room temperature for around another 15 minutes.

The sheet resistance was measured in dive different locations on each wafer, and the values were recorded as $R_{drive\text{-}in1}$. The drive-in heating process and sheet resistance measurement was done 2 more times to get a dataset of sheet resistance as a measure of time.

III. RESULTS AND DISCUSSION

The experiment was mainly to investigate the diffusion process in two p-type silicon wafers by comparing junction depths (x_j) and sheet resistance (R_s) in different conditions. To evaluate the distribution of impurity concentrations and their effect on the electrical characteristics of silicon, the predeposition and drive-in procedures were examined over time. The average readings of 2 wafers of both the members of the group were used. The junction depth for predeposition was calculated equations 1 and 2, and with data from figure 1. Equations 3, 4, 6 and 7 were used for the junction

depths for the drive-ins. For experimental values, substrate concentrations were calculated using equations 6 and 7.Using those values of C_s, Irvin's curve from figure 2a was used to get the value for sheet resistance junction depth (R_s x_j) value, which was then divided by sheet resistance before predeposition to get the experimental junction depth for predeposition and the values are noted down in table 1. Figure 2b was used in the same way, and junction depth of drive-in was found. Percentage errors measured and experimental values were found to show the difference in the results. A visual representation of results is shown in figure 3.

	Time (s)	Calculated x_j (μm)	Measured Average R_S (Ω/□)	Experimental x_j (μm)	Percent Difference (%)
Predeposition					
	900	0.165	316.5	0.221	33.9
Drive-in					
1	900	0.413	232.7	0.365	11.6
2	1800	0.569	192.5	0.779	36.9

Table 1: Percentage difference between the calculated and experimental junction depth values.

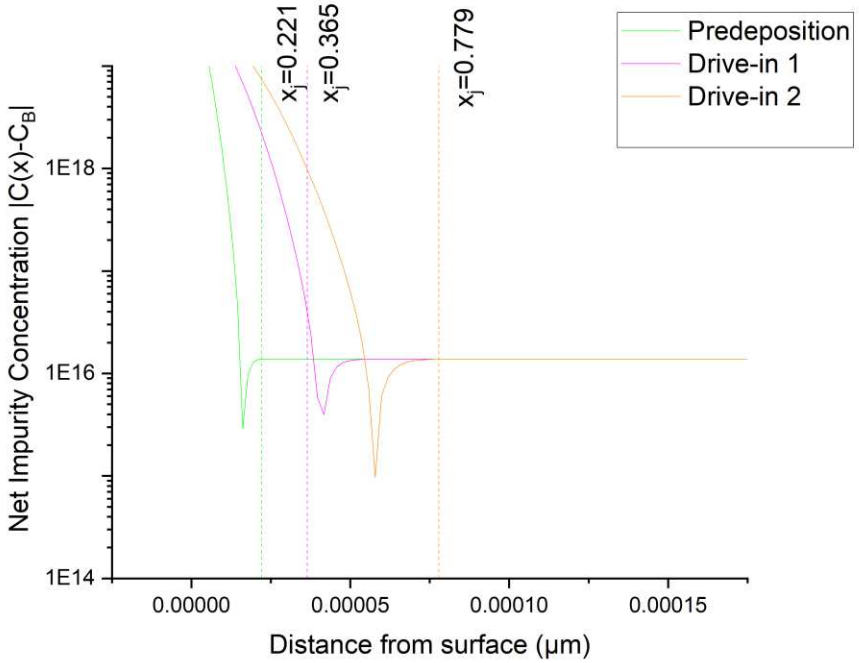

Fig 3: Calculated net dopant impurity concentration as a function of distance from sample surface for predeposition and drive-in diffusion. The vertical dashed lines represent junction depth determined from resistance measurement.

900 seconds of the first drive in process gave a calculated junction depth of 0.165 μm while the experimental data was 0.221 μm. The sheet resistance was 316.5 Ω/□. This indicated that there might be a doped region near the surface. There was a percentage difference of 33.9%.

The first drive in had calculated and experimental values 0.413 μm and 0.365 μm, with percentage error of 11.6%, which is fairly lower than the other two values. This could be due to the better condition of the wafer. It might have less or no crystals on it, and possibly no oxide layer formed on it.

The second drive in had calculated value of 0.569 μm and the experimental one had 0.779 μm, and the percentage difference was 36.9%. This might be due to divergence in experimental conditions and assumptions in calculation model, which might be due to extended high temperature exposure on dopant behavior due to structural changes of the wafer.

The discrepancy in results could be due to native oxide layer on the wafers, and some crystals also formed during doping. Native oxide layers form when silicon is exposed to oxygen, and act as barrier to dopant diffusion. This could give lower penetration depth as dopants might not distribute or penetrate evenly. This could result in lower junction depth than the theoretical value. Additionally, during high temperature doping, there could be local crystallographic alterations or clustering, which might not allow uniform distribution of dopants. This could lead to variations in sheet resistance and junction depth measurements, so errors could be there with experimental and calculated results. Another possibility of error could be measurement uncertainties while taking sheet resistance measurement using four-point probe. There could be variations in the calculated values due to any small errors in the measurements. The presence of impurities could have created non uniform diffusion.

In table 1, the sheet resistance decreased over time as with each phase of diffusion, more charge carriers penetrated the silicon wafer, resulting in increased concentration of charged carriers in the wafer. The resistivity of the material was reduced with the higher dopant concentration, allowing current to flow more easily. Also, more time for diffusion allowed more uniform distribution of dopants, which further lowered resistance across wafer.

In figure 3, the graphs show increase in junction depth with increase in time as due to diffusion, the dopant atoms penetrate deeper into the silicon wafer over the time. As diffusion time and temperature increase, the dopants spread further from the surface, resulting in greater junction depth for subsequent phases. The rightward shift is visual representation of dopant migration, consistent with Fick's laws of diffusion[9]. These wafers can later be used in MOS capacitor fabrication and electrical characterization, where capacitance-voltage (C–V) behavior plays a vital role in analyzing oxide quality and interface state[10].

CONCLUSION

To determine the percentage difference between the calculated and experimental junction depths of the wafer after pre deposition and drive-in, the experiment was performed, with results being tabulated and displayed in a graph. The wafers were cleaned before the steps to get rid of organic and inorganic components and photoresists present on the wafer. Irvin's curves were used in finding experimental values. There were percentage errors over 30% in two cases due to presence of crystals and formation of native oxides on the wafers. There were also uncertainties in measuring sheet resistances using the four-point probe. To minimize presence of native oxides, HF dip could be

performed for longer period of time, or possibly multiple times. Better quality wafers could be used to reduce clustering and crystal defects. The four-point probe could be recalibrated before measurements of each step to improve measurement accuracy and reduce variability in junction depths. The wafers of this experiment could be used later in MOS capacitor fabrication and electrical characterization further in the semester.

References

1. Campbell, S. A. (2013). Fabrication Engineering at the Micro- and Nanoscale (4th ed.). Oxford University Press.

2. J. C. Irvin, "Resistivity of bulk silicon and of diffused layers in silicon," in The Bell System Technical Journal, vol. 41, no. 2, pp. 387-410, March 1962.

3. J. S. Christensen, H. H. Radamson, A. Yu. Kuznetsov, B. G. Svensson; Phosphorus and boron diffusion in silicon under equilibrium conditions. Appl. Phys. Lett. 7 April 2003; 82 (14): 2254–2256.

4. Wittel F., Dunham S. Diffusion of phosphorus in arsenic and boron doped silicon Appl. Phys. Lett. 66 (11), 1415 (1995)

5. Christensen, J.S.: Dopant diffusion in Si and SiGe ISRN KTH/FTE/FR-2004/2-SE, ISSN 0284-0545 KTH, Royal Institute of Technology, Department of Microelectronics and Information Technology Stockholm 2004.

6. M. L. Barry 1970 J. Electrochem. Soc. 117 1405

7. D. Mathiot, A. Lachiq, A. Slaoui, J.C. Muller, C. Dubois, “Phosphorus diffusion from a spin-on doped glass (SOD) source during rapid thermal annealing” Mater. Sci. Semicond. Process., 1(1998), pp. 231-236.

8. R.A. Colclaser, Microelectronics: Processing and Device Design, John Wiley & Sons, New York, 1980.

9.ScienceDirect Topics, Fick's Law, ScienceDirect, Elsevier, https://www.sciencedirect.com/topics/engineering/ficks-law (accessed October 30, 2024).

10. Sarker, J. (2025). Fabrication and Analysis of Metal-Oxide-Semiconductor Capacitors: Investigating C-V Characteristics for Varying Pad Sizes. September 2025. DOI: 10.21203/rs.3.rs-7669775/v1