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Fast growth of wafer-scale graphene on sapphire

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Fast growth of wafer-scale graphene on sapphire

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Abstract

Efficient growth of graphene over wafer-scale insulators is essential for fab-integration. Here we show that modulations of step architectures and atomic surfaces of c-plane sapphire allow fast graphene growth on 6" wafers (complete coverage in 10 mins), thus enabling batch synthesis to reduce production costs. We identify carbon capture at Al-rich surfaces and unidirectional flake emergence guided by step edges as the key elements leading to uniform graphene films. The growth quality of single-layer graphene is demonstrated by testing over 3300 top-gated device arrays on a 4" graphene/sapphire wafer, reaching mobility > 3000 $cm^2V^{-1}s^{-1}$. We use this to make white light-emitting diodes (LED) in an industrial production line, attaining~25% reduction in thermal resistance and~90% decrease in attenuation of light output power with respect to counterparts fabricated without graphene, during an accelerated aging test of 168 h at 85°C, equivalent to 1.8 years in normal room-temperature conditions. Our findings pave the way to transfer-free batch synthesis of high-quality graphene wafers.

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Introduction

Graphene is ideally suited for a variety of wafer-scale (opto)electronic applications[1-5] and it is progressing towards fab-level integration[2]. Most approaches to date require transfer after growth on a Cu covered substrate[6], however, the ultimate goal is to achieve direct growth via chemical vapor deposition (CVD) over target insulators, thus avoiding the transfer process[7]. In contrast to metals[8-10], the decomposition of carbon precursors and the migration of carbon species need to surmount 3–10 times higher energy barriers[11, 12], owing to the lack of catalytic activity on insulators[13], resulting in random domain orientations[14] and uncontrollable layer thickness[14]. This is a bottleneck for scaling-up device processing at a wafer level.

The ability to grow layered materials (LMs) on wafer scale holds transformative potential for next-generation electronics[3, 15, 16], optoelectronics[3, 17] and photonics[2, 3, 17], particularly for semiconductor technology nodes into the sub-nm regime[18]. A critical bottleneck remains in attaining large-area (≥ 4”), single-crystalline LMs on insulating substrates[19], with spatial homogeneity, due to grain boundaries and adlayers[20]. Leading semiconductor companies have prioritized LM integration in their roadmaps[21-24] yet scalable synthesis of high carrier mobility LMs, e.g. ≥ 1000 $cm^2V^{-1}s^{-1}$ for 4’’-sized SLG directly grown on sapphire, has not been achieved yet.

Single-crystalline c-plane sapphire is the substrate of choice for wafer-scale LM growth due to its lattice compatibility[22], atomic-level surface flatness[22], and thermal/chemical stability[22]. As-synthesized TMDs[25, 26] and single layer graphene (SLG)[27] on sapphire have superior crystallinity and uniformity compared to those grown on Si[28, 29], Si_3N_4[30], and SiC[31, 32] (commonly used in CMOS processes[30]). SLG can be used to enhance the performance of LEDs[33] by acting as buffer layer to guide the crystallographic alignment of III-nitride semiconductors[34] on sapphire. SLG is also promising in solving the problem of heat dissipation for LED applications[35], thanks to its high thermal conductivity[36, 37]. LEDs fabricated on sapphire using a vertically oriented SLG buffer were reported with~37% improved light output power and~3.8% temperature reduction with respect those without graphene[37]. However, the effect of SLG in improving heat dissipation for wafer-scale (≥ 2”) LED devices has not investigated yet. The application of wafer-scale CVD SLG/sapphire in industrial production lines of LEDs has not been demonstrated yet.

The co-optimization of scale-cost-performance for SLG growth on sapphire faces obstacles, including (Table 1): (i) Slow growth rates (0.07 – 2 μm/h), with 4–15 h needed to fully cover one 2”-4” wafer[28, 38-40]. (ii) Trade-offs between size and quality: The size of SLG with I(D)/I(G)≤ 0.1 on a sapphire is ≤ 2”[27]. (iii) Limited understanding of growth mechanism. Step edges and/or atomic terraces of sapphire were used to guide the controllable production of TMDs[18, 25, 26], yet remain unexplored for SLG growth[27, 39, 41, 42]. The role of Al-rich surface configurations as catalytic promotor in aiding SLG formation is unexplored[27, 39, 41, 42].

A few strategies[27, 29, 39, 43, 44] have been developed to optimize SLG growth and realize wafer-scale synthesis on insulating substrates, especially sapphire[27, 39, 44], which combines high thermal stability (maintaining crystal lattice integrity at ~2000 °C)[45], lattice symmetry compatibility with SLG[46], and broad availability in semiconductor manufacturing[47, 48]. Surface reconstruction *via* pre-H_2-etching was proposed[39] to grow 4” SLG at 1200°C, but without the availability of batch production compatible with industrial lines. Surface metallization by fusing Cu foils over Al_2O_3(0001) was used for 2’’ wafer-scale SLG growth by multi-cycled CVD[27]. However, Ref.27 did not report data on possible metal contamination stemming from the Cu foil. The parameter control was laborious because of the ~25 h annealing period, and the throughput low (1 piece at a time) compared to traditional[49] CVD growth (>

10 pieces at a time), limiting industrial uptake[27]. Ref.44 showed that increasing the temperature from 1100 to 1400°C by using electromagnetic induction heating CVD resulted in 2" SLG/sapphire wafers with sheet resistance (R_s) = 587 ± 40 ohms/□[44]. However, the combination of I(D)/I(G) < 0.1, high production efficiency (complete coverage within 60 mins), 4" or larger wafer size, remains to be demonstrated.

Here, we present a co-modulation strategy that leverages atomic terraces and step architectures of c-plane sapphire to enable the fast growth of SLG on 6" wafers with I(D)/(I(G)<0.05. The growth rate reaches~140 μm h^{-1}, with 6" wafers entirely covered within 10 mins. This translates to a production efficiency (growth time for one 6" wafer) 10 to 10000 times higher than previous reports[27, 39, 50]. Carbon capture at the Al-rich surface and unidirectional flake emergence guided by step edges are identified as dual drivers for the high-speed, high-quality growth of uniform SLG films. The formation of step-edges and the atomic-surface controls the nucleation and enlargement of SLG domains on sapphire. This contrasts previous reports claiming that the Al-terminated atomic-surface configuration is the dominant factor controlling SLG nucleation orientation[27, 39, 42, 44]. The size of the SLG/sapphire wafers can be readily extended to 8" and 12".

By using HfO_2 (20 nm thick) prepared *via* low-temperature (200 °C) atomic layer deposition (ALD) as dielectric layer, we fabricate>3300 top-gated devices on 4" SLG/sapphire. These have an average room temperature mobility μ> 1000 $cm^2V^{-1}s^{-1}$ and a maximum μ> 3000 $cm^2V^{-1}s^{-1}$, surpassing previous results for transfer-free SLG devices in terms of scalability (430-1720% larger)[29, 51].

SLG grown on stepped sapphire also facilitates the nucleation of AlN domains, enabling their faster (200%) coalescence into void-free films. We grow GaN on 4'' AlN/SLG/sapphire using the industrial GaN-based LED production line of Hangzhou Silan Microelectronics[52], where white LED device arrays are fabricated[52]. In comparison with commercial GaN-based white LEDs on sapphire without SLG, our SLG-based LEDs show~25% reduction in thermal resistance and~90% decrease in the attenuation of the light output power during an aging test of 168 h. Our findings pave the way to transfer-free batch synthesis of high-quality graphene wafers.

Graphene growth on c-plane sapphire

SLG growth is carried out using an electromagnetic induction heating cold-wall CVD system, as shown in **Fig. 1a**. A graphite carrier is heated by an alternating magnetic field generated by an induction coil. The growth temperature (T) is monitored by a pyrometer, and the pressure is adjustable *via* a closed-loop control. 4" or 6" c-plane sapphire (Unionlight Technology Co., Ltd.) is placed on the graphite carrier. The substrate is then heated to ~1400°C under a mixture of H_2 (500 sccm) and Ar (1000 sccm) at 2000 Pa, and stabilized for 15-30 mins. CH_4 (100 sccm) is then introduced as the carbon precursor. After a set growth duration, the system is cooled to room temperature (RT) under the Ar and H_2 mixture.

Substrate engineering by pretreatment plays a major role in synthesizing high-quality (I(D)/I(G) < 0.1) SLG crystals[19, 53]. Using a c-plane (0001) sapphire with a small misorientation angle (~0.2°)[54], controlled thermal annealing under elevated T~1400°C in vacuum enables the formation of ordered step edges and terraces (**Supplementary Fig. 1 and 2**) with a (0001) surface without discernible reconstructions (**Supplementary Figs. 3 and 4**). Surface lattice oxygen is prone to be lost[39], resulting in an Al-rich surface. This boosts the dissociation of the precursor molecules and the unidirectional growth of SLG domains, which ultimately give rise to a complete SLG film (**Fig. 1b**). To achieve Al-rich flat terraces and regular step edges, a cold-wall apparatus is used, where the substrate is directly

placed over a graphite carrier to allow heating. The growth parameter space is enhanced compared to typical CVD reactors[27, 29, 39, 55], enabling T~1400°C in 10 min, over 10 times faster than hot-wall reactors[49]. Upon delivery of CH_4, SLG wafer-coverage is achieved in 10 min. This can be extended to 6" wafers (**Fig. 1c**). To demonstrate wafer-scale synthesis with stable batch productivity, the growth experiments are carried 11 times. The resulting 4" SLG/sapphire wafers exhibit inter-batch and intra-wafer uniformity, as shown in **Fig. 1c**.

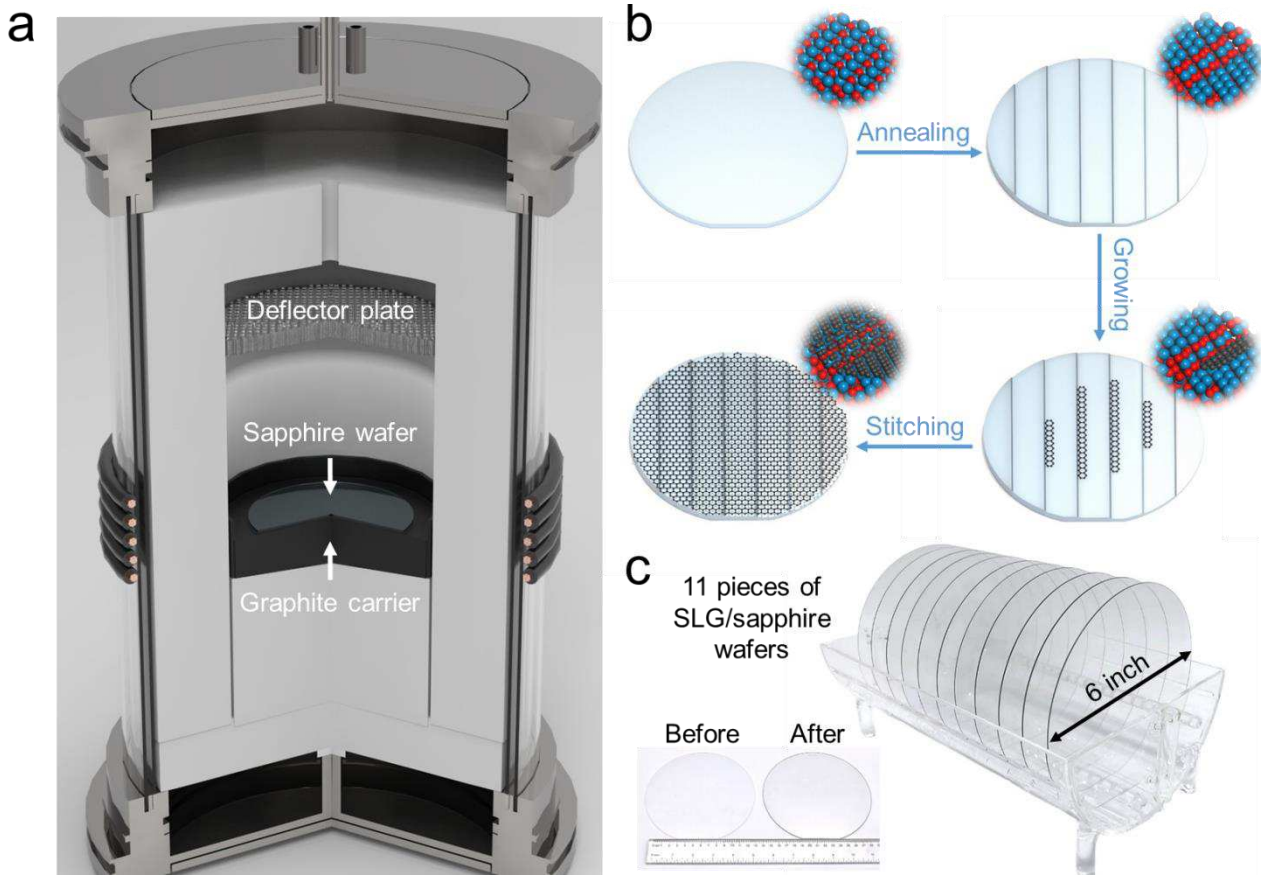

Fig. 1. Synthetic strategy. a, Schematic of direct growth of SLG on annealed sapphire wafer. **b**, Schematic of CVD reactor equipped with a gas distribution plate, with the substrate placed on a graphite carrier. **c**, Photograph of synthesized 6" SLG/sapphire wafers. The inset shows photographs of the sapphire wafer before (left) and after (right) SLG growth.

A uniform distribution of gaseous precursors is the key to the macroscopic homogeneity of SLG at a wafer scale. In our system, a gas distribution plate is incorporated beneath the gas inlet, designed to aid the even dispersion of gas flows prior to reaching the substrate. **Supplementary Fig. 5** reports the simulations of the gas flow field with/without the presence of plate. **Fig. 2a** suggests that the porous structure of the plate guides the gas flow into a uniformly dispersed form, covering the whole 6'' substrate carrier, mitigating any dead zones without gas covered, leading to an even distribution of gas across the substrate. The reduction from ~0.31 (± 0.07) to ~0.28 (± 0.02) mm s^{-1} in flow velocity caused by the plate also helps diminish the generation of turbulence flow within the chamber.

Fig. 2b presents optical transparency (measured by UV-vis transmittance spectroscopy, Perkin-Elmer Lambda 950) and R_s (measured by four-probe system, ResMap 178) of 5 representative samples. The transmittance at 550 nm for each 4" SLG/sapphire assessed across 30 points is~97.4-97.8%, consistent with the 2.3% optical absorbance of SLG[56]. The wafer-level R_s distribution is narrow

(standard deviation~2.37-4.15%), with average<600 ohms □$^{-1}$ without any treatment.

Fig. 2c and **Table 1** compare our approach with other transfer-free CVD synthesis on sapphire[27, 39], quartz[38, 57], SiO_2/Si[28, 29] and h-BN[13, 40], in terms of growth rate, batch time, I(D)/I(G), domain size and SLG coverage. Our approach enables one or two orders of magnitude faster wafer-level synthesis, while maintaining crystallinity and coverage, with domain size>40μm, paving the way for fab-level electronic/optoelectronic device production.

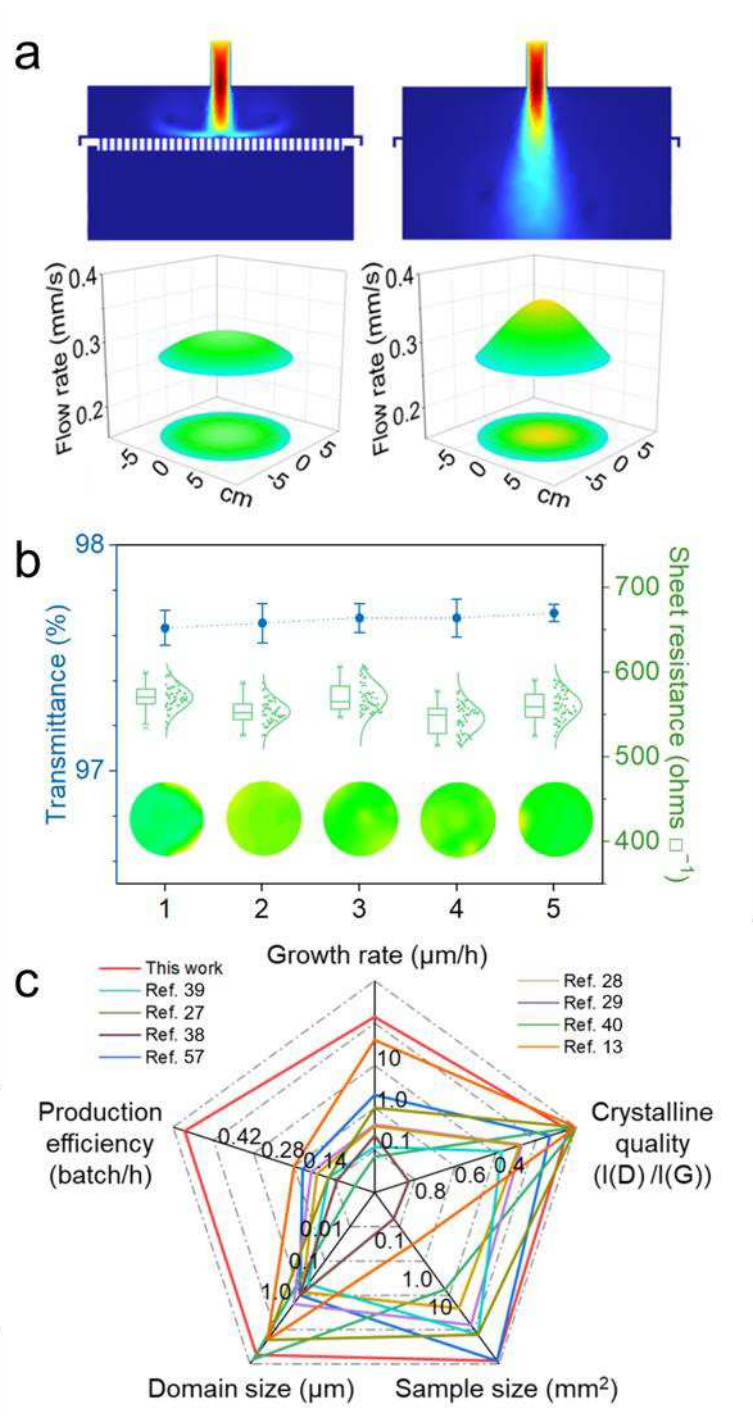

Fig. 2. Wafer-scale synthesis. a, Simulation of gas distribution within the CVD chamber (1400°C; 3000 Pa) (top panel) and 3d color maps of flow velocity over the graphite carrier surface (bottom panel). **b**, R_s maps and visible light transmittance statistics of 5 representatives 4" SLG/sapphire

wafers from adjacent batches (30 data points per sample). **c**, Comparison of our approach and other direct CVD routes in terms of growth rate, I(D)/I(G), sample size, domain size, batch/h[13, 27-29, 38-40, 57].

Table 1. Growth rate, batch/h, I(D)/I(G), domain size, sample size, carrier mobility and Rs reported here in in previous SLG grown on dielectric substrates.

Refs.	Substrate	Growth rate (μm/h)	Batch/h	I(D)/I(G)	Excitation wavelength	Domain size (μm)	Maximum sample size	Carrier mobility at RT ($cm^2V^{-1}s^{-1}$)	Rs ($\Omega\ \square^{-1}$)	Applications
This work	Sapphire	140	1.5-3	0.04	514 nm	42	6''	>3,000	<600	Transistors; transparent electrodes, LED, microelectronics
[39]	Sapphire	0.9-2	4-7	0.13	532 nm	~1	6''	2,260*	~1,100	
[27]	Sapphire	~0.07	~13.8	/	532 nm	~74	2''	Electron: 7,400* Hole: 8,600*	/	
[38]	Quartz	0.13-0.4	4.5-13.5	0.27	514 nm	1.8	6 × 10 cm^2	/	~900	Optical modulators, THz wave devices, chemical sensors
[57]	Quartz	0.12-0.37	5-11	0.28	/	0.7-0.8	60 × 60 mm^2	/	/	
[28]	SiO_2/Si	~0.12	6-10	0.37	532 nm	~0.47	4''	15,773†	1,409	CMOS compatible devices, MEMS/NEMS devices
[29]	SiO_2/Si	0.22	7.5	0.83	633 nm	1	1.5 × 1.5 cm^2	1,510	/	
[40]	h-BN	1	6	/	514 nm	20	4''	/	/	Quantum devices, spintronic devices
[13]	h-BN	40	3.5-5	/	488/532/633 nm	20	< 1''	Electron: 23,000* Hole: 19,000*	/	

*Device fabricated after SLG transfer onto SiO_2/Si, †electrolyte-gated device.

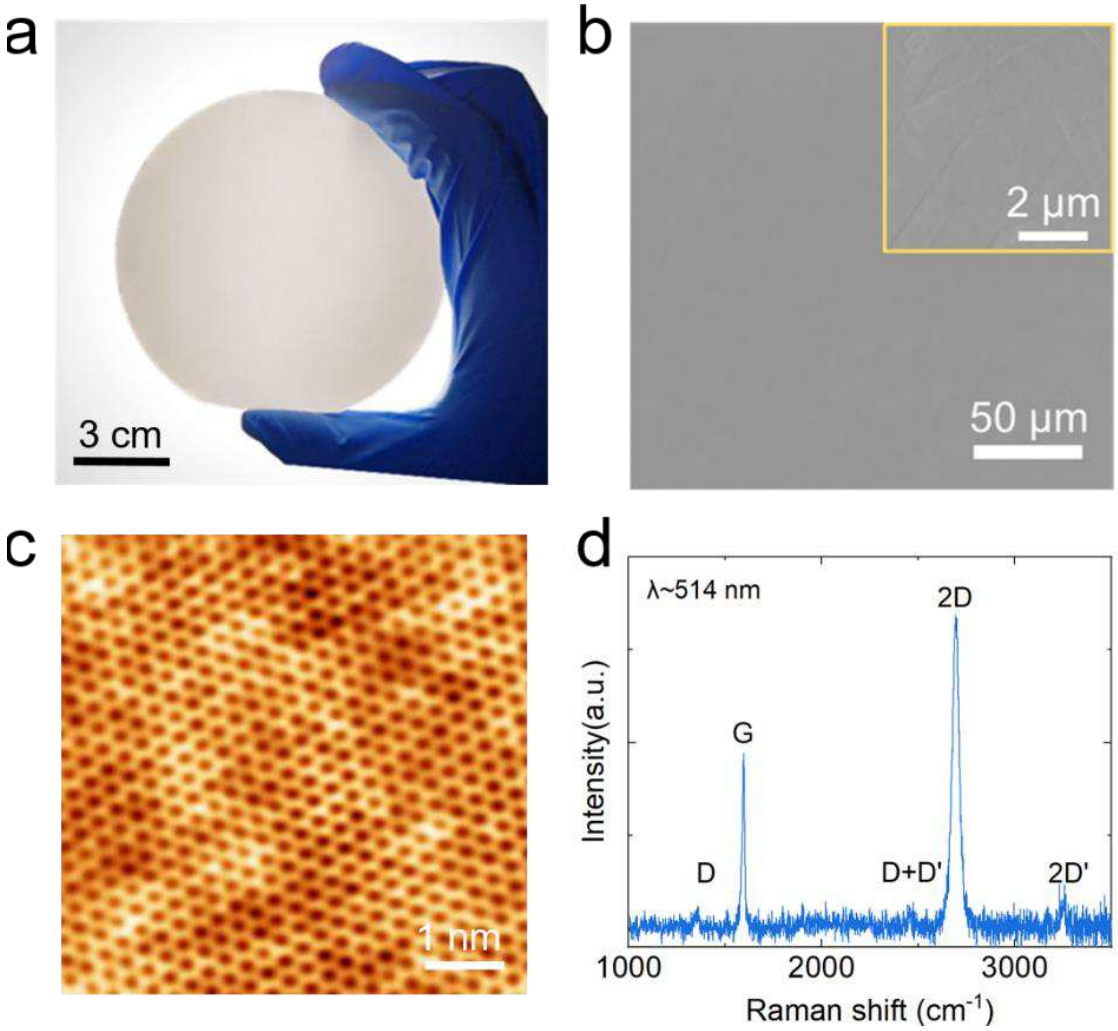

Fig. 3. Characterization. a, Photograph of 4" SLG/sapphire wafer. **b**, SEM image of SLG on sapphire. **c**, STM image of SLG, displaying a continuous honeycomb lattice. **d**, Representative Raman spectrum of as-grown SLG on sapphire

Characterization

The elevated T = 1400°C in the cold-wall CVD system enhances the efficiency of CH_4 decomposition and the migration of active carbon species[58, 59]. Under an optimized growth window (1400°C, 3000 Pa, 1000 sccm Ar, 500 sccm H_2, 100 sccm CH_4), continuous SLG film can be synthesized on 4" sapphire wafers within 10 mins, **Fig. 3a**. There is no observable breakage in SEM images (**Fig. 3b**). This is also shown by the atomic force microscopy (AFM, Bruker Dimension Icon) characterization in **Supplementary Fig. 6**. Scanning tunneling microscopy (STM, Omicron VT-STM/STS 330 system) resolves the SLG hexagonal honeycomb lattice (**Fig. 3c**). The grown surface is devoid of contaminant, as confirmed by X-ray photoelectron spectroscopy inspection (Kratos Analytical Axis Ultra spectrometer using a monochromatic Al Kα x-ray source) (**Supplem. Fig. 7**).

To transfer SLG, the sample is spin-coated by poly (methyl methacrylate) (PMMA 950K A4) and then the sapphire is etched using a 10% mass capacity NaOH solution. After that, PMMA/SLG is placed on SiO_2/Si and dried. Acetone is then used to remove the PMMA.

The optical microscopy (OM, Olympus DX51) image upon transfer from sapphire onto SiO_2/Si shows lack of contrast variations, indicative of full coverage SLG (**Supplementary Fig. 8**). Cross-

sectional transmission electron microscopy (TEM, FEI Tecnai F20; operating at 200 kV) corroborates uniform SLG formation (**Supplementary Fig. 9**). A step edge (2.7 nm in height) and the continuous coverage of the SLG on sapphire are also revealed by cross-sectional TEM (Nion U-HERMES 200; at 60 kV), with more details in **Supplementary Fig. 10**.

As-grown SLG is characterized by Raman spectroscopy with a Renishaw InVia spectrometer equipped with 100x objective at 514.5 nm. 63 spectra are collected from SLG/sapphire to estimate doping and defect density. The errors are calculated from the standard deviation across different spectra, the spectrometer resolution (~1 cm^{-1}) and the uncertainty associated with the different methods to estimate the doping from full width at half maximum of G-peak, FWHM(G), intensity and area ratios of 2D and G peaks, I(2D)/I(G), A(2D)/A(G). **Supplementary Table 1** summarizes the Raman peaks fits, E_F, charge carrier density n and defects density n_D. E_F is derived from A(2D)/A(G), I(2D)/I(G) and FWHM(G)[60-62]. First, n is derived from A(2D)/A(G), I(2D)/I(G) and FWHM(G) for each spectrum as for Refs.[61, 62].

The strain is derived from Pos(G)[63, 64]. Since Pos(G) depends on both E_F and strain, we first derive E_F from A(2D)/A(G), I(2D)/I(G) and FWHM(G), which are independent of strain[60-62], and then calculate Pos(G) corresponding to this E_F. The strain is then retrieved from the difference between the experimental and calculated Pos(G): $\left[\mathrm{Pos(G)}_{calc} - \mathrm{Pos(G)}_{exp}\right]/\Delta\mathrm{Pos(G)}$, with ΔPos(G) ~23 cm^{-1}/% for uniaxial strain[63] and ~60 cm^{-1}/% for biaxial strain[63]. n_D is derived from I(D)/I(G) for a specific E_F, using $\mathrm{n}_D = (2.7 \pm 0.8) \times 10^{10}\mathrm{E}_L^4\ [\mathrm{eV}]\mathrm{I(D)/I(G)E}_F(\mathrm{eV})^{(0.54\pm0.04)}$[62]. The Raman spectrum of as-grown SLG is in **Fig. 3d**. The 2D peak is a single-Lorentzian with FWHM(2D) = 29 ± 1 cm^{-1}, Pos(G) = 1588 ± 1 cm^{-1}, FWHM(G)= 16 ± 2 cm^{-1}, Pos(2D) = 2693 ± 1 cm^{-1}, I(2D)/I(G) = 5.6 ± 0.9 and A(2D)/A(G) = 10.2 ± 1.3, indicating a p-doping with E_F= 210 ± 75 meV[61, 62] . I(D)/I(G) = 0.01 ± 0.05 corresponds to n_D ~ 5.8 ± 2.0 × 10^{10} [62] for 2.41 eV excitation. Biaxial strain can be differentiated from uniaxial by the absence of G-peak splitting with increasing strain, however at low (≤0.5%) strain the splitting cannot be resolved. For uniaxial (biaxial) strain, Pos(G) depends on both E_F and strain[61, 63]. To obtain the contribution of strain only, we first derive E_F from A(2D)/A(G), I(2D)/I(G) and FWHM(G), which are independent of strain[60-62], and then calculate Pos(G) corresponding to this E_F. The strain is then retrieved from the difference between the experimental and calculated Pos (G), with biaxial strain = 0.07 ± 0.02% and uniaxial strain = 0.18 ± 0.04%.

To further evaluate the quality and uniformity of our SLG films, we prepare 3328 SLG top-gated field effect transistor (GFET) arrays on a 4" SLG/sapphire wafer (**Fig. 4a**). We use electron beam lithography (EBPG 5200, Raith GMBH) with double-layer PMMA (kayakuAM) as resist. 495k PMMA A2 and 950k PMMA A4 are spin-coated onto SLG/sapphire, both using 1 krpm rate, followed by baking at 120°C for 5 min. AR-PC (Allresist, Electra 92) is then used to enhance electrical conductivity of SLG/sapphire (4 krpm, 60°C bake for 2 min). Electrode materials, Au and Cr, are deposited by thermal evaporation (MiniLab 60, Moorfield Nanotechnology Ltd) at 1.0 and 0.4 nm/s, respectively under a high vacuum (10^{-7} - 10^{-6} torr). The SLG channels are patterned using oxygen plasma etching (3 W, 75 sccm, 10^{-5} Torr, 30 s) (NanoEtch, Moorfield Nanotechnology Ltd). HfO_2 is deposited atop the SLG channel at 130°C using thermal atomic layer deposition (Fiji, Veeco) as top gate dielectric. The devices are measured using a Cascade Probe Station and Parameter Analyzer at RT in air by applying a constant drain current (50 μA) and sweeping V_G from −5 to 5 V. To exclude contact resistance on calculating carrier mobility, four-probe measurements (CDE ResMap 178) are performed[10,11].

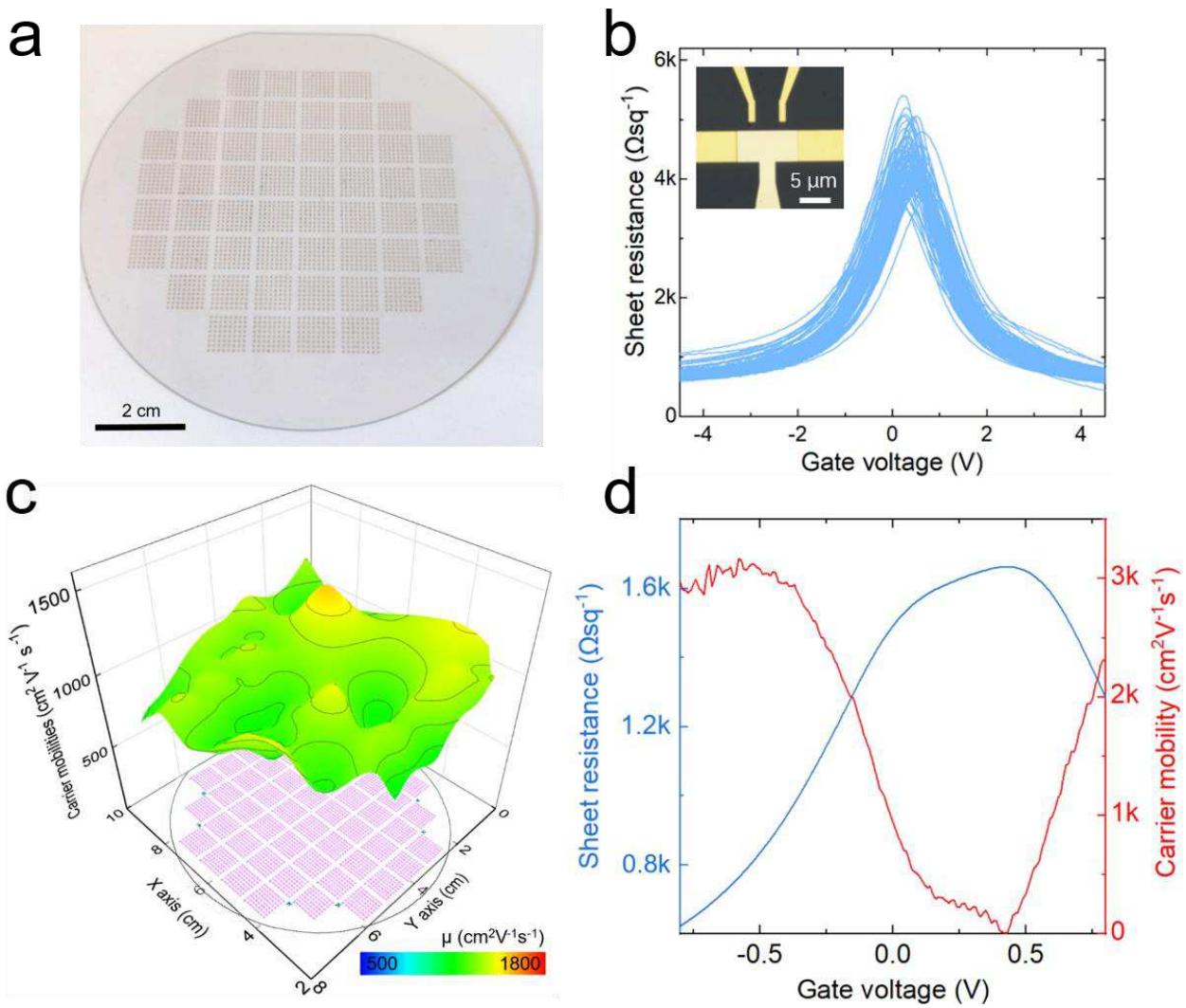

Fig. 4. Transport properties. **a**, Photograph of top-gated SLG device array based on 4" SLG/sapphire. The inset shows OM image of a top-gated SLG device. **b**, Transfer curves of 100 GFETs. **c**, Color map of μ distribution over a 4" wafer. **d**, Representative gate-dependent Rs and μ.

A zoomed-in OM image of device arrays is in **Supplementary Fig. 11**. Both length (L) and width (W) of the SLG channels are 5 μm (**Fig. 4b**, Inset). **Fig. 4b** plots the resistivity [$\rho = (W*V_{12})/(I_{sd}*L)$] of 100 SLG devices as a function of V_G. μ is extracted using the direct transconductance method as $\mu = [L*(\partial I_{sd}/\partial V_G)]/(V_{12}*C*W)$, where C is the back gate capacitance, calculated using the relative permittivity (~10.5) of 20 nm thick HfO_2, estimated fabricating dual-gated SLG devices on SiO_2/Si (**Supplementary Fig. 12**)[65, 66]. **Supplementary Fig. 13** provides statistical results of RT, ambient-air μ of 100 GFETs fabricated in one batch. >99% devices have μ>1,000 $cm^2V^{-1}s^{-1}$, with average μ~1298 (± 135) $cm^2V^{-1}s^{-1}$. **Fig. 4c** summarizes the mapping of GFETs on 4" sapphire. **Fig. 4d** shows a GFET with μ >3000 $cm^2V^{-1}s^{-1}$, outperforming previous transfer-free GFETs without h-BN encapsulation[67].

Growth mechanism

To gain further insights into the role of step structures in SLG growth, first-principles calculations based on density functional theory (DFT) are performed to investigate the optimal orientation of SLG domains on sapphire (**Supplementary Fig. 14**). The adsorption of $C_{24}H_{12}$, considered as nucleation seed[44, 68], at a step edge site is simulated with cluster edges passivated by H atoms to avoid any edge

effects. The SLG armchair edge is designated as 0° when parallel to the armchair edge of the sapphire substrate. The cluster is then rotated from 0° to ± 30° at 5° intervals (**Fig. 5a and Supplementary Fig. 15**). Our calculations indicate that $C_{24}H_{12}$ has a minimum energy configuration at a vector angle of 0°, ~0.06 eV lower than −30° and 30° configurations (**Fig. 5b**), suggesting stable orientation of SLG guided *via* sapphire step edges.

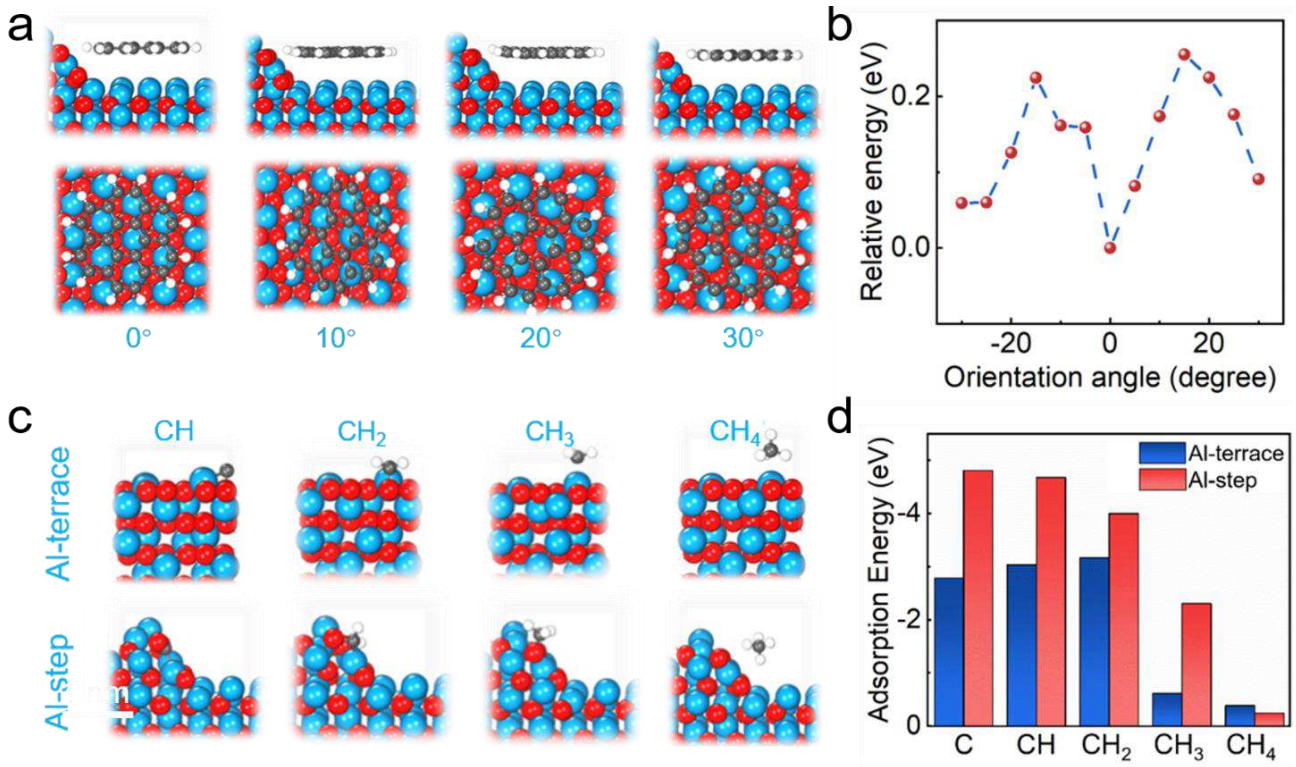

Fig. 5. Mechanistic insight into co-manipulation growth. a, Relaxation structures of $C_{24}H_{12}$ cluster adsorbed on the steps of Al_2O_3 (0001) with rotation angles of 0, 10, 20, 30°. **b**, Relative (referenced to 0°) energies of $C_{24}H_{12}$ clusters adsorbed at different rotation angles. **c**, Optimized structures for CH, CH_2 CH_3 and CH_4 adsorbed on Al-terrace (upper panel) and Al-step (lower panel). **d**, Calculated adsorption energy of CH_x (x = 0-4) on Al-terrace and Al-step surfaces. Al and O atoms are represented by blue and red balls, respectively.

The Al_2O_3 (0001) surface has been confirmed to exhibit Al termination under high-T conditions[44, 69]. Models of Al-terrace and Al-step were constructed to investigate the adsorption behavior of carbon species during the initial stages of SLG growth. An Al-rich surface might favor the decomposition of carbon sources, because Al sites are strong Lewis acids that dissociate CH_4 molecules[39], thus SLG growth. To probe the catalytic effect of the Al-rich surface, we calculate the adsorption energies of carbon species (CH_x, x = 0-4) on both Al-terrace and Al-step of the c-plane sapphire (**Fig. 5c**). A plane-wave cutoff energy of 400 eV is used, and the Brillouin zone is sampled using a 3×3×1 Monkhorst-Pack k-point grids for structure relaxations. As for **Fig. 5d**, the adsorption energy (E_{ads}) remains negative, indicating that Al-rich surfaces favor the capture of carbon species. The negative E_{ads} for Al-steps are larger than for Al-terraces, suggesting that carbon species are more likely to adsorb at Al-steps for nucleation.

Our computational model considers a $C_{24}H_{12}$ cluster on an Al-step, with armchair edges parallel to those of sapphire. The adsorption energies of carbon atoms incorporated at 4 inequivalent positions

are calculated to investigate the propagation process of SLG edges along the steps. As depicted in **Supplementary Figs. 16 and 17**, the adsorption energy for carbon atoms attached along the steps (sites 1 and 4) is lower. SLG domains are prone to expand along the direction of the steps, in good agreement with **Supplementary Fig. 18**. Collectively, our theoretical and experimental results demonstrate the growth benefits from synergistic modulations of step architectures and Al-rich surface features. This implies equal importance of terraces and edges.

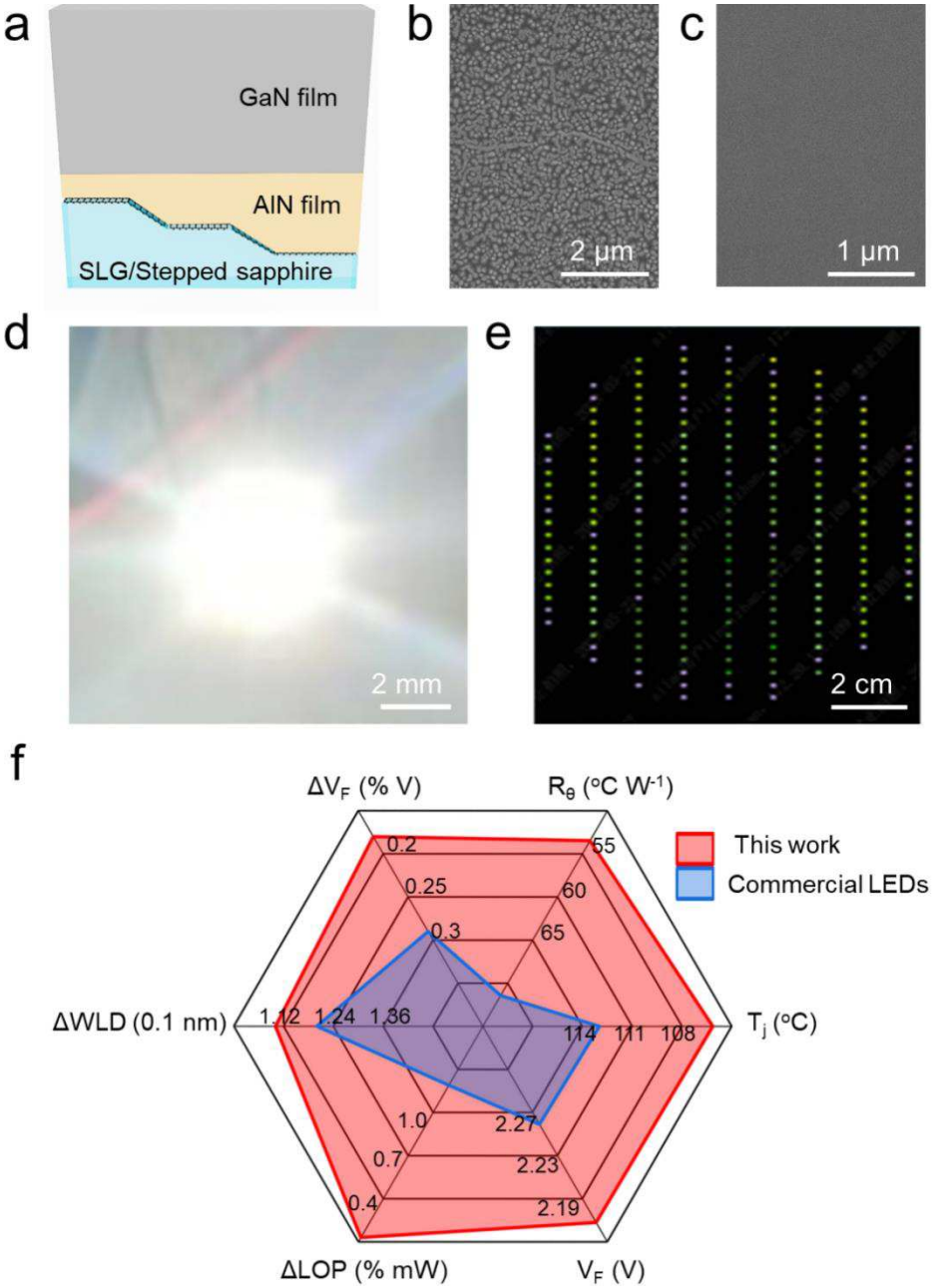

Fig. 6. LED application. a, Schematic illustration of epitaxial growth of AlN on stepped sapphires wafers without and with SLG. **b**,**c**, SEM images of (b) AlN domains and (c) continuous films on SLG/sapphire. **d**, Photograph of white LED fabricated using GaN/AlN/SLG/sapphire. **e**, Light-up yield of SLG-based white LEDs on a 4'' wafer. **f**, Comparison of our LEDs with commercial ones in terms of thermal resistance (heat dissipation capability), junction T (T of the PN junction inside the LED), forward voltage (the voltage required during LED operation), and aging test performance (device stability under prolonged operation or in high-T environment).

Our SLG/sapphire samples can be used for remote epitaxy of III-nitride semiconductors, for which size[70] (wafer scale, ⩾2'') and efficiency[71] (time required to form continuous films) are important. Taking AlN, a wide (4.7-6.3 eV)-bandgap[72] group III nitride material[73], as an example, previous works claimed that 1 h[74, 75] is required to get continuous films and 2 h[76] for 2''-sized AlN/SLG/sapphire wafer. Our SLG/sapphire promotes both nucleation and growth rates of AlN domains (**Figs. 6a and 6b**) in comparison to the as-purchased commercial sapphire (Unionlight Technology Co., Ltd.), without degrading the crystallinity of the AlN film (**Supplementary Figs. 19−21**). The presence of atomic steps in our SLG/sapphire not only increases the AlN nucleation density (number of AlN domains per μm^2) from 26 μm^{-2} on commercial sapphire to 62 μm^{-2} on our SLG/sapphire substrates, but also facilitates faster (200% in comparison to sapphire without SLG and Refs.[75, 76]) formation of void-free films, enabling complete 2" wafer coverage within 0.5 h (**Fig. 6c**).

After the formation of continuous AlN film on SLG/sapphire, we used the production line of Hangzhou Silan Microelectronics[52] for landscape lighting to deposit GaN films by metal organic CVD on it and then produce SLG-based white LEDs by replacing their sapphire wafers with our SLG/sapphire, without changing other parameters, such as deposition T and flow rate[77].

One of the lighting white LED is shown in **Fig. 6d**. Performance tests of both commercial LEDs and our SLG-based white LEDs are conducted to compare their lighting yield (ratio of working devices in one batch based on electroluminescence test), thermal resistance (R_θ), forwards voltage (V_F), and junction temperature (T_j) (**Fig. 6e**). An aging test is conducted under 200 mA for 168 h by monitoring the attenuation of the light output power (△LOP), drift of V_F (ΔV_F), and shift of emission wavelength (ΔWLD). For each group of experimental conditions, 10 LED devices are tested, and the mean is used as the benchmark for performance evaluation to ensure statistical significance. Our SLG-based LEDs exhibit a 25% reduction in R_θ (53.47 *vs.* 71.42 $^oCW^{-1}$), 6% decrease in T_j (106.14 *vs.* 112.975 ^oC), 4% drop in forward voltage (2.168 *vs.* 2.259 V), together with~90% decrease in △LOP (0.13% *vs.* 1.19% mW), 8.33% decrease in △WLD (0.11 nm *vs.* 0.12 nm) and 37.93% decrease in ΔV_F (0.18% *vs.* 0.29% V) (**Fig. 6f**), with their lighting yield (75%) 7% smaller than commercial white LEDs (82%). This can be attributed to SLG thermal conductivity[36, 78] and indicate the potential of our SLG/sapphire wafers for commercialization, especially when stability and lifetime of LEDs are concerned.

Conclusions

We reported the fast growth of 4''and 6'' high-quality (I(D)/I(G) < 0.1) SLG on c-plane sapphire. The co-manipulation of step edge formation and atomic surface configuration under elevated T=1400 °C is a key requirement for successful preparation of wafer-sized continuous SLG, reducing the per-batch processing time by one to two orders of magnitude compared to previous reports[27-29].

Methods

Density functional theory. All the calculations are performed by using DFT methods implemented in the Vienna *ab initio* simulation package[79]. The exchange-correlation effects and electron-nuclei interactions are described by the Perdew-burke-Ernzerhof scheme[80], within the general gradient approximation and the projector augmented wave method, respectively[81]. To avoid interactions between two adjacent images, a vacuum space of at least 15 Å is chosen between the images. The convergence threshold for the self-consistent field is set at 10^{-4} eV for the total energy change and 0.02 eV/Å for the maximum forces on atoms. As for the model of SLG clusters on stepped sapphire, the calculations employ a plane-wave cutoff energy of 400 eV and a 1×1×1 Monkhorst-Pack[82] k-point

grid to sample the Brillouin zone for structural relaxation[79]. To avoid interactions between two adjacent images, a vacuum space of at least 10 Å is chosen. The convergence threshold for the self-consistent field is set at 10^{-3} eV for the total energy change and 0.5 eV/Å for the maximum force on atoms. To provide more accurate data, a van der Waals DFT-D2 method based on the exchange-correlation function is used[83]. The binding energy (E_b) between adsorbent molecules and surface is defined as the energy difference between the adsorption system ($E_{complex}$) and the sum of pure surface ($E_{surface}$) and pure adsorbent molecules (E_{abs}): $E_b = E_{complex} - (E_{surface} + E_{abs})$. The lower adsorption energy indicates the more stable state.

COMSOL Multiphysics simulation. We use transient computation[84] to model the pressure and velocity fields over a duration of 2 s with a time step of 0.2 s. The GMRES solver[85] is employed, configured with a residual tolerance of 0.01 and a maximum of 100 iterations, using a 5-level multigrid approach for smoothing aggregation. Default settings are maintained for the number of iterations and degrees of freedom, and the PARDISO direct solver[86] is used for coarsening with default settings. The meshing for the air domain is carried out using free tetrahedral meshes, with refinements at cavities and chamfers (locally finer mesh near geometric features). The mesh for the domain with a gas distribution disk consists of 1,068,923 elements, averaging a quality score (mean of element-wise shape metrics over the entire mesh[87]) of 0.8085, while the mesh without the disk comprises 316,841 elements with an average quality of 0.8628. We use a transient compressible laminar flow model[87], with governing equations for momentum and mass conservation as follows[87]:

$$\rho\frac{\partial \mathbf{u}}{\partial t} + \rho(\mathbf{u}\cdot\nabla)\mathbf{u} = \nabla\cdot\left[-p\mathbf{I} + \mathbf{K}\right] + \mathbf{F} \tag{1}$$

$$\frac{\partial \rho}{\partial t} + \nabla\cdot(\rho\mathbf{u}) = 0 \tag{2}$$

where ρ is the density (kg/m^3), $\mathbf{u}$ is the velocity vector (m/s), p is the pressure (pa), K is the viscous stress tensor (pa), and F is the gravity acceleration (N/m^3). The gas properties equation is as follows[88]:

$$\rho\frac{\partial \mathbf{u}}{\partial t} + \rho(\mathbf{u}\cdot\nabla)\mathbf{u} = \nabla\cdot\left[-p\mathbf{I} + \mathbf{K}\right] + \mathbf{F} \tag{3}$$

$$\frac{\partial \rho}{\partial t} + \nabla\cdot(\rho\mathbf{u}) = 0 \tag{4}$$

$$\mathbf{K} = \mu\left(\nabla\mathbf{u} + (\nabla\mathbf{u})^{\mathrm{T}}\right) - \frac{2}{3}\mu(\nabla\cdot\mathbf{u})\mathbf{I} \tag{5}$$

where I is the identity tensor. The inlet boundary condition is defined as a mass flow, with[89]:

$$-\int_{\partial\Omega}\frac{\rho}{\rho_{\mathrm{st}}}(\mathbf{u}\cdot\mathbf{n})d_{\mathrm{bc}}\mathrm{d}S = Q_{\mathrm{sccm}},\ \ \rho_{\mathrm{st}} = \frac{P_{\mathrm{st}}M_{\mathrm{n}}}{RT_{\mathrm{st}}} \tag{S6}$$

where sccm represents the standard flow rate, P_{st} is the standard pressure, and T_{st} is the standard temperature. Specifically, Q_{sccm} is 1600 sccm, P_{st} is 3000 Pa, and T_{st} is 1400 °C.

The outlet boundary condition is defined as a pressure exit[90]:

$$\mathbf{u}\cdot\mathbf{t}=0,\ P_{\text{inl}}:\ p_{\text{av}}=\frac{1}{A}\int_{\partial\Omega_{\text{out}}}pdS,\ A=\int_{\partial\Omega_{\text{out}}}dS \tag{S7}$$

where P_{av} is the average pressure.

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Author contributions

J. Sun, J.Z. and Z.L. designed the concept. Y.L., M.W., J. Shan, K.Z., Z.X., L.J., W.W., Z.C. performed the sample growth. F.X. and W.Z. conducted the theoretical calculations. B.L. and P.G. performed the TEM characterizations. C.X. and Y.Z. carried out the STM measurements. Y.G. and T.W. performed the AlN growth and fabricated the LED device. J.Z. C.W. and A.C.F. performed the Raman analysis and electrical measurements. Y.L., F.X., W.Z., J. Sun, J.Z., A.C.F. and Z.L. co-wrote the manuscript. All authors discussed the experimental and theoretical results and commented on the manuscript. All authors have approved the final version of the manuscript.

Competing interests

The authors declare no competing interests.

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