Supplementary Information: *High Performance Monolithic Integration of Light Amplifiers in Silicon Photonic Circuits*

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I III/V stack

A schematic of the full epitaxial structure is presented in Supplementary Fig. 1(**a**). Atomic force microscopy (AFM) measurements of Supplementary Fig.1(**b**) revealed a surface root-mean-square roughness of 1.62 nm of GaAs grown on the asymmetric step-graded (ASG) buffer layer on Ge-on-Si virtual substrate (VS), while the threading dislocation density (TDD) was measured to be 7.3×10^6 cm^{-2} using electron channeling contrast imaging (ECCI) as shown in Supplementary Fig. 1(**c**).

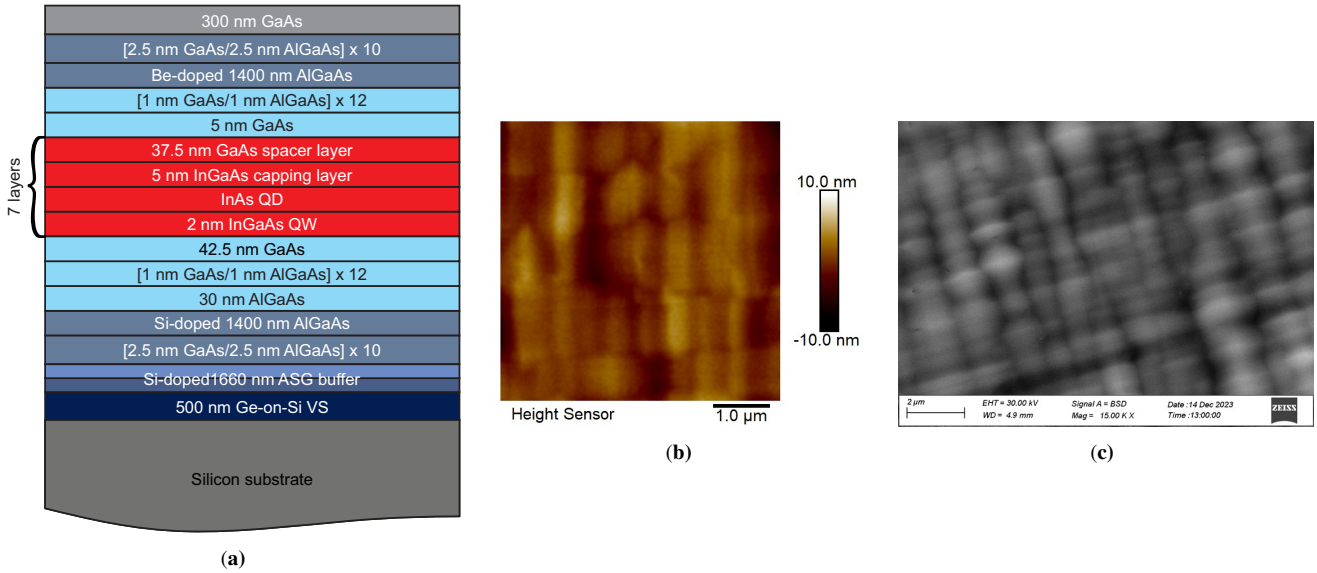


Fig. 1. III/V epitaxy. (a) Full epitaxial stack, (b) atomic force microscopy (AFM) measurements and (c) electron channeling contrast imaging (ECCI). ASG: asymmetric step-graded, VS: virtual substrate.

II Fabrication Process Steps

Supplementary Fig. 2 illustrates the fabrication steps for the laser integration with the SiN waveguides.

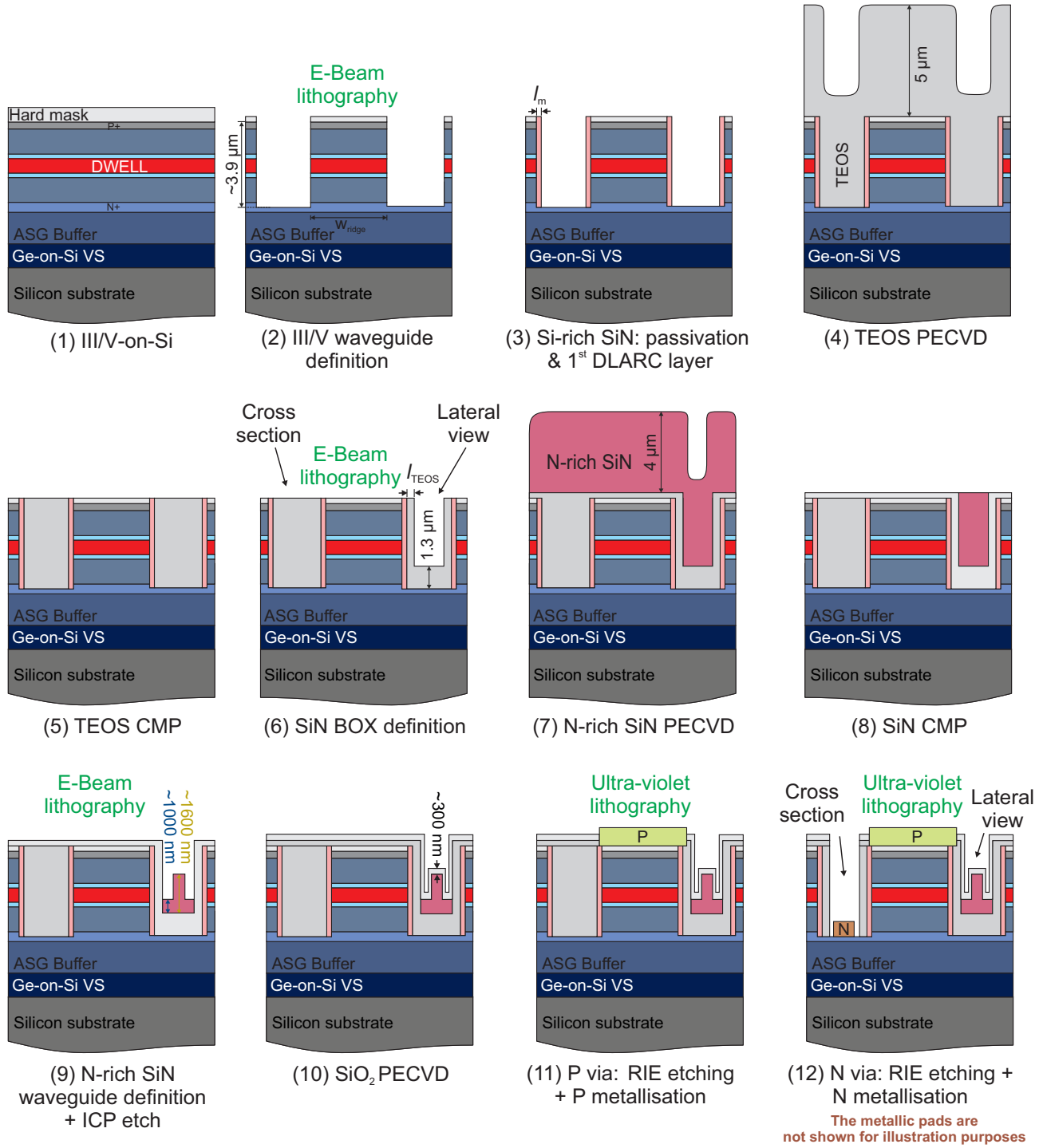


Fig. 2. Fabrication process flow. DWELL: Dot-in-well, ASG: asymmetric step-graded, VS: virtual substrate.

III Active-to-Passive Coupling

The passive waveguide platform used for the coupling with the III/V gain areas was a N-rich silicon nitride (SiN) composition with a refractive index of $n = 1.9$. This material has shown low propagation losses in the O-band, ranging from 1 to 2 dB cm^{-1}[11],

while its amorphous, tunable and low temperature growth with plasma-enhanced chemical vapour deposition (PECVD), allows thick layers in variable substrate configurations without defects.

Low losses and reflections at the interface between the active III/V and the passive SiN waveguides is important for a reliable single-mode laser operation. Any modal spatial differences at the two waveguides and the effective index differences due to the different materials can cause unwanted coupling losses. Moreover, any parasitic back-reflections due to above discrepancies, can also lead to interference with the main lasing mode, resulting to disruption of coherence. For that reason, the meticulous design of the N-rich SiN waveguide cross-section is very important in order to maximise the coupling efficiency with the III/V waveguide. As implemented in Supplementary Ref. 2, a double-layer anti-reflective coating (DLARC) with a tetraethyl orthosilicate (TEOS) layer and a silicon-rich (Si-rich) SiN layer was used to reduce the light reflected back to the laser. The refractive indices of the layers were $n = 1.446$ and $n = 2.514$, respectively.

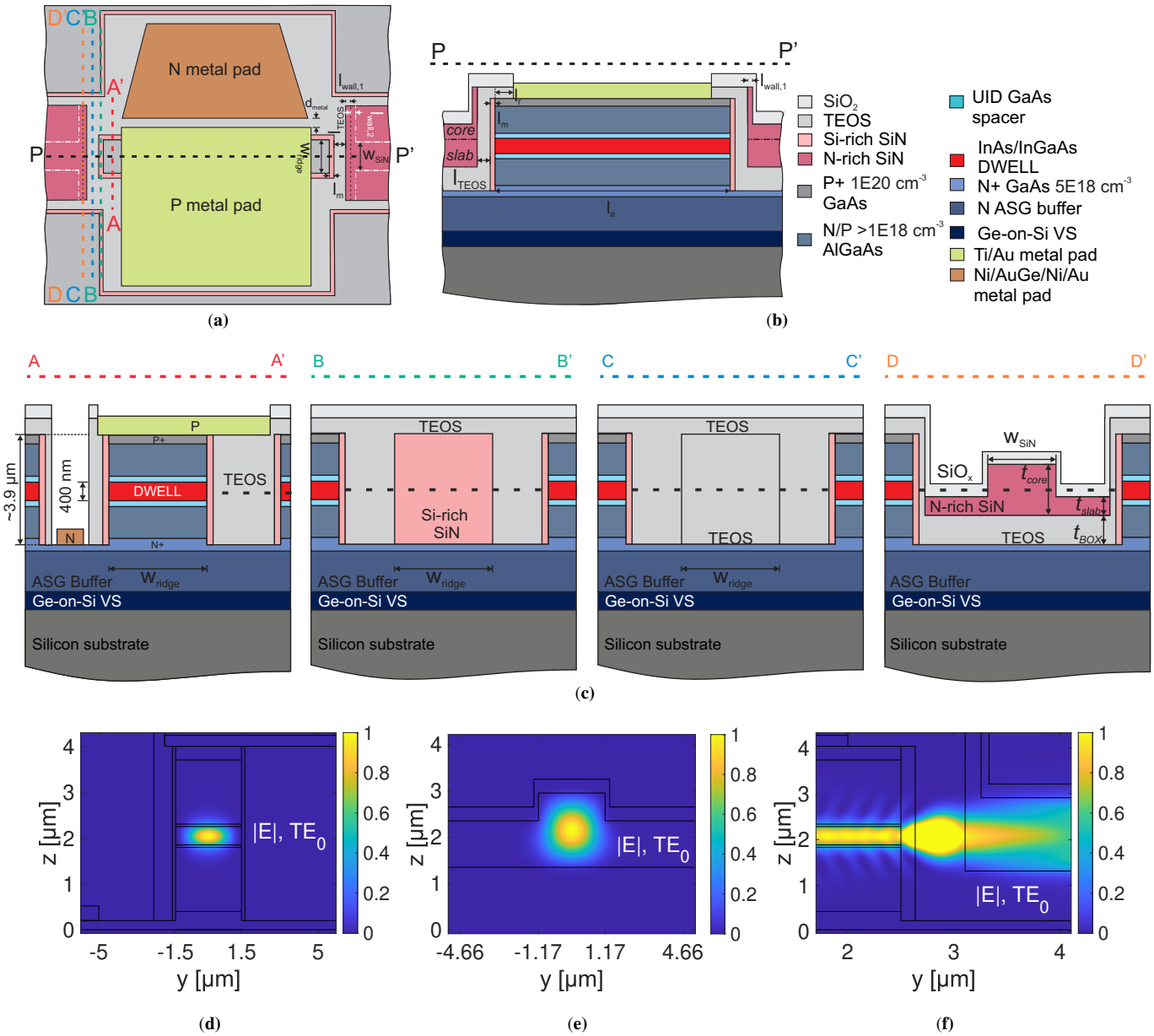


Fig. 3. Integration schematics. The quantum dot laser integrated with silicon nitride (SiN) waveguides in (a) top and (b) lateral views. The cross sections of the III/V and SiN waveguides along with the double layer anti-reflective coatings (DLARCs) of Si-rich SiN and TEOS are shown in (c). The intensity of the supported TE modes in the III/V and SiN waveguides are plotted in (d) and (e), respectively. The light transition from the III/V to the SiN waveguide is depicted in (f). ASG: asymmetric step-graded, VS: virtual substrate, UID: unintentionally doped, DWELL: Dot-in-well, TE: transverse electric.

Two-dimensional schematics of the active-to-passive transition in a top and a side view are given in Supplementary Fig. 3(**a**) and 3(**b**), respectively, along with the waveguides' cross-sections in Supplementary Fig. 3(**c**). The interface between the waveguides is designed as normal. The III/V section is a ridge waveguide and the N-rich SiN section is designed as a rib waveguide. The structures are encapsulated in SiO_2 top and TEOS bottom claddings of thicknesses t_{TOX} and t_{BOX}, respectively. The fundamental TE modes for the III/V and the SiN waveguides are shown in the Supplementary Fig. 3(**d**) and Supplementary Fig. 3(**e**), respectively, as simulated with the commercial software *MODE Solutions* from Ansys. Moreover, the light propagation at the III/V-SiN interface as modelled with 3D finite-difference time-domain (3D-FDTD) simulations using the commercial software *FDTD Solutions* from Ansys, is shown in Supplementary Fig. 3(**f**) with the input port at the III/V waveguide and the output port at the SiN waveguide.

To prevent any interaction between the top metal electrode and the optical field, a recessed length l_r was strategically left above the III/V waveguide. This structural modification allows the metal pad to remain clear of the loosely confined optical mode in the adjacent SiN region. Instead, the contact is placed on top only of the III/V material stack in a location where the guided mode is highly confined and minimally affected by surface proximity. Despite the offset, a consistent electric field is maintained throughout the III/V region, due to the high level of P+ doping (10^{20} cm^{-3}). The two electrodes are laterally spaced by roughly $d_{metal} \sim 10\,\mu$m.

High-efficiency optical coupling was achieved by carefully refining the physical dimensions of both SiN and III/V waveguide structures. Key parameters—including the thicknesses of the SiN core (t_{core}) and underlying slab (t_{slab}), along with the lateral widths of the SiN waveguide (w_{SiN}) and the III/V ridge (w_{ridge})—were engineered to enhance the modal overlap and optimise the coupling efficiency. These design efforts used detailed 3D-FDTD modelling, leveraging S-parameter analysis to fine-tune the matching of the TE-polarised fundamental mode across the interface. To counteract alignment limitations inherent to electron-beam lithography—where overlay accuracy is restricted to about 20 nm—a longitudinal layer of tetraethyl orthosilicate (TEOS) was introduced, with a defined length of l_{TEOS}. This layer functions as a lithographic buffer, compensating for misalignment during processing while preserving the intended profile of the Si-rich SiN slab. During the dry etching which is used to shape the buried oxide (BOX) cladding, the longitudinal TEOS layer acts as a protective barrier, safeguarding the Si-rich layer. Without this layer unwanted thinning of the Si-rich material could occur, degrading the performance of the anti-reflective coating (ARC) and distorting the optical field. Furthermore, two protective layers were used to prevent any etching of the TEOS anti-reflective layer during the etching of the SiN waveguide. These were designed with lengths of $l_{wall,1}$ and $l_{wall,2}$ referring to the etch of the SiN window and the slab of the rib waveguide, respectively.

The efficiency of the coupling between the III/V and the SiN waveguides was assessed through a cut-back structure. The cut-back structure consisted of a set of cascaded III/V-SiN interfaces of increasing number, as shown in Supplementary Fig. 4(**a**). The N-rich SiN waveguide sections contain a taper in order to filter out potential higher-order modes, while 100 µm long III/V waveguides were used to avoid reflections due to potential modal fluctuations during propagation. It is noted, that the III/V sections for the cascaded interfaces were metallised. To determine the loss at one interface, the overall measured response as plotted in Supplementary Fig. 4(**b**) was adjusted by deducting the III/V insertion loss, the insertion loss of the N-rich SiN passive part and the loss from the fibre-to-facet coupling. This calculation was done for the wavelength range of 1260 nm-1360 nm. The coupling loss was derived from different devices used in the cut-back structure of a single chip. The III/V-SiN interface for this cut-back structure can be seen in the scanning electron microscope (SEM) of Supplementary Fig. 5. The real geometric parameters of the fabricated device are indicated on the image. It is noted that a small air gap of ∼55 nm length between the Si-rich SiN and the TEOS ARC layers is taken into account.

According to Supplementary Fig. 4(**c**), the coupling loss in the O-band decreases as the wavelength increases and it reaches values down to 1.48 dB at 1330 nm and 1.45 dB at 1350 nm. It is noted that all the measured values in the O-band were below 2.18 dB. The transition at the fabricated interface was simulated and plotted for comparison with the measured response in the same figure showing agreement between the theoretical and the experimental results. The losses for different waveguide widths at the interface were characterised for different chips and plotted in Supplementary Fig. 4(**d**) along with the simulated values for the optimally designed geometry. It is noted, that the simulated points are plotted as the mean values and standard deviations of the S_{12} and S_{21} parameters, taking into account both III/V-to-SiN and SiN-to-III/V responses. The errobar values corresponding to the standard deviation are $<10^{-3}$ highlighting the reciprocity of the coupling at the waveguide interface.

The discrepancy between the two cases is attributed to geometric and material deviations from the ideal coupling scenario. Fabrication challenges such as a lithographic overlay misalignment, an over or under-exposure, over or under-etching steps and constraints in characterisation techniques, like ellipsometry measurements on multi-layer dielectric stacks, can induce differences from the optimal design manifold. Specifically, they can cause errors in the thicknesses and the refractive indices of the waveguides, the lengths and the refractive indices of the anti-reflective layers and the positioning of the waveguides against each other. The spread of the coupling loss and the back-reflection around their optimal values can be assessed through propagation 3D-FDTD simulations with random variations on each geometric and material variable in a constrained range as described in the work of Supplementary Ref. 3 and applied in the work of Supplementary Ref. 2. In this work a population of

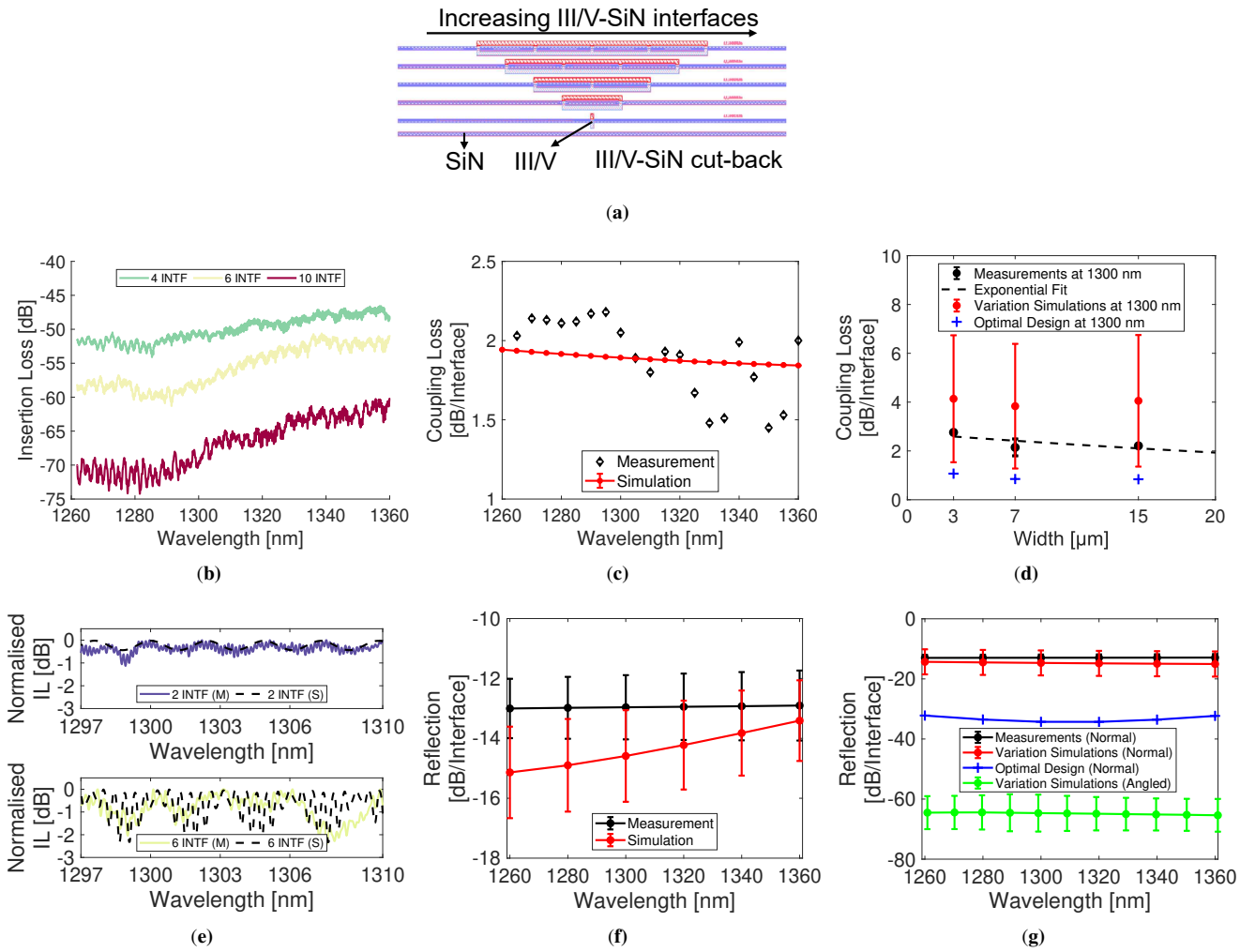


Fig. 4. Coupling efficiency. (a) The cut-back structure used for the assessment of the III/V-SiN interface coupling losses and back-reflections. The spectra for 7 μm wide devices with an escalating number of III/V-SiN interfaces is shown in (b). The calculated coupling losses from the spectral measurements of (b) are plotted in (c). The corresponding simulated values are also plotted. Measurements and simulations are depicted in (d) for a varied laser width. The characterised loss is plotted with black dots, the ideal simulated loss is plotted with blue crosses and the simulated response based on material and geometric variations is plotted with red dots. The dots refer to the mean value, accompanied by a standard deviation error bar. In (e) the normalised spectral response around 1300 nm for two and six interfaces is plotted, along with the circuit simulated and fitted graph. The characterised reflection based on the simulated fit of (e) is plotted in (f), along with propagation simulations. In (g) the measured reflection is compared with the simulated values under an ideal normal design and for geometric and material parameter variations. The simulated reflection under an angled junction is also plotted. The characterised reflection is plotted with black dots, the ideal simulated reflection is plotted with blue crosses and the simulated normal and angled interface response based on material and geometric variations is plotted with red and green dots, respectively. The dots represent mean values, accompanied by a standard deviation error bar.

100 uniformly distributed points was used for the whole O-band. The variables for the designed optimal point and the given range to the variables is provided in Supplementary Table 1. It is important to note that this design point was selected primarily to optimise the back-reflection, aiming to achieve the lowest disruption to the lasing mode. The parameters for the fabricated devices as shown in Supplementary Fig. 5 are given also in Supplementary Table 1. The statistical analysis from the graph suggests that the interface maintains a coupling loss near 4 dB and can be even below 2 dB, as measured for the real devices.

The same cut-back structure was used to calculate the back-reflection for one interface. The reflectivity of each interface was based on the fitting of the insertion loss to the simulated response using a scattering matrix model, as described in Supplementary

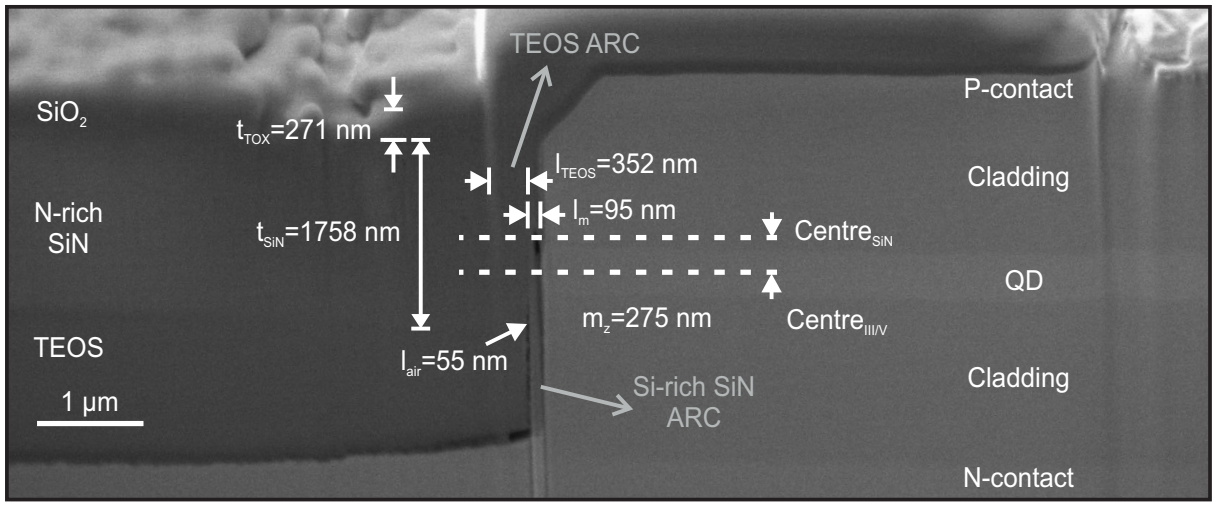


Fig. 5. Scanning electron microscope (SEM) image of the III/V-SiN interface.

Table 1. Geometric and material variables of the active-to-passive interface as designed and as varied. The variables are the following, t_{core}: SiN rib waveguide core thickness, t_{slab}: SiN rib waveguide slab thickness, $n_{\text{N-SiN}}$: N-rich SiN refractive index, l_{TEOS}: length of the TEOS anti-reflective coating, l_m: length of the Si-rich SiN anti-reflective coating, w_{SiN}: width of the SiN waveguide, w_{ridge}: width of the III/V waveguide, $l_{wall,1}$: SiN waveguide protection layer 1, $l_{wall,2}$: SiN waveguide protection layer 2, m_z: z-axis waveguide misalignment, l_{air}: air gap between the Si-rich SiN and TEOS anti-reflective layers.

Case	t_{core} [µm]	t_{slab} [µm]	$n_{\text{N-SiN}}$	l_{TEOS} [nm]	l_{m} [nm]	n_{m}	w_{SiN} [µm]	w_{ridge} [µm]	$l_{wall,1}$ [nm]	$l_{wall,2}$ [nm]	m_z [nm]	l_{air} [nm]
Design	1.6	1	1.9	470	135	2.514	6.17	7	150	150	0	0
Fabricated	1.758	1.168	1.9	352	95	2.514	6	7	~ 150	~ 150	275	55
Range	[1600, 2400]	[800, 1200]	[1.88, 1.92]	[320, 620]	[85, 185]	[2.484, 2.544]	[5970, 6370]	[6800, 7050]	[130, 170]	[130, 170]	[0, 1000]	[0, 100]

Ref. 3. The devices with 2 and 6 interfaces in total were used to compare its measured and simulated responses near 1300 nm as plotted in Supplementary Fig. 4(**e**). It should be pointed out, that an envelope of the measurement response curve was used and that the simulation curve was normalised to its maximum value for a fair comparison. Based on the fit, a mean reflectivity of -12.96 dB with a standard deviation of ± 1.07 dB at 1300 nm and less than -12.90 dB in the whole O-band is calculated, which falls into the simulated statistical range. The measured reflections are given as mean values and standard deviation bars based on the two different fittings for the 2 and the 6 interfaces. The simulated mean values and standard deviations refer to the S_{11} and S_{22} parameters, taking into account both III/V-to-SiN and SiN-to-III/V responses.

The range of values from the Supplementary Table 1 were used for the generation of the simulated points based on the randomly uniform transitioning cases. These points are plotted in Supplementary Fig. 4(**g**), along with the measured points and the optimally designed response. This suggests that the induced back-reflection to the laser taking into account multiple design deviations can be below -14 dB on average in the whole O-band, which aligns with quantum dot laser back-reflection tolerances of -13 dB, as discussed by Huang et al. (2025) in Supplementary Ref. 4. It is worth noting that the above study refers to a normal interface, however a more sophisticated angled junction can improve the reflectivity further safeguarding the effectiveness of the gain area. Specifically, by implementing a tilted interface of 7° a reflectivity below -60 dB can be maintained, as predicted by propagation simulations plotted in Supplementary Fig. 4(**g**). These simulation results take into account all the variations described in Supplementary Table 1.

IV Grating Coupler

The power of the light emitted by the laser was collected through an optical fibre and a straight grating coupler on the SiN platform. Hence, the measured power was normalised by the insertion losses of the SiN waveguide section and the response of

one grating coupler. The corresponding schematic layout is given in Fig. 6(**a**) and the total insertion loss is plotted in Fig. 6(**b**). The simulated reflections of one grating coupler as simulated by a 2D-FDTD solver using the commercial FDTD package of Ansys is also depicted in Supplementary Fig. 6(**b**).

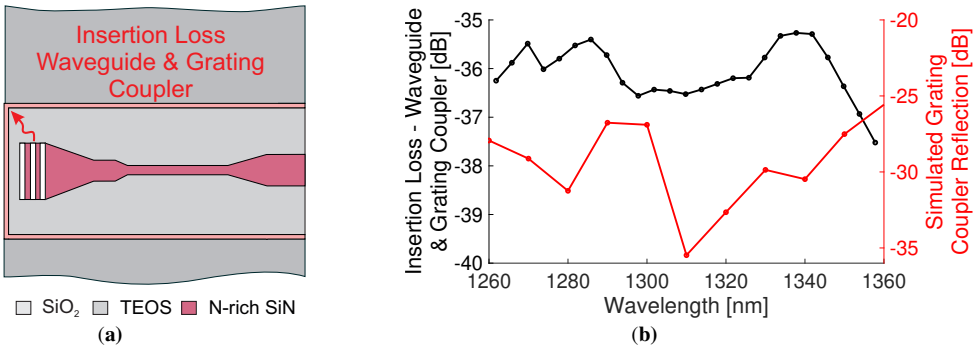


Fig. 6. Silicon nitride waveguide and grating coupler sections. (a) The layout and (b) the measured insertion losses along with the simulated reflections.

V Distributed Bragg Reflector

The distributed Bragg reflector (DBR) laser consists of two reflectors made on the N-rich SiN layer with different reflectivity levels. A top-view layout can be seen in Supplementary Fig. 7(**a**). The DBR gratings both exhibited a duty cycle ratio of 13:87 with a ∼340 nm period after fabrication and were all designed as first-order gratings, as seen in the SEM image of Supplementary Fig. 7(**b**). In addition to the intended cavity created by the DBR gratings, the reflections created by the SiN-III/V interfaces are taken into account. The grating couplers induce minimal reflections that can be seen in the results of 6(**b**) as simulated with the 2D-FDTD package by Ansys. Hence they are not considered in the analysis. Several sub-cavities can supply Fabry-Perot effects and individual resonances with distinctive free spectral ranges (FSRs), which can contribute to the superimposed interference. To simplify the calculation, the entire device is divided into three different waveguide segments determined by the four potential reflectors, namely the two DBRs and the two interfaces. The optical length of the waveguide segments is estimated by using their simulated group index n_g and their physical length. Supplementary Table 2 lists the parameters of the segments adopted for the cavity length calculation.

Table 2. Parameters and optical length for different waveguide segments.

Segment	Start	End	Length [µm]	n_g	Optical Length [µm]
SiN waveguide 1	DBR_L	$INTF_1$	231.215	2.0022	463
Gain section	$INTF_1$	$INTF_2$	3000	3.5403	10621
SiN waveguide 2	$INTF_2$	DBR_H	563.521	2.0022	1128

Supplementary Table 3 presents the four sub-cavities that are considered as the major contributors to the mode superposition. The optical length of the cavities that contain the DBR grating are given by summing up the optical path of the waveguide part and the effective length of grating. Since the two gratings have same design of index modulation, both effective lengths are calculated as 96.9 µm, which is shorter than the physical length of DBR_H, but longer than the physical length of DBR_L. Therefore, for the purpose of the optical length calculation, DBR_H is considered to have a penetration depth of 96.9 µm, whereas the other one is represented by its physical length as 20.34 µm. Using the average group index of the DBRs as 2.001, the optical path for two DBRs are 194 µm and 41 µm, respectively. The SiN-III/V junction is treated as a reflective interface in the cavity, as described in the *Active-to-Passive Coupling* section.

A fast Fourier transform (FFT) analysis of the amplified spontaneous emission (ASE) spectrum was performed to validate the existence of all four sub-cavities. The ASE spectra were acquired with 0.06 nm resolution and 2.6 GHz sampling interval at 17.5 °C. According to the Nyquist–Shannon sampling theorem only FSR frequencies higher than 5.2 GHz can be recognized with this FFT analysis. Supplementary Fig. 8(**a**) shows the ASE spectrum and Supplementary Fig. 8(**b**) depicts the corresponding FFT result of the ASE spectrum, which indicates the existence of all four sub-cavities. Peaks (a) and (d) are the highest and lowest FSR frequencies and they correspond to the longest cavity 1 formed between the two DBRs and the shortest

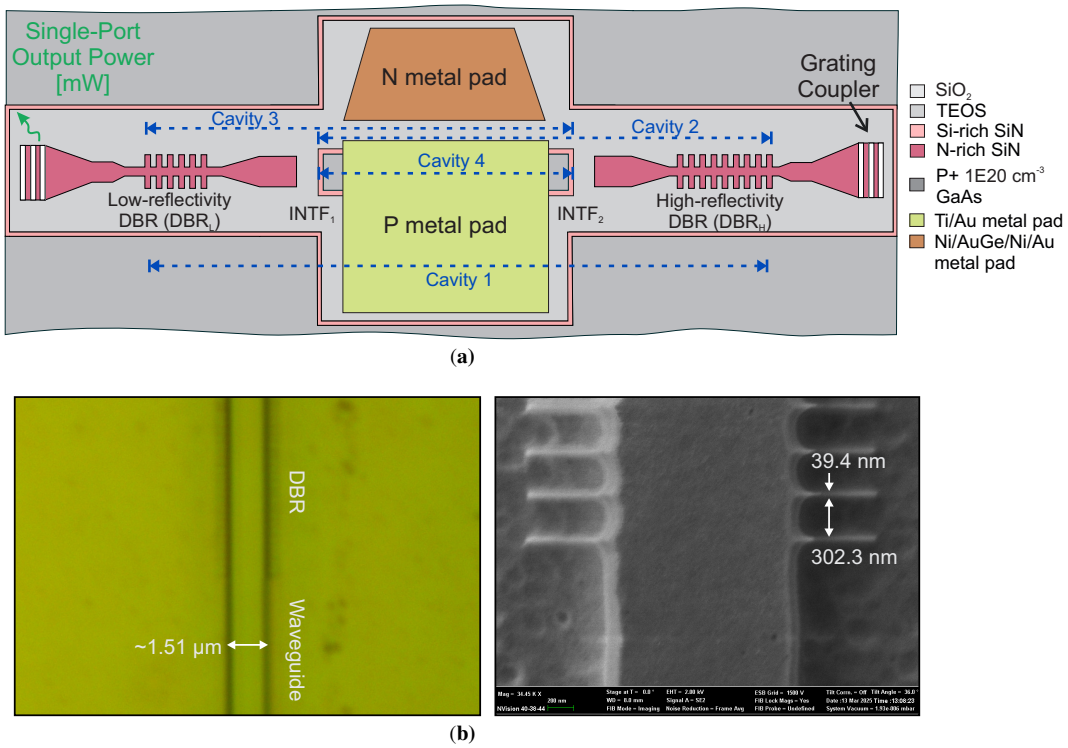


Fig. 7. The distributed Bragg reflector (DBR). (a) The layout of the DBR reflectors on the silicon nitride platform along with the gain area and (b) the fabricated DBR in a microscope and a scanning electron microscope (SEM) image.

Table 3. Distributed Bragg reflector (DBR) analysis. Cavity lengths and free spectral range (FSR) of the cavity modes calculated for different sub-cavities. DBR_H: High-reflectivity DBR, DBR_L: Low-reflectivity DBR.

Cavity Number	Mirrors	Optical Cavity Length [µm]	FSR [GHz]	Peak
1	DBR_H - DBR_L	12447	12.043	(a)
2	DBR_H - $INTF_1$	11278	13.291	(c)
3	$INTF_2$-DBR_L	11790	12.719	(b)
4	$INTF_1$-$INTF_2$	10621	14.113	(d)

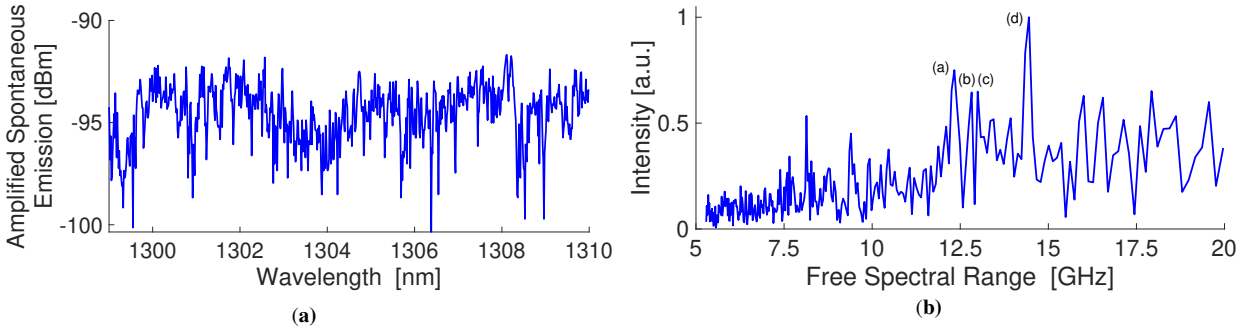


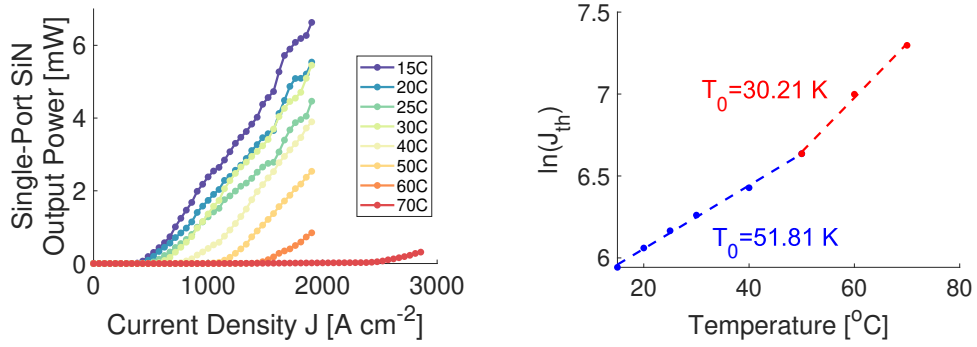
Fig. 8. Analysis of the amplified spontaneous emission spectra from the laser at 17.5 °C. The amplified spontaneous emission (ASE) spectrum of the laser in (a) and its fast Fourier transform (FFT) in (b).

cavity 4 between the two SiN-III/V interfaces, respectively. It is worth noting that the peak intensity of the cavity between the two interfaces is higher than the cavity enclosed by the two DBR reflectors, which is reasonable as the DBR cavity suffered the insertion losses from both SiN-III/V interfaces. Although the DBRs have higher reflectivity, the modal gain of this cavity is still impacted by the loss. Additionally, peaks (b) and (c) correspond to the sub-cavities 2 and 3, which are both hybrid cavities

formed by a DBR grating and an interface. These two peaks appear close to each other due to the similar optical lengths of their specific cavities. This result suggests that all sub-cavities contribute to the superimposed interference, consequently the final lasing process is determined by the Vernier effect contribution from the multiple cavities and has periodically spaced multi-modes.

VI Pulsed Lasing

The $7 \times 3000\,\mu m^2$ InAs/GaAs quantum dot (QD) DBR laser was characterised under pulsed injection with a time period of 200 µs and a pulsed width of 1 µs. The emitted power under a varying injection current and elevated temperatures was measured and it is shown in Supplementary Fig. 9(**a**). The device achieved lasing for a temperature up to 70 °C. The characteristic temperature T_0 of the laser was calculated as the slope of the $\ln(J_{th})$ against temperature and it is noted in Supplementary Fig. 9(**b**).



(**a**) (**b**)

Fig. 9. Pulsed operation of the $7 \times 3000\,\mu m^2$ InAs/GaAs QD laser. (a) The emitted power versus the threshold current density J_{th} at various temperatures and (b) the natural logarithm of J_{th} against temperature. The characteristic temperature of the laser is the slope of the linear fit of $\ln(J_{th})$ with temperature calculated for the regimes 20-50 °C and 50-70 °C.

In the 20-50 °C regime T_0 =51.81 K, while for 50-70 °C it dropped to 30.21 K. Under minimal self-heating the laser can operate at elevated temperatures, revealing the potential of the device in light of an improved heat dissipation around the active region. The influence of the thermal effects to the laser can be further mitigated with a modulation co-doping strategy for the QDs[5], in addition to a precisely designed heat extraction topology from the active region down to the silicon (Si) substrate.

Supplementary References

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