Supplementary Information:
Mechanism for reconfigurable logic in disordered dopant networks

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S1. INFLUENCE OF NUMBER OF COUNTERDOPANTS

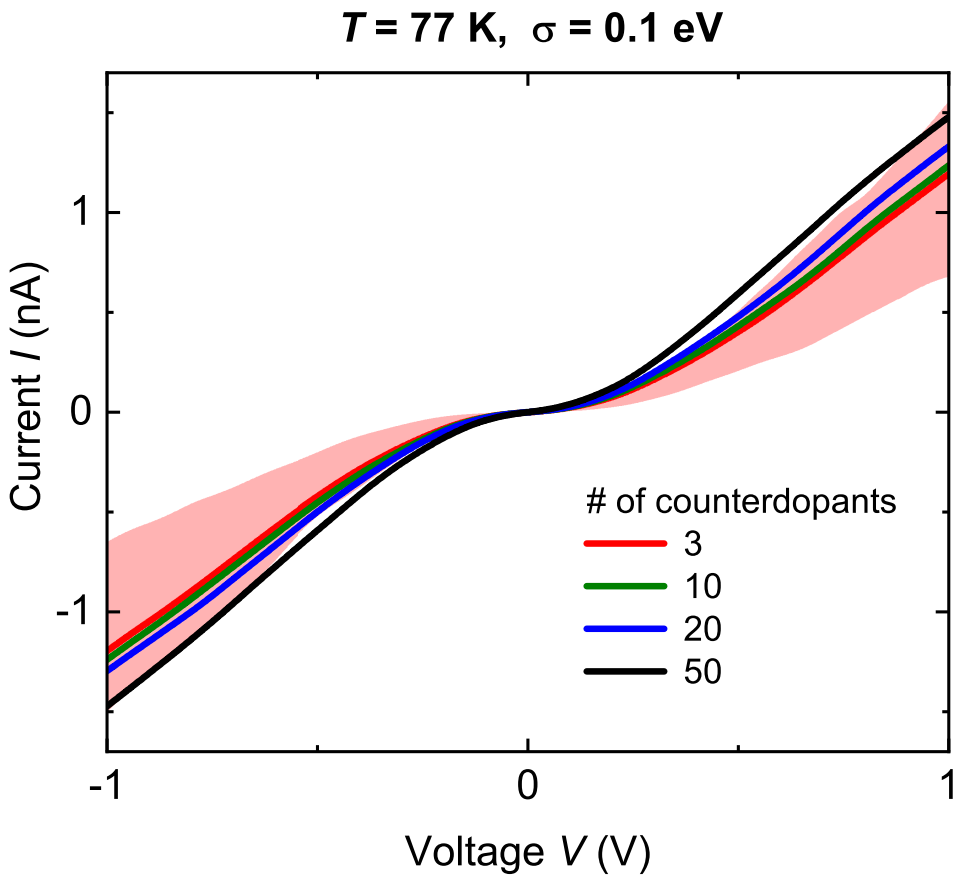
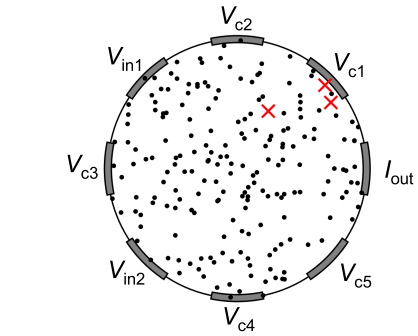


Figure S1. Simulated I–V characteristics at 77 K and energy disorder strength $\sigma = 0.1$ eV, averaged over the 8 neighbouring electrode combinations of 30 devices with different numbers of counterdopants. The result for 3 counterdopants is the same as in Fig. 1a of the main text, where half of the 240 I–V characteristics fall in the shaded red region. The averaged I–V characteristic for 50 counterdopants (black line) still falls in this region.

S2. ARTIFICIAL EVOLUTION OF BOOLEAN LOGIC IN A SECOND DEVICE



	AND	OR	NOR	NAND	XOR	XNOR
V_{c1}	0.158	-0.138	0.141	-0.035	-0.015	0.166
V_{c2}	0.896	-0.574	0.026	0.243	0.073	0.485
V_{c3}	0.088	-0.108	0.049	0.293	0.155	0.182
V_{c4}	-0.459	-0.338	-0.335	-0.590	-0.242	0.018
V_{c5}	-0.15	0.428	-0.328	-0.304	-0.082	-0.158
F	33.5	26.2	17.6	33.5	11.7	11.0

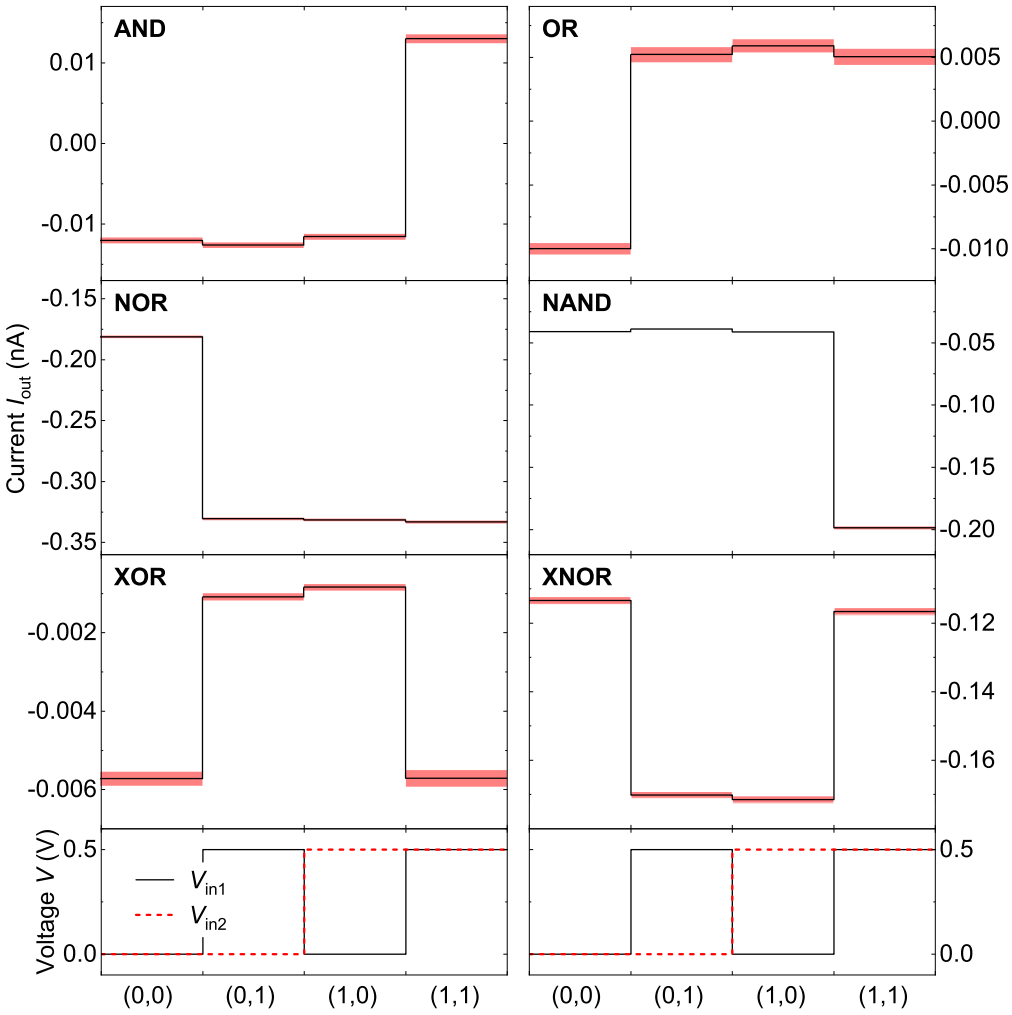
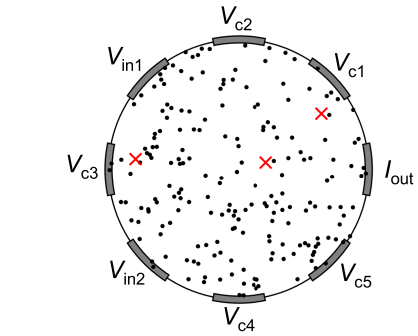


Figure S2. Boolean functionality at 77 K as found by artificial evolution in the device shown at the top left, which is different from that in Fig. 2 of the main text. The control voltages V_{c1}–V_{c5} and fitnesses F are given in the table at the top right.

S3. BOOLEAN LOGIC WITH SHORTER SIMULATION TIME



	AND	OR	NOR	NAND	XOR	XNOR
V_{c1}	0.146	0.218	-0.124	-0.155	-0.112	0.509
V_{c2}	0.975	0.468	-0.790	-0.437	-0.347	-0.542
V_{c3}	-0.602	-0.780	0.188	-0.353	-0.414	0.505
V_{c4}	0.887	-0.272	-0.415	-0.199	-0.240	-0.231
V_{c5}	0.209	-0.209	-0.403	-0.109	0.083	-0.316
F	19.9	21.3	18.5	14.9	19.3	4.0

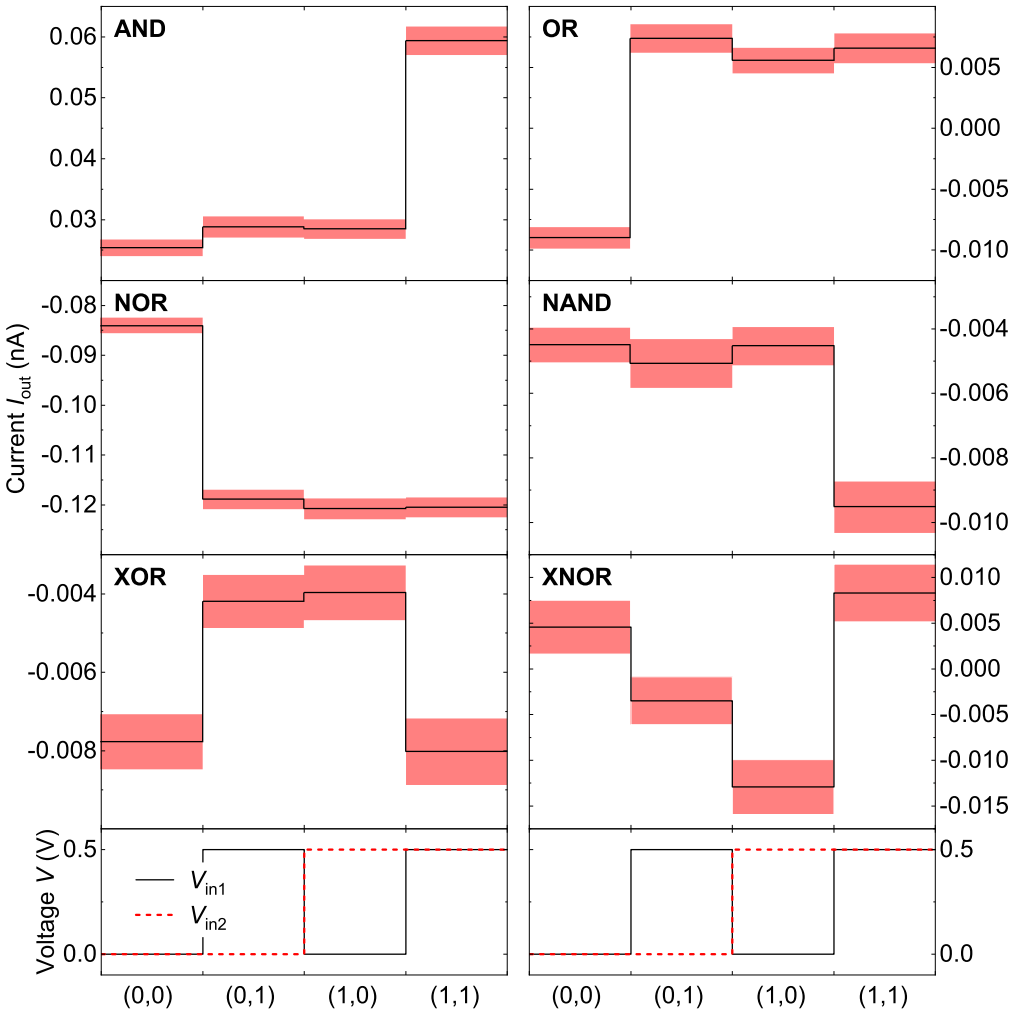


Figure S3. Same as in Fig. 2 of the main text, but with currents and uncertainties determined for 10^6 instead of 10^7 KMC steps. The control voltages V_{c1}–V_{c5} are unchanged.

S4. VOLTAGE AND CURRENT DISTRIBUTIONS FOR RANDOM CONTROL VOLTAGES

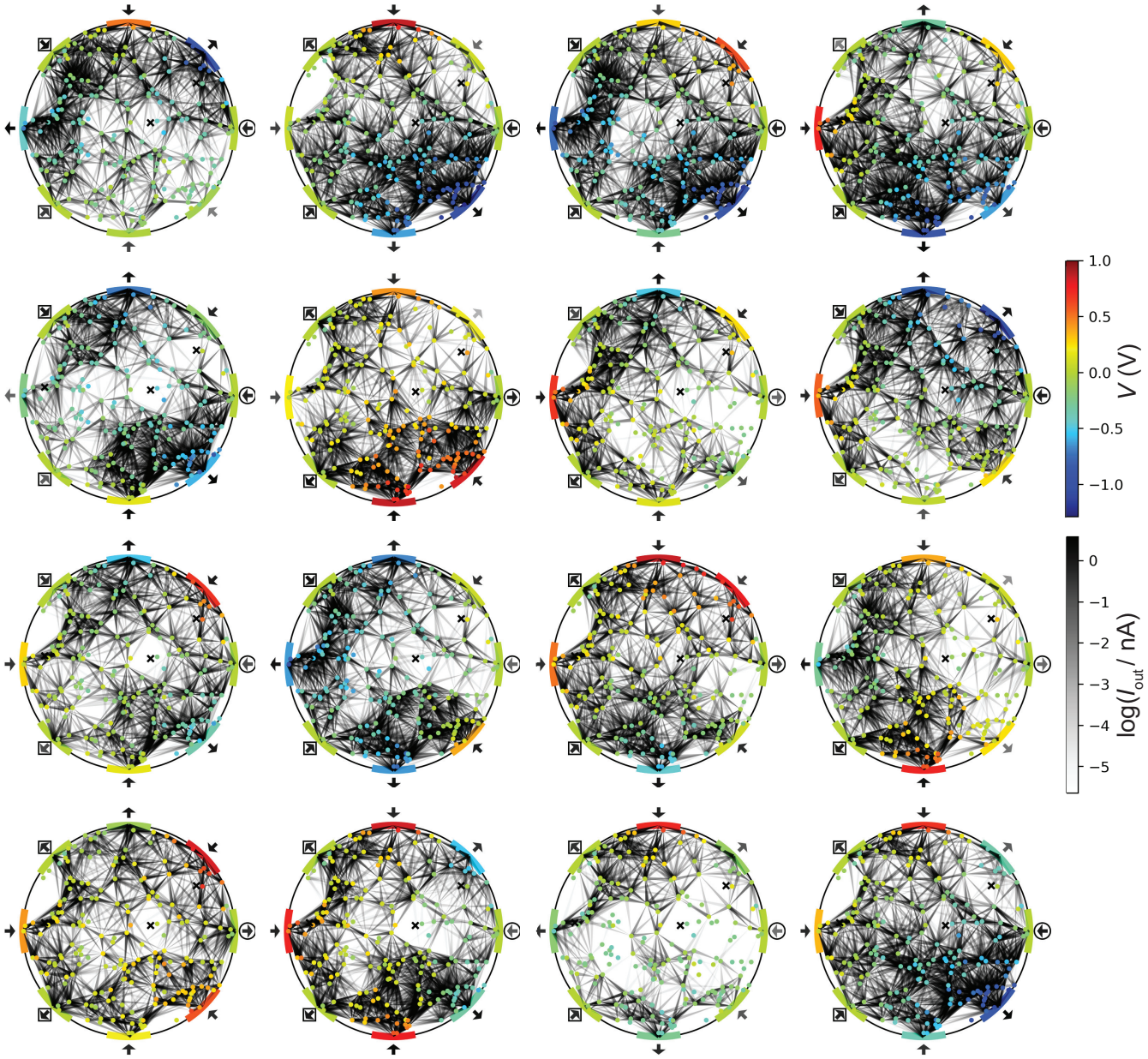


Figure S4. Voltages and currents for the device of Fig. 2 in the main text with 16 random control voltages in the interval [−1,1] V and (0,0) input.

S5. VOLTAGE AND CURRENT DISTRIBUTIONS FOR BOOLEAN GATES IN A SECOND DEVICE

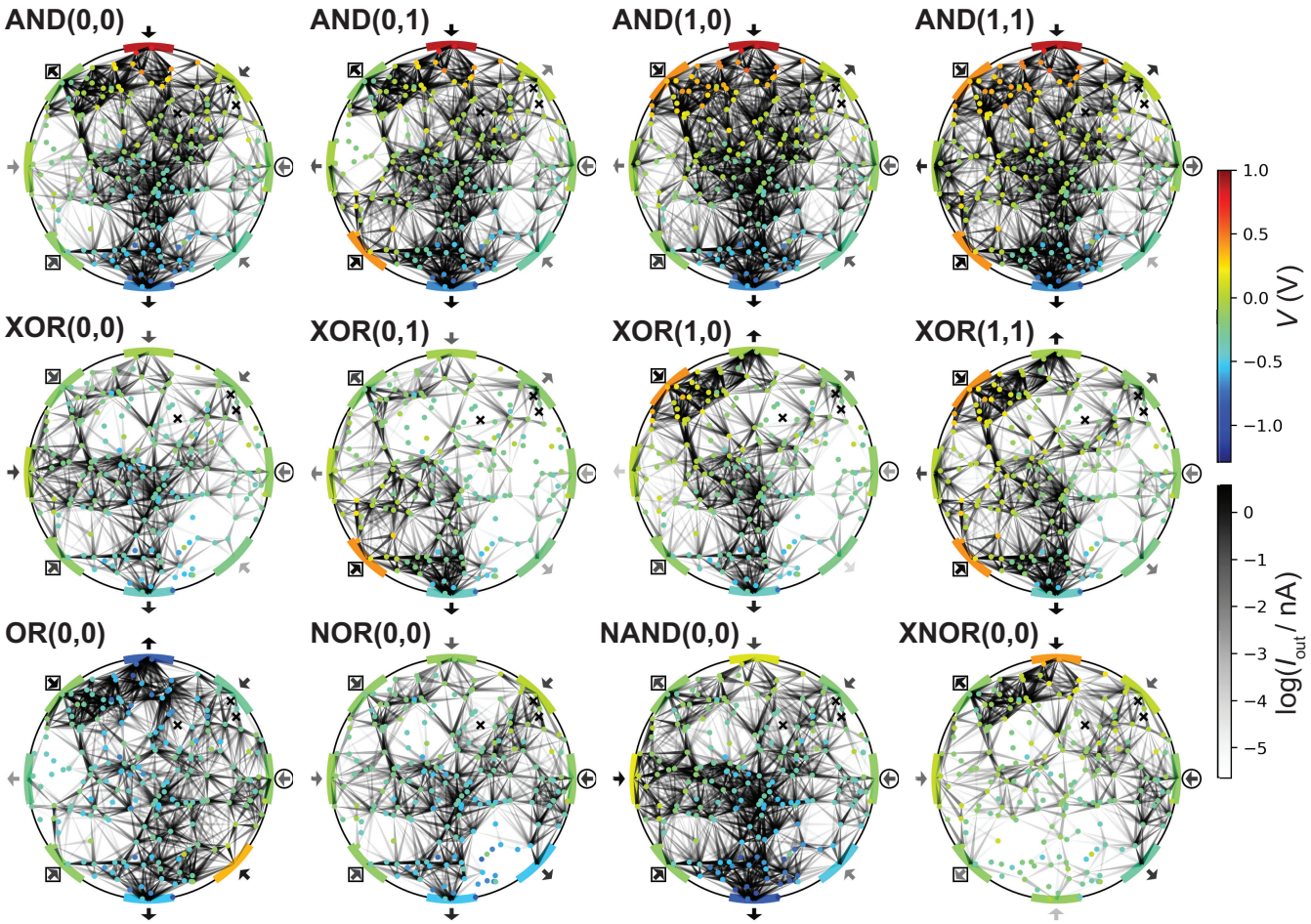


Figure S5. Voltages and currents for the device of Fig. S2. First row: AND gate for the four logic input combinations. Second row: XOR gate. Third row: OR, NOR, NAND, and XNOR gate with (0,0) input.

S6. CORRELATIONS IN OUTPUT CURRENT FOR DIFFERENT LOGIC INPUTS

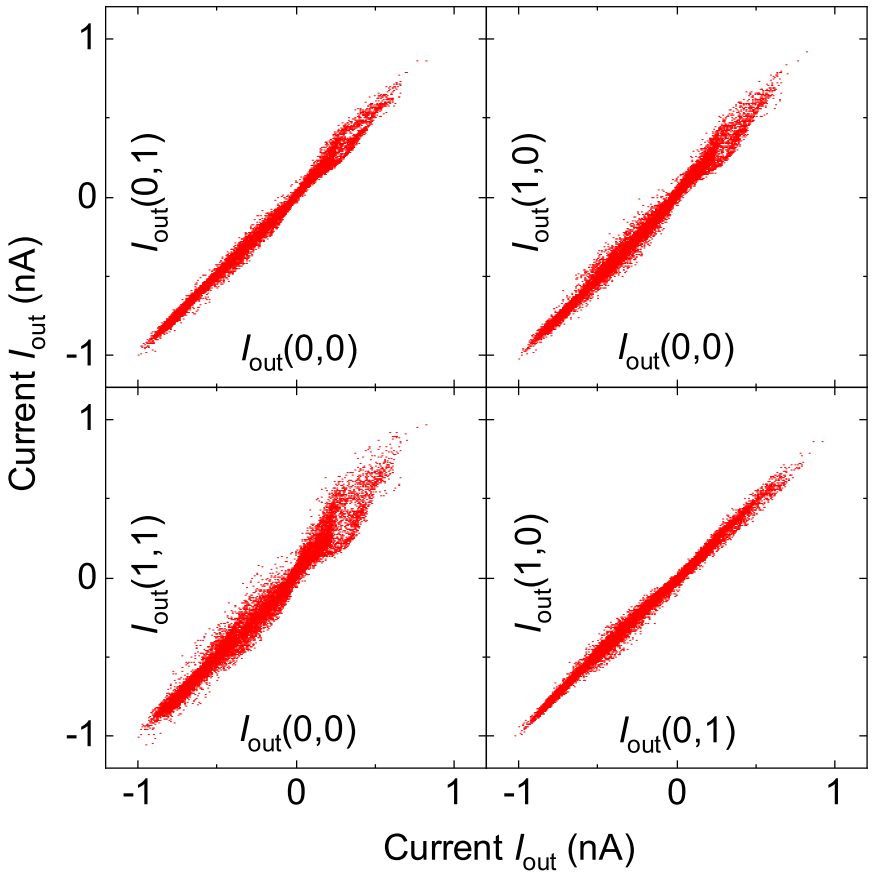


Figure S6. Correlations between current outputs of the device of Fig. 2 in the main text for logic inputs (0,0), (1,0), (0,1), and (1,1), and about 20,000 random combinations of the control voltages V_{c1}–V_{c5} in the interval [−1,1] V.

S7. SENSITIVITY OF AND AND XOR GATES TO V_{c2} AND V_{c3}

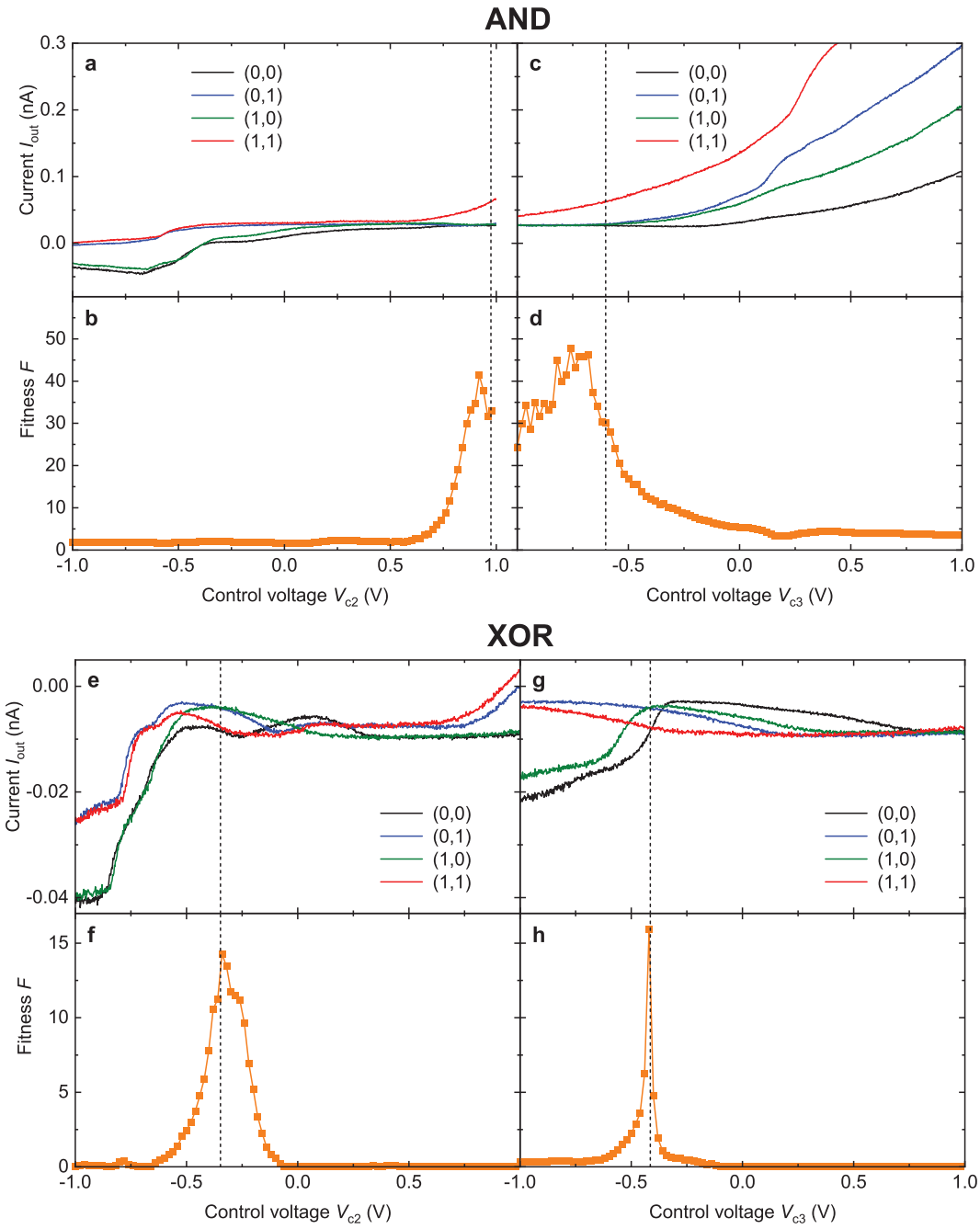


Figure S7. **a**, Output currents I_{out} for the four logic input combinations and **b** fitness F of the AND gate of Fig. 2 in the main text as a function of control voltage V_{c2}. Vertical dashed lines in a and b: value of V_{c2} found by artificial evolution. **c** and **d**, Same as a and b, but for V_{c3}. The evolutionary algorithm did not find before stopping the somewhat higher fitnesses of F in b and d at other values of V_{c2} and V_{c3}. **e**–**h**, Same as a–d, but for the XOR gate.

S8. GATE ABUNDANCES IN A SECOND DEVICE

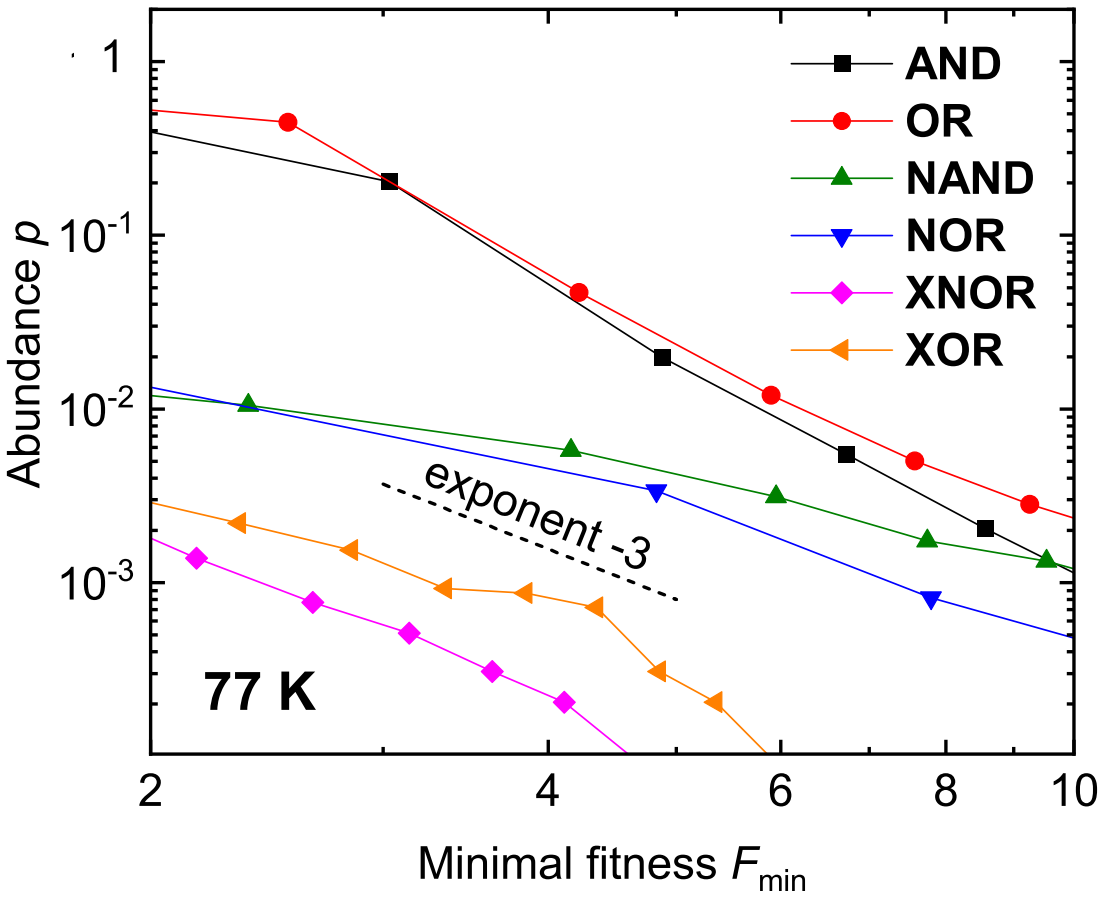


Figure S8. Abundance p of the six basic Boolean gates with minimal fitness $F_{\min}$ among about 20,000 random combinations of the control voltages V_{c1}–V_{c5} of the device in Fig. S2 at 77 K. Fitnesses were obtained from simulations of 10^7 KMC steps for each combination. Dashed line: power law with exponent −3.