Supplementary Information

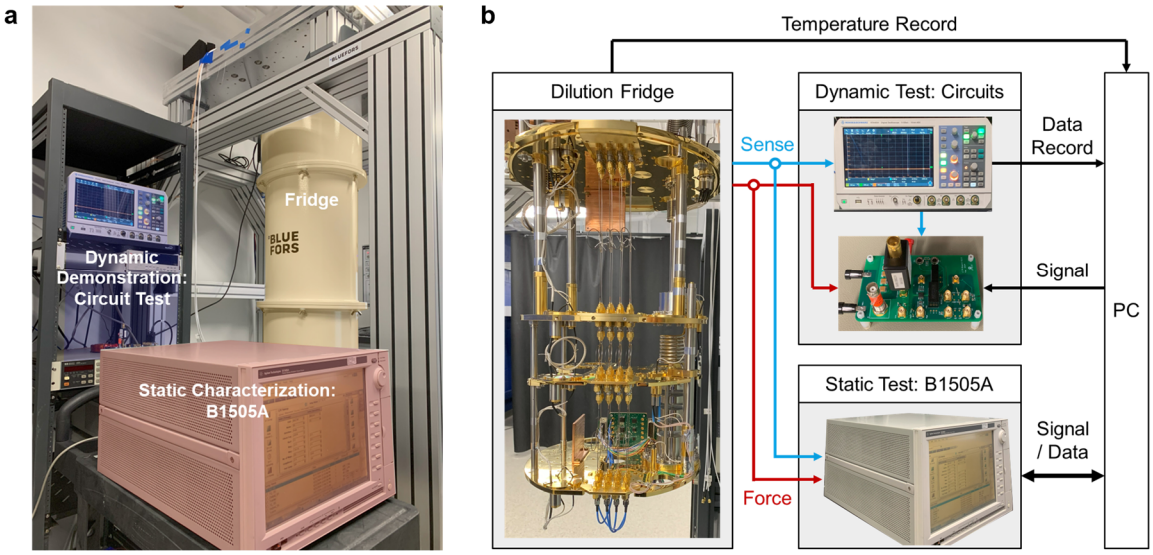
Supplementary Note 1. Cryogenic measurement environment

The cryogenic measurement system (**Supplementary Fig. 1a**) comprises a cryogen-free dilution refrigerator and a comprehensive suite of electrical characterization equipment for both static and dynamic measurements. To minimize interference, all equipment is stabilized in racks, and cabling is meticulously secured. A schematic overview of the system and its connections is provided in **Supplementary Fig. 1b**.

The cooling system utilizes a Bluefors LD250 cryogen-free dilution refrigerator, which features a multi-plate structure capable of providing temperatures down to ~10 mK. The entire system is enclosed within four concentric cans to ensure optimal thermal isolation and maintain vacuum conditions. Temperature monitoring within the system is performed using a well-calibrated CX-1010-SD-HT-P sensor, commonly employed in quantum experiments. A dilution unit, supported by a turbo pump, continuously maintains the cooling cycle during operation, enabling stable temperatures below 10 mK in the mixing chamber, located at the bottom of the refrigerator.

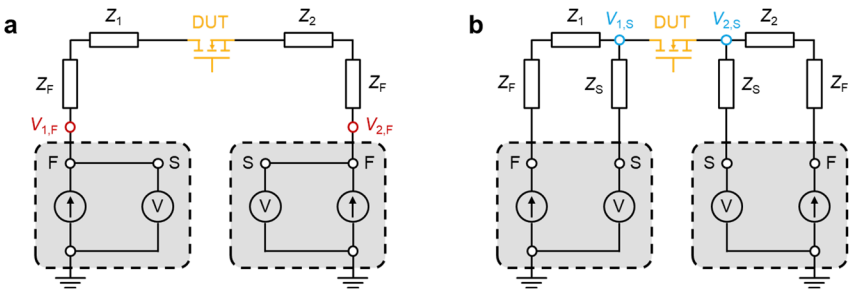
The device under test (DUT) is mounted on a custom-designed daughter board, which is secured to the mixing chamber plate using cryogenic thermal paste to enhance thermal conduction. This daughter board is designed to accommodate various device footprints and feature multiple coaxial connectors for signal transmission. The connection of measurement signals within the cryogenic environment adheres to the Kelvin (four-wire) connection principle to minimize measurement errors caused by cable impedances for both static and dynamic tests (**Supplementary Fig. 2**). Force lines, which carry the high voltage and current signals, are connected to the power input/output ports. Sense lines from the fridge, which transmit the measurement signals, are directly connected to the signal capture and recording ports. Driving or input signals are provided by a function generator and connected to the motherboard.

For static characterization, a Keysight B1505A Power Device Analyzer is used. This system integrates multiple measurement units and offers adjustable measurement modes. Dynamic measurements are performed using a custom-designed setup integrated onto a motherboard located outside the refrigerator. An automated Python-based program was developed to control the measurement processes and record temperature and waveform data.



Supplementary Figure 1 | Cryogenic test system for static and dynamic characterization. a, Photograph of the complete cryogenic test system, featuring the Bluefors dilution refrigerator housing the device under test (DUT), a Keysight B1505A power device analyzer for static measurements, and the custom-designed dynamic test setup including printed circuit boards (PCBs), power supplies, and an oscilloscope. **b,** System schematic and connections. The DUT is mounted at the mixing plate (base temperature of 10 mK) at the bottom of the refrigerator. Four-wire

Kelvin connections are utilized to separately carry force signals for high-current conduction and sense signals for precise voltage measurement. The setup supports both static and dynamic characterization circuits.

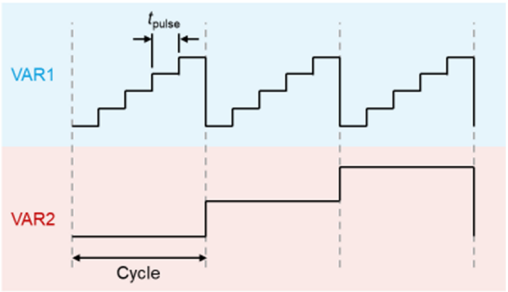


Supplementary Figure 2 | Schematic of two-wire connection and Kelvin connection. a, Typical two-wire connection. Measurement error arises from the equivalent impedance of cables (Z_1, Z_2, and Z_F). The measured device voltage ($V_{1,F}$ - $V_{2,F}$) will be higher than the actual value due to voltage drops across these impedances under high current. **b**, Kelvin (four-wire) connection. Voltage meters are connected as close as possible to the DUT, effectively excluding the impact of voltage drops across Z_1, Z_2, and Z_F. The sense line does not conduct high measurement current, rendering the voltage drop on Z_S negligible.

Supplementary Note 2. Static and dynamic measurement setup

B1505A based static measurement

The Keysight B1505A Power Device Analyzer integrates multiple source measurement units (SMUs) with various power, voltage, and current capabilities. For device static characterization, a High Power SMU (HPSMU) was connected to the device's drain and source terminals, functioning as the primary sweep parameter (VAR1) in current sweep mode. The measurement ranges span from ±1 nA to ±1 A, employing a log-scale sweep with high resolution down to 10 fA in the 1 nA range. The pulse width (t_{pulse}) for these measurements was set at 100 ms to mitigate the effects of on/off ringing. A total of 200 measurement points were acquired. The device's gate signal served as the secondary sweep parameter (VAR2) in voltage sweep mode. The gate voltage remained constant during each sweep cycle of VAR1 and stepped to the next value upon completion of each primary sweep cycle.



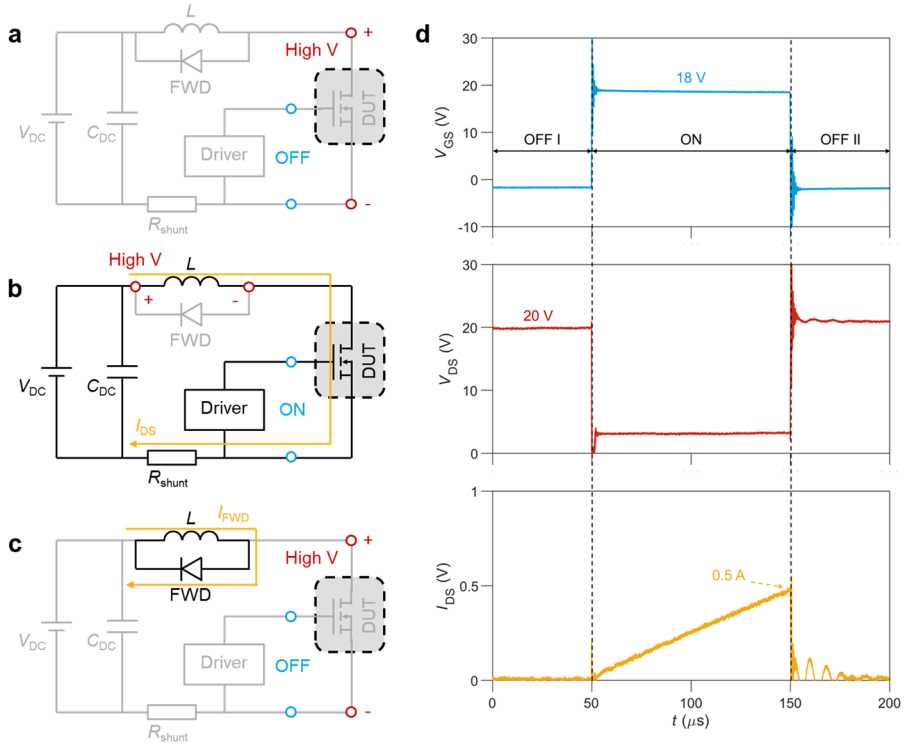
Supplementary Figure 3 | Schematic of current-voltage (*I-V*) sweep mode. This diagram illustrates the sequential operation of the *I-V* sweep. The primary sweep parameter (VAR1) executes a sweep from its start to stop value with a defined step and pulse width (t_{pulse}). During each VAR1 sweep cycle, the secondary sweep parameter (VAR2) remains constant. Upon completion of a VAR1 cycle, VAR1 resets to zero, and the process repeats with an incremented value of VAR2.

Circuit based dynamic measurement

A circuit-based dynamic measurement method, the single-pulse test (SPT), was employed for dynamic characterization. This technique overcomes the current limitation of static tests and enables faster measurements, operating within microseconds. The DUT remains inside the cryogenic refrigerator, while a custom-designed motherboard houses other electronic components outside. The power loop of the SPT circuit consists of an adjustable DC power supply (V_{DC}), 10 μF DC input capacitors (C_{DC}), a 5.5 mH inductor

(*L*), and a Schottky diode free-wheeling diode (FWD). Current measurements are performed using a serially connected 0.1 Ω coaxial shunt resistor (SSDN-10), chosen for its low parasitic parameters and suitability for high-frequency applications. Output signals from the shunt resistor and device voltage from the sense lines are connected to an RTA4004 oscilloscope. A commercial driver IC (Si8271) generates the gate signal, triggered by a function generator. This driver IC provides an adjustable gate voltage from -5 V to 20 V, with a +18 V/-2 V combination used for the on/off states in this test.

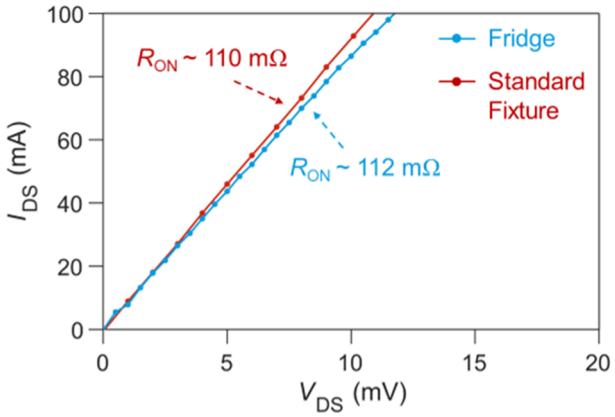
Supplementary Figure 4a shows the equivalent circuit schematic during the initial off-state (OFF I) before the trigger signal arrives. In this state, the DUT blocks the voltage bias from V_{DC}, and no current flows through the circuit. When the device turns on (**Supplementary Fig. 4b**), controlled by the function generator, the DC bias is applied to the inductor, generating a linearly increasing current through the inductor, DUT, and shunt resistor. The total on-state time is custom-defined, set to 100 μs in this test. This shorter pulse duration, compared to the 100 ms pulse used in static measurements, effectively prevents device self-heating at high currents. After this period, the device turns off again (OFF II), and the current is transferred to the free-wheeling diode branch (**Supplementary Fig. 4c**). Consequently, the device current rapidly drops to zero, while the inductor current slowly decreases until it reaches zero, at which point the system returns to the OFF I stage. The full switching waveforms, including gate voltage (V_{GS}), device voltage (V_{DS}), and current (I_{DS}) under a 20 V bus voltage at 20 mK are shown in **Supplementary Fig. 4d**. The maximum current can be adjusted by changing the bus voltage, the inductor or the pulse width. By mapping the current and voltage data together during the on-state, the extended *I-V* curve can be accurately extracted at higher current levels.



Supplementary Figure 4 | Working principles of dynamic single-pulse test (SPT). a, Equivalent circuit schematic of SPT at the initial off-state (OFF I). The device is in the off-state with a low gate voltage, and a high voltage bias is applied across the DUT's drain and source. **b**, On-state (ON), with a high voltage bias applied across the inductor, resulting in a linearly increasing current through the device. **c**, Freewheeling state (OFF II), where the DUT again blocks the high voltage, and the inductor current is redirected through the freewheeling diode (FWD). **d**, Experimental waveforms at 20 mK for a 20 V V_{DC} supply with a 100 μs turn-on gate pulse. A gate-source voltage (V_{GS}) of 18 V is applied during the on-state, and -2 V during the off-state. A peak current of 0.5 A is observed during the turn-off transient.

System verification

The functionality of the cryogenic measurement system was verified by comparing its measurement results against those obtained from a standard test setup (**Supplementary Fig. 5**). In the standard setup, the DUT was characterized by using the fixture kit in the Keysight B1505A test system in Kelvin connection mode with a calibrated short measurement loop. The on-state resistance (R_{ON}) measured was ~ 110 mΩ at a V_{GS} of 20 V. In comparison, measurements performed using the proposed cryogenic system, which features a longer measurement loop and places the DUT in the low-temperature measurement plate, yielded an R_{ON} of 112 mΩ, representing a 2 mΩ increase. This difference corresponds to a measurement deviation of 1.8%. This deviation is potentially attributable to the additional overlap of force and sense lines on the PCB or to measurement ringing effects. Despite this minor discrepancy, the observed consistency validates the functionality and accuracy of the cryogenic test system operating in Kelvin connection mode for characterizing device behaviors.



Supplementary Figure 5 | System verification at room temperature. DUT's *I-V* characteristics are measured at room temperature using two different ways: the cryogenic system's long measurement loop (112 mΩ) and a standard short measurement loop (110 mΩ). The observed difference of 2 mΩ (1.8%) is attributed to potential resistance from additional overlapping PCB tracks in the force and sense lines, or inherent measurement uncertainties.

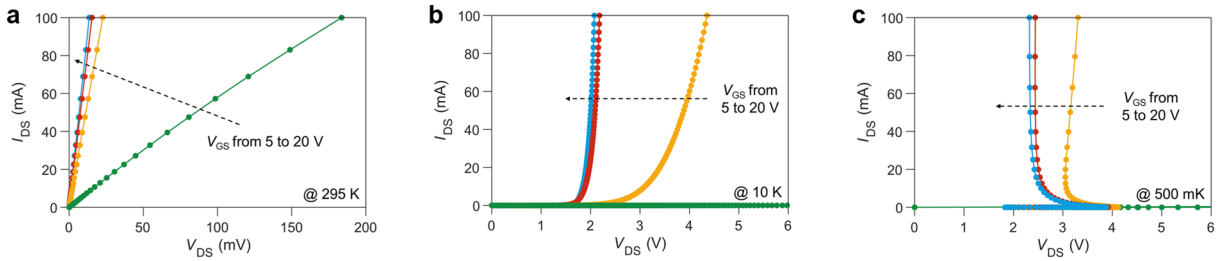
Supplementary Note 3. *I-V* characteristics of SiC MOSFET across a wide range of temperature and time

The automatically controlled measurement system facilitated long-term characterization across a wide range of temperatures and durations. Given the strong temperature-dependent nature of negative differential resistance (NDR), the *I-V* behavior of the DUT was first comprehensively characterized from room temperature (297 K) down to deep cryogenic temperatures. At 295 K, the device shows typical ohmic behavior when in the on-state (**Supplementary Fig. 6a**), where its resistance is primarily controlled by the applied V_{GS}. A V_{GS} of 5 V is sufficient to turn on the device, albeit with a relatively high R_{ON}, which decreases with increasing V_{GS}. As the temperature is lowered, the device transitions to a non-Ohmic regime, characterized by the emergence of a distinct turn-on voltage (V_{ON}) required for current conduction (**Supplementary Fig. 6b**). Notably, at low temperatures, a V_{GS} of 5 V is no longer sufficient to turn on the device, indicating a significant shift in its threshold voltage. The V_{ON} is dependent on V_{GS}, and the differential resistance in the on-state can also be modulated by adjusting V_{GS}. Below ~2 K, a gate-controllable NDR behavior becomes evident, even when viewed on *I-V* characteristics plotted in a linear scale (**Supplementary Fig. 6c**).

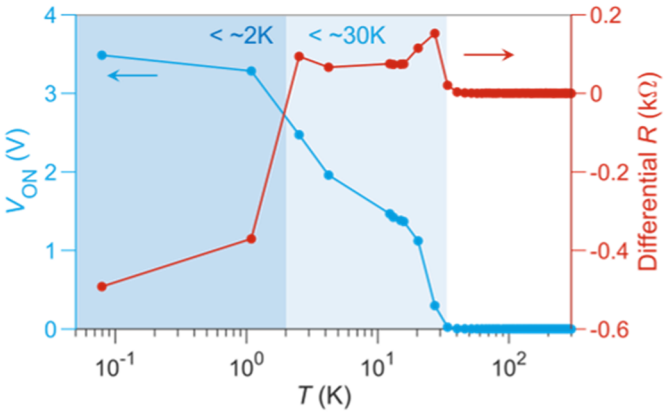
To provide a clear quantitative overview of these changes in the device's *I-V* characteristics, V_{ON} is defined as the voltage at a current of 1 mA, and the corresponding slope at this point is represented as the differential resistance (DR) value. **Supplementary Fig. 7** presents the full temperature measurement results

at a V_{GS} of 20 V, ranging from 297 K down to 80 mK. Initially, V_{ON} remains close to zero due to the low static R_{ON} at 20 V gate voltage, and the DR value is equivalent to the R_{ON}. As the temperature drops below 30 K, both V_{ON} and the DR value begin to increase, signifying the onset of non-Ohmic behavior. At cryogenic temperatures below 2 K, V_{ON} continues to increase, while the DR value transitions to negative. The peak V_{ON} and NDR value observed are 3.5 V and -0.5 kΩ, respectively.

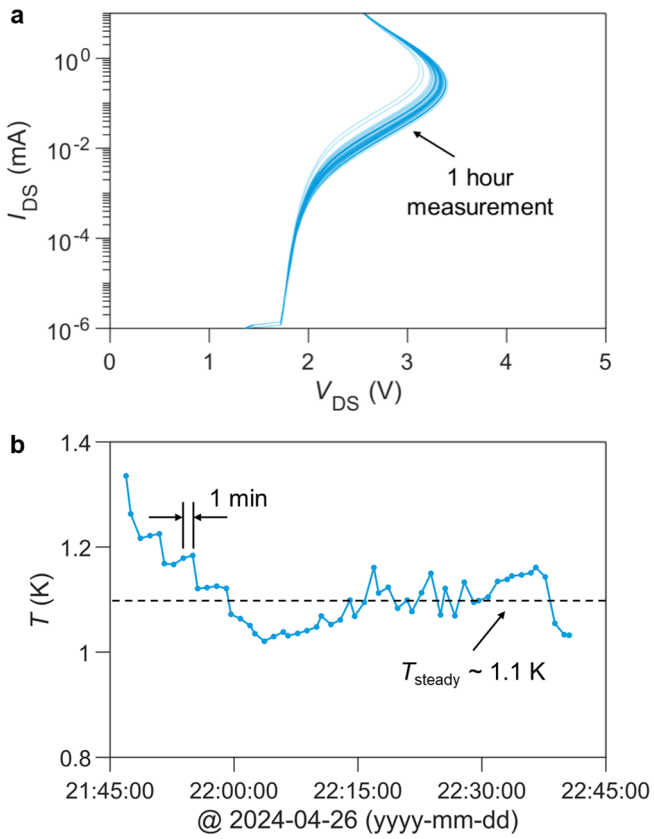
Long-term measurements were conducted at cryogenic temperatures below 2 K to assess the sustained functionality of the NDR. These one-hour measurement sessions comprised 55 sweeps for a single device. NDR behavior was consistently observed across all tests, with minor variations attributed to temperature fluctuations (**Supplementary Fig. 8a**). The overall temperature remained below 2 K, averaging ~1.1 K, with a small peak-to-peak variation of 0.3 K during the measurement period (**Supplementary Fig. 8b**). The thermal load imposed on the DUT during these static measurements prevented further cooling below 1 K, highlighting a limitation of the static characterization.



Supplementary Figure 6 | *I-V* characteristics of DUT at various temperatures with V_{GS} from 5 to 20 V. a, Current-sweep results at 295 K. The device exhibits typical ohmic behavior, where the drain-source voltage increases linearly with increasing current. The overall resistance is controlled by the applied gate voltage. **b**, *I-V* characteristics at 10 K. The device demonstrates non-ohmic behavior, requiring a distinct turn-on voltage (V_{ON}) for current conduction. **c**, *I-V* characteristics at 500 mK. The device shows gate-controllable negative differential resistance (NDR) behavior.



Supplementary Figure 7 | Temperature dependence of V_{ON} and DR value from 297 K to 80 mK at 20 V V_{GS}. V_{ON} is defined as the voltage at a current of 1 mA, while the differential resistance (DR) value represents the slope at the 1 mA operating point. The device maintains ohmic behavior until the temperature drops below 30 K, characterized by an increasing V_{ON} and positive DR. Below ~2 K, the DR value becomes negative, clearly indicating the onset of NDR behavior.



Supplementary Figure 8 | Long-term stability of NDR characteristics. a, *I-V* curves measured over a one-hour period. The observed shifts in NDR shape are attributed to subtle temperature variations during the measurement. **b,** Corresponding temperature profile recorded during the one-hour measurement, exhibiting a peak-to-peak variation of 0.3 K around an average temperature of ~ 1.1 K.

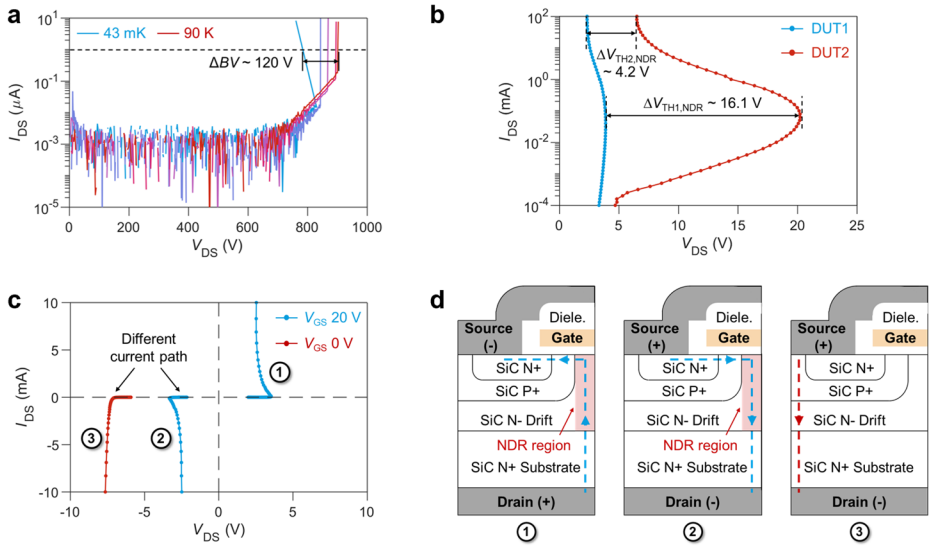
Supplementary Note 4. Further characterizations for understanding the origin of NDR

To elucidate the origin of the observed NDR, several additional characterization tests were conducted. Firstly, off-state *I-V* characteristics were measured across various temperatures with a V_{GS} of 0 V (**Supplementary Fig. 9a**). This characteristic effectively reveals the maximum blocking voltage of the internal P-N junction. While a 120 V drop in the breakdown voltage (*BV*) was observed as temperature decreased to 45 mK, the *BV*, extracted at 1 μA, remained above 800 V. As *BV* is much higher than the NDR onset voltage (~2.4 V), the NDR in SiC MOSFETs is not related to avalanche-induced breakdown behaviors, unlike NDR in thyristors.

Secondly, a SiC MOSFET with a 3300 V voltage rating (DUT2) was selected as a reference. Compared to the 650 V device (the main DUT in this study), the primary structural difference in the higher voltage-rated device is a thicker and lower-doped N-type drift region, designed to support its increased breakdown voltage. Characterization of both devices revealed significant differences in their NDR threshold voltages, with values of 16.1 V and 4.2 V observed for $V_{TH1,NDR}$ and $V_{TH2,NDR}$, respectively (**Supplementary Fig. 9b**). These findings indicate that a thicker and lower-doped drift region contributes to a wider voltage range for the NDR, confirming the critical role of carrier transport in drift region on the observed NDR behaviors.

Furthermore, the first- and third-quadrant *I-V* characteristics were tested at V_{GS} values of 0 V and 20 V (**Supplementary Fig. 9c**). When a V_{GS} of 20 V was applied, generating a current conduction channel beneath the gate structure and the JFET region (**Supplementary Fig. 9d**), NDR behaviors were observed in both quadrants. However, when a V_{GS} of 0 V was applied, the device remained in the off-state in the first quadrant, but current could flow through the body P-N junction in the third quadrant (**Supplementary Fig.**

9d). Under this scenario, no NDR was observed, indicating that the drift region beneath the gate is the primary determinant of the NDR behavior.



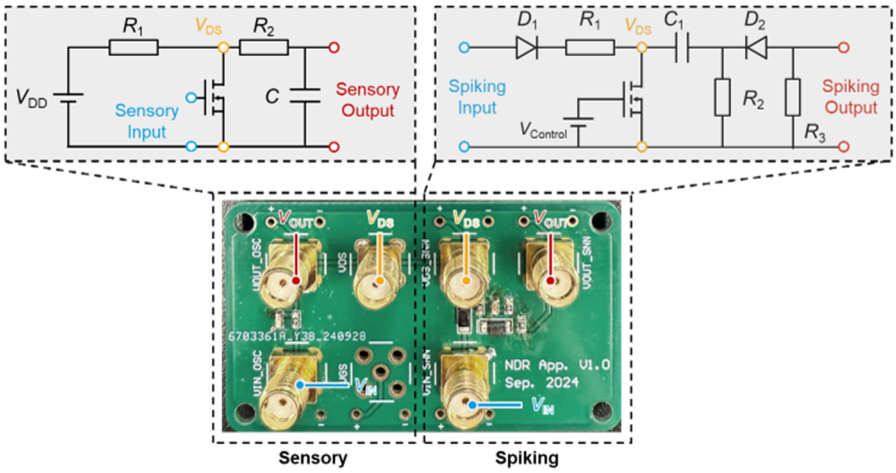
Supplementary Figure 9 | Key results elucidating the origin of NDR. a, Off-state *I-V* characteristics of the SiC MOSFET measured from 90 K to 43 mK. The breakdown voltages (*BV*s), extracted at a current of 1 μA, remained above 800 V, exhibiting a 120 V decrease as temperature was lowered. This high *BV* confirms that the observed NDR behavior at a few volts is not related to device breakdown. **b**, Comparison of NDR performance in SiC MOSFETs with different voltage ratings. DUT1 and DUT2 possess rated voltages of 650 V and 3.3 kV, respectively, with measurements conducted at temperatures of approximately 100-200 mK. Clear differences are observed in the NDR threshold voltages ($V_{TH1,NDR}$ and $V_{TH2,NDR}$), which are 16.1 V for DUT1 and 4.2 V for DUT2. These variations are primarily attributed to differences in the thickness of the drift region, a critical parameter designed for high-voltage blocking in the off-state and significantly influencing NDR performance. **c**, First-quadrant and third-quadrant NDR performance at V_{GS} of 20 V and 0 V. NDR behaviors are evident in both quadrants when a 20 V V_{GS} is applied. However, no NDR behavior is observed for the third-quadrant measurement at 0 V V_{GS}, indicating the device remains in the off-state. **d**, Device schematic illustrating the current flow through the device channel beneath the gate structure for both first (#1) and third quadrants (#2) when gate voltage is applied. Third-quadrant conduction path when no gate voltage is applied (#3). In this scenario, current flows through the body P-N diode formed by the N-type doped drift and substrate regions, and the P-type region, further supporting that the NDR originates from the drift region beneath the gate.

Supplementary Note 5. Electric circuits used for NDR applications

Demonstration circuits

Similar to the static measurement setup, the custom-designed PCB carries external electronic components, which are connected to the NDR device inside the cryogenic refrigerator via coaxial cables to enable various applications. This single PCB board (**Supplementary Fig. 10**) facilitates the demonstration of three types of neuron applications: sensory neurons, spiking-based logic neurons, and integrate-and-fire neurons.

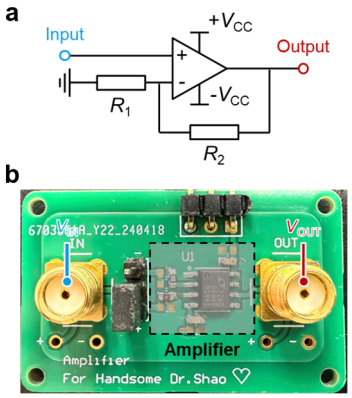
The left portion of this PCB is dedicated to the sensory neuron circuit, featuring three SMA connectors for signal measurement and transmission. The resistance and capacitance values within this circuit are adjustable. The right side of the PCB is designed for spiking circuits, supporting both spiking-based logic and integrate-and-fire applications. The functionality of this circuit can be reconfigured between these two application types by altering the gate driving scheme: when a V_{GS} is used as the trigger signal, the circuit functions as a logic neuron, whereas applying a steady DC voltage enables its operation as an integrate-and-fire neuron. All components on the PCB are interchangeable, and a basic reset function can be implemented by changing the blocking diode (D_1) to an additional transistor. Furthermore, cascading two such PCBs allows for the realization of cascaded integrate-and-fire neurons.



Supplementary Figure 10 | Photo and schematic of PCB used for NDR application. This PCB integrates two distinct circuit schematics: one for the sensory neuron (left side) and another shared schematic for both the spiking-based logic neuron and the integrate-and-fire neuron (right side). The latter two neuron types utilize the same circuit configuration but are differentiated by their control mechanisms.

Amplifier for cascaded neuron

To accelerate the voltage integration process within the cascaded neuron structure, a signal amplifier was employed to boost the output of the first-stage integrate-and-fire neuron. A non-inverting amplifier circuit (**Supplementary Fig. 11**) was constructed using an LTC6090-5 amplifier, selected for its high voltage range (±70 V), high bandwidth (up to 68 kHz), and fast response time (< 1 μs). The custom-designed PCB for this application accommodates all necessary components, including two resistors (R_1 and R_2) that determine the amplifier's gain. Operating with a ±12 V supply voltage (V_{CC}), the circuit achieved a gain of 31, set by R_1 = 1 kΩ and R_2 = 30 kΩ. The input signal for this amplifier was connected via an SMA connector to the output of the first-stage integrate-and-fire neuron, and its amplified output was then directed to the input of the second stage.



Supplementary Figure 11 | Non-inverting amplifier for cascaded neuron. a, Circuit schematic of the non-inverting amplifier, detailing its configuration and component connections. **b**, Photo of the amplifier PCB.

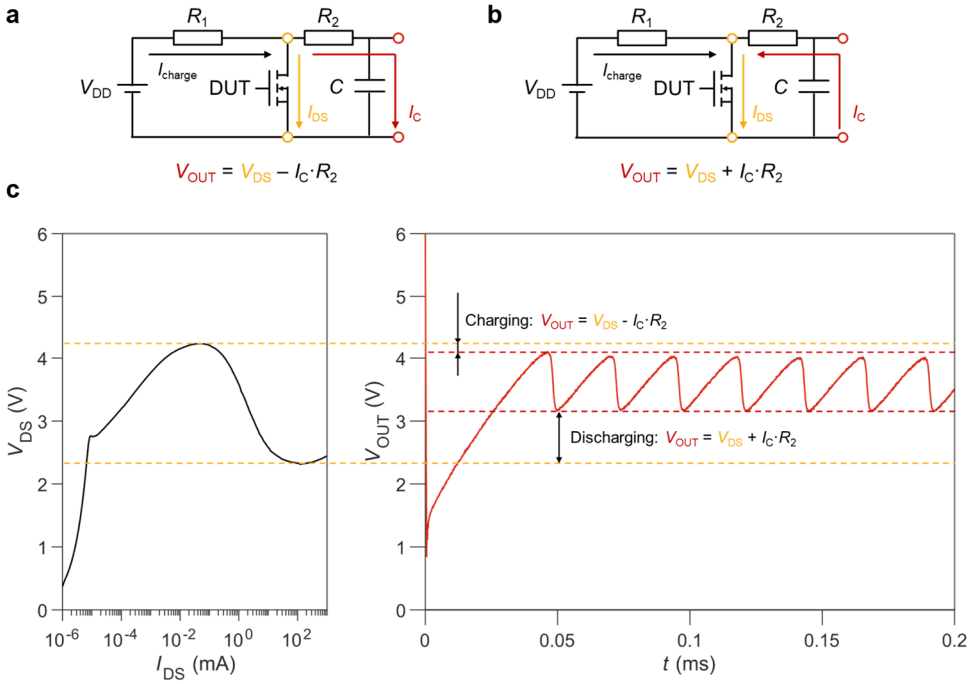
Supplementary Note 6. Working principles and output degradation of sensory neuron

A sensory neuron based on the NDR device was thoroughly investigated under various conditions. The equivalent circuits during the charging and discharging processes are analyzed in **Supplementary Figure 12a** and **Figure 12b**, respectively. In this setup, R_2 represents the equivalent parasitic resistance introduced by the long cables, which causes a voltage variation between the output voltage (V_{OUT}) and the V_{DS}. During the charging process, the current flows through R_2 to charge capacitor C, resulting in V_{OUT} being lower than

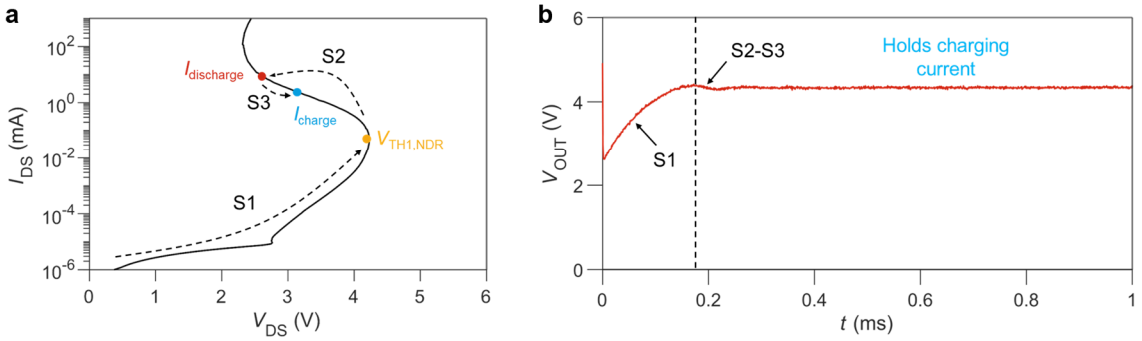
V_{DS}. Conversely, when C discharges, V_{OUT} becomes higher than V_{DS}. This analysis effectively explains the observed differences between the peak (V_{peak}) and bottom voltages (V_{bottom}) of V_{OUT} and the intrinsic NDR threshold voltages (**Supplementary Fig. 12c**). The impact of R_2 is more pronounced during the discharge process due to the larger current involved in triggering device oscillation.

To further analyze the oscillation behavior in the sensory neuron, tests were conducted under various supply voltages (V_{DD}) while maintaining constant circuit parameters. At low V_{DD}, a non-oscillation scenario can be observed (**Supplementary Fig. 13a**). In this mode, the device undergoes a pre-charging process, but oscillation does not occur after the initial drop in V_{DS}. Unlike the oscillation mode, the peak discharge current in this non-oscillatory state is insufficient to drive the operating point out of the NDR region. This leads to a "drive-back" phenomenon in the S-shape curve, resulting in an increase in V_{OUT} but a decrease in current as the transient discharge from C ceases. This drive-back behavior is clearly visible in the switching waveforms under a 5 V V_{DD} (**Supplementary Fig. 13b**). V_{OUT} then stabilizes at a steady value after the initial drop, corresponding to a voltage within the NDR region determined by the charging current controlled by V_{DD} and R_1. This distinct non-oscillation behavior elucidates the working principle of the sensory neuron and its trigger requirements: a higher discharge current is necessary to exit the NDR region and initiate oscillation; otherwise, the device remains within the NDR region and gets into steady state.

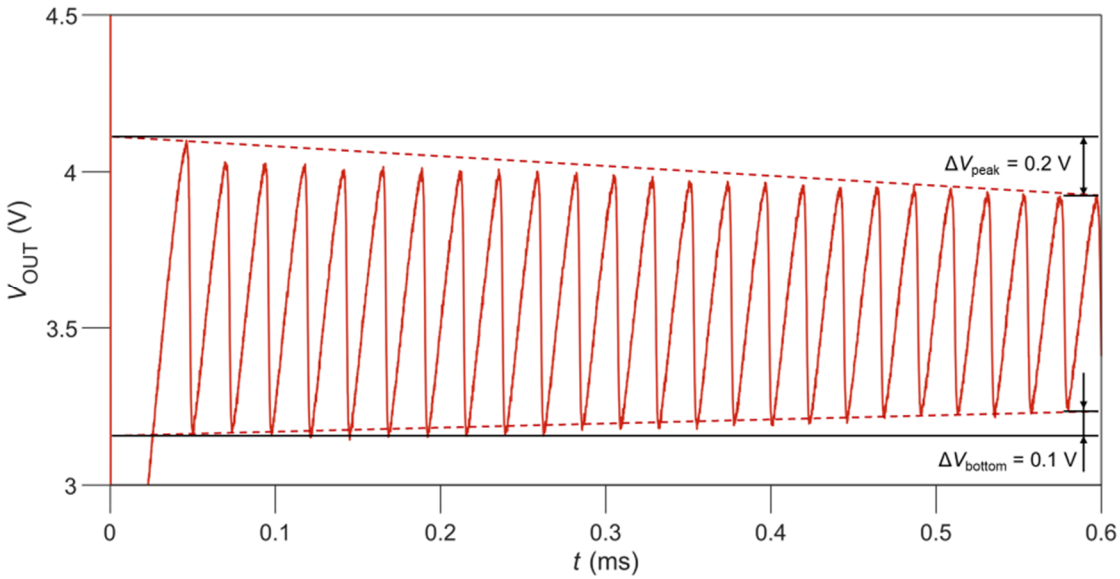
Additionally, a damping phenomenon is observed during oscillation, characterized by a decrease in the V_{peak} and an increase in V_{bottom} (**Supplementary Fig. 14**). Differences of ~0.2 V for V_{peak} and 0.1 V for V_{bottom} can be extracted from the waveforms. This phenomenon is explained by self-heating-induced changes in the NDR characteristics. As temperature increases, $V_{TH1,NDR}$ decreases while $V_{TH2,NDR}$ increases, making the S-shape I-V curve appear more linear-like. The drop in $V_{TH1,NDR}$ leads to a decrease in V_{peak}, and correspondingly, the increase in $V_{TH2,NDR}$ results in a higher V_{bottom}.



Supplementary Figure 12 | Working principles of sensory neuron. a, Circuit schematic during the charging process. Current flows through DUT and the R_2C branch, resulting in an output voltage (V_{OUT}) that is smaller than V_{DS}. **b**, Circuit schematic during the discharging process. Owing to the voltage drop across the NDR region of the DUT, the capacitor (C) discharges, causing V_{OUT} to be larger than V_{DS}. **c**, Comparison of the threshold point between the DUT's intrinsic characteristics and the sensory neuron's output signal.



Supplementary Figure 13 | Non-oscillation scenario for the sensory neuron. a, Operation stages under non-oscillation conditions. When DUT turns on, the device and the R_2C branch are charged to a higher voltage level (S1) until reaching the NDR threshold. Due to insufficient discharging current, the device's operating point cannot exit the NDR region (S2). The voltage at the end of S2 cannot be sustained as the transient discharging current ceases. Consequently, the device voltage drives back to a higher value with a lower current (S3) and enters a steady state. The steady current is then supplied by the applied power supply (V_{DD}). **b**, Waveforms of V_{OUT} when a 5 V V_{DD} is applied, illustrating a steady-on state achieved after the initial discharging process.



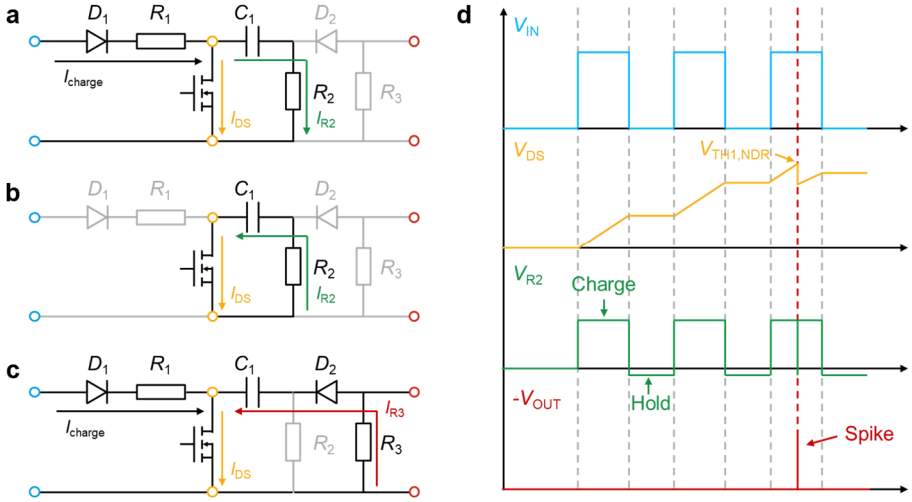
Supplementary Figure 14 | Damping phenomenon of the sensory neuron during a single operation. The switching waveforms are extracted under a 10 V V_{DD} with an R_1/C combination of 9 kΩ/10 nF. Over the duration of the pulse, the peak oscillation voltage decreases by ~0.2 V, while the bottom voltage increases by ~0.1 V.

Supplementary Note 7. Working principles and gate controllable demonstration for spiking neurons

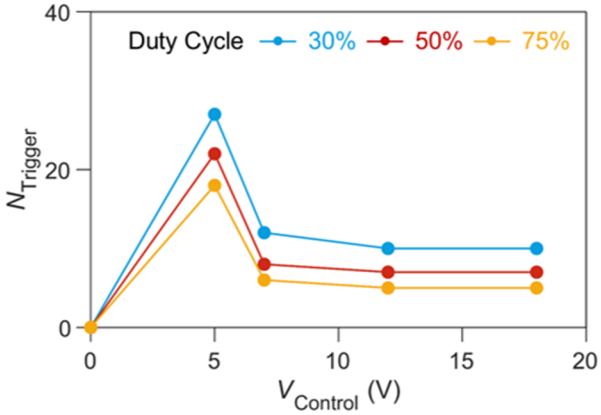
The spiking logic neuron and integrate-and-fire neuron, while serving distinct functions, are both based on the same fundamental circuit structure, differentiated by their gate control strategies. Taking the integrate-and-fire application as an example, the V_{DS} integrates incoming input spikes, with current flowing through the DUT and the R_2C_1 (1 kΩ/1 μF) branch (**Supplementary Fig. 15a**). During the intermittent periods between input spikes, diodes D_1 and D_2 block the discharge path of C_1, allowing V_{DS} to remain steady. This stability requires only a small current to maintain the DUT's voltage, which is supplied by the R_2C_1 branch (**Supplementary Fig. 15b**). When the integrated V_{DS} reaches the $V_{TH1,NDR}$, a sudden drop in V_{DS} is initiated by the NDR characteristics, leading to a rapid discharge of C_1. A smaller resistor R_3 (50 Ω) and D_2 form the

discharge path, generating a high transient current (**Supplementary Fig. 15c**). **Supplementary Figure 15d** illustrates the ideal waveforms of the input spikes (V_{IN}), V_{DS}, voltage across R_2 (V_{R2}), and voltage across R_3 (also represented as V_{OUT}). While the V_{R2} is positive during charging and negative during intermittent periods, V_{OUT} exhibits a negative output only when NDR is triggered, accurately mimicking the behavior of an integrate-and-fire neuron.

Owing to the gate-controllable NDR behavior, the number of input pulses required to trigger an output ($N_{Trigger}$) can be adjusted by varying the gate control voltage ($V_{Control}$), which in turn modifies $V_{TH1,NDR}$. Additionally, the input pulse width also impacts on the V_{DS} integration process, offering another means to alter $N_{Trigger}$ (**Supplementary Fig. 16**). A higher $V_{Control}$ and wider input pulses facilitate faster triggering, accommodating diverse application requirements for integrate-and-fire neurons.



Supplementary Figure 15 | Illustration of the working principles of spiking neurons. a, Circuit schematic during the charging stage. Current flows through the DUT and the R_2C_1 branch, causing an increase in V_{DS}. **b**, Circuit schematic during the intermittent stage. The device voltage is sustained by the current supplied through the R_2C_1 branch. **c**, Circuit schematic illustrating the spike transient. R_3 (50 Ω) has a significantly smaller value than R_2 (1 kΩ), providing a high-current discharge path for the spike. **d**, Ideal waveforms of a spiking neuron. The input signal is integrated until V_{DS} reaches the $V_{TH1,NDR}$. A distinct output spike can then be measured across R_3, resulting from the large transient discharging current.



Supplementary Figure 16 | Gate-controllable firing behavior of integrate-and-fire neurons. The number of input pulses required to trigger an output ($N_{Trigger}$) are shown as a function of the control voltage ($V_{control}$) for various input pulse duty cycles. The data demonstrates that higher duty cycles necessitate fewer pulses to trigger an output. Additionally, increasing $V_{control}$ effectively decreases the NDR threshold voltage, thereby enabling a faster neuron firing response.