Supplementary Materials
Common Mode Control and Confinement Inversion of Electrostatically Defined Quantum Dots in a Commercial CMOS Process

Andrii Sokolov[1,*,+], Xutong Wu[1,2,+], Conor Power[1,2,+], Mike Asker[3], Panagiotis Giounanlis[1], Ioanna Kriekouki[1], Pèter Hanos-Puskai[4], Conor McGeough[1], Imran Bashir[3], David Redmond[1], Dirk Leipold[3], Bogdan Staszewski[1,2], and Elena Blokhina[1,2]

[1]Equal1 Laboratories, Dublin, D04 V2N9, Ireland
[2]Centre for Quantum Engineering, Science, and Technology and School of Electrical and Electronic Engineering, University College Dublin, Dublin, D04 V1W8, Ireland
[3]Equal1 Laboratories, San Carlos, CA 94070, California, USA
[4]Equal1 Laboratories Romania SRL, 300124, Timișoara, Romania
[*]andrii.sokolov@equal1.com
[+]these authors contributed equally to this work

ABSTRACT

1 QTCAD Model Calibration

As discussed in the main text, the QTCAD model requires calibration, as it is very sensitive to a slight change of input parameters. One calibration method is to measure a DC current through the device and fit it with a simulated DC current. However, this is not feasable in cryogenic semiconductor devices, since the traditional Poisson equations are singular at $T \lessapprox 70$ K. QTCAD does not provide DC leakage current through the device, however, it can predict the biasing voltages of Coulomb blockade transitions and tunneling current using the WKB approximation and the Non-Equilibrium Greens Functions (NEGF) framework[1].

The device considered in the main text is too large for calibration, given the size of its geometry and the number of input voltages, which increases the variability of results. Hence, experimental data from the 22 nm FD-SOI minimum size transistor (Fig. 1 (a)) was chosen. The DC measurements at $V_{\mathrm{CM}} = -400$ mV show a single clear Coulomb diamond, see Fig. 1 (b),(c). This implies that the device under test has a very shallow quantum well that can produce a single Coulomb blockade event before fully conducting. We then calibrated a model of this minimum size transistor to produce this same shallow well response, the calibrated parameters of which are then used in the full QDA model. We describe this calibration next.

The only possible configuration of the quantum well for the single-gate transistor is when the potential minimum is below the Fermi level and under the gate oxide, and potential barriers are higher than the Fermi level and forming below the spacers, see Fig. 1 (d). Therefore, as a first step, a sweep over the wide range of input parameters was applied:

- Common mode voltage $-0.6\ \mathrm{V} \leqslant V_{\mathrm{CM}} \leqslant -0.4\ \mathrm{V}$, in steps of 20 mV.
- Gate-source voltage $0\ \mathrm{V} \leqslant V_{\mathrm{GS}} \leqslant 0.65\ \mathrm{V}$, in steps of 50 mV.
- Wide sweep of n-dopants concentration in the channel under the source and the drain.
- Tuning of the gate and backgate workfunctions.

The given parameters are chosen to be close to the expected ones. In total, this results in 9702 simulations that are not feasible to analyse manually. Hence, the following automatic algorithm was used:

1. Solve the Poisson equation with QTCAD at the given set of parameters.
2. Select three line cuts in the Silicon channel (at height 0.1 nm, 3.0 nm and 5.9 nm from the top of the channel).

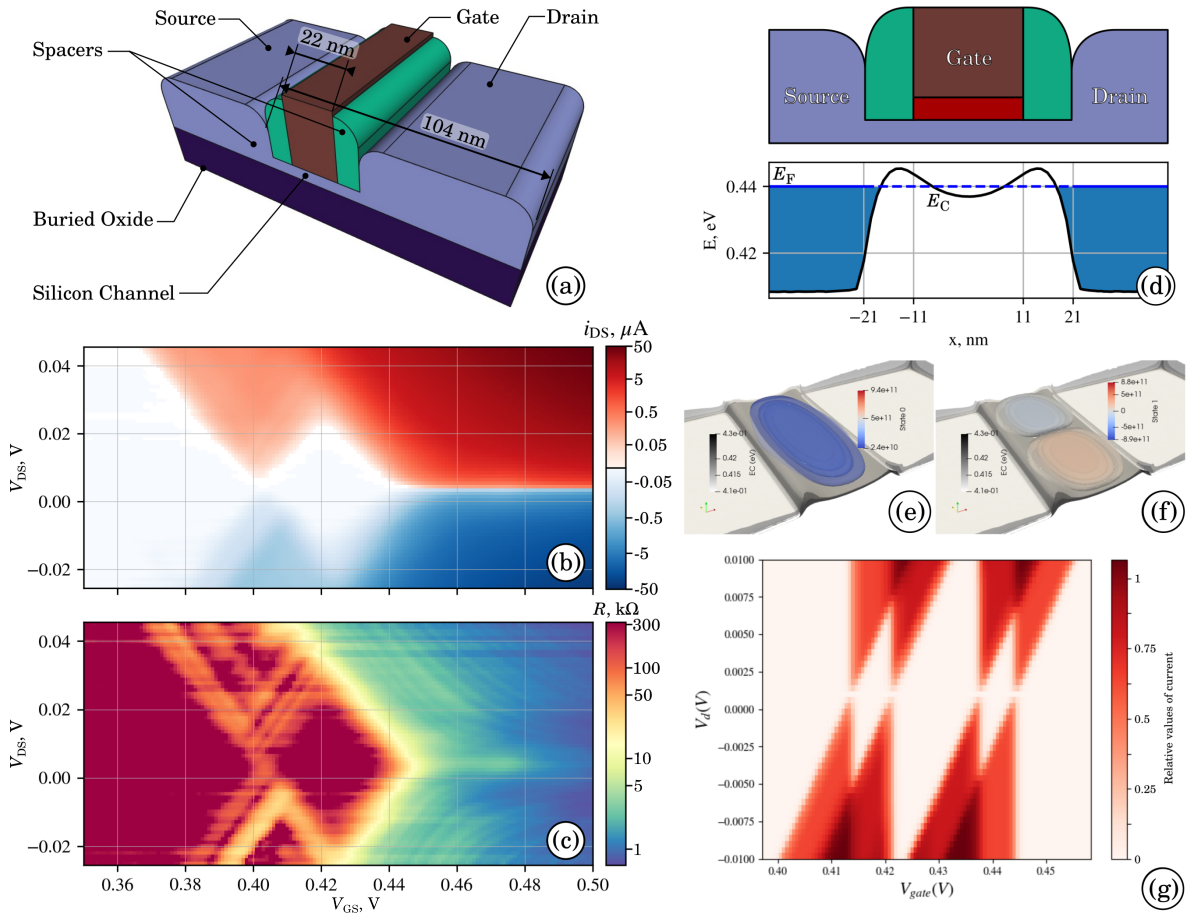

Figure 1. Experimental demonstration of the Coulomb blockade in the minimal feature size standard transistor. (a) The geometry of the transistor with a pitch of 104 nm and gate width of 22 nm. (b) The positive and negative drain-source DC current through the transistor (at $V_{CM} = -400$ mV). (c) Calculated resistance through the transistor. (d) The QTCAD simulation results for the minimal feature size FDX-22 transistor. 1D line cut of the conduction band aligned with the schematic view of the transistor. Blue areas correspond to the quantum leads. The black line is the conduction band edge. The blue dashed line is the Fermi level at the source and drain. (e) The wavefunction that corresponds to the ground state — blue-to-red colours correspond to the wavefunction, and the grayscale colours — equipotential surfaces. (f) The wavefunction that corresponds to the first excited state. (g) Coulomb diamonds were simulated using the master equation.

3. Define the maximal, E_C^{max}, and minimal, E_C^{min}, values of the conduction band edge (the minimal value is defined under the gate not including the source and drain regions).

4. Define the Fermi level, E_F, under the source and drain (since the source/drain voltages are set by the shifting of the Fermi levels under the source and the drain).

5. The set of parameters is considered to be valid if $E_C^{min} < E_F < E_C^{max}$.

The given algorithm filtered 58 valid sets of parameters of the 9702 tested. An example of a valid 1D line cut of the conduction band is shown in Figure 1 (d). The conduction band edge that forms the dedicated quantum well makes it possible to calculate the single-electron wavefunctions, see Fig. 1 (e),(f). The depth of all analysed quantum wells is such that it can localize up to three quantum levels inside, all other wavefunctions will form outside of the barriers. This allows one to calculate the lever arm of the quantum dot and compare it with an experimental one (≈ 0.8eV/V, method outlined in[2] and data shown in Figs. 1(b),(c)). The closest simulated lever arm was ≈ 0.83 eV/V, extracted using QTCAD.

The final stage of the calibration was to match the position of the Coulomb peaks in simulations with one in experiments. QTCAD uses the master equation method to calculate the positions of the Coulomb peaks, and to reduce computational complexity it linearizes the single-electron energies in a quantum dot, which makes the shape of the Coulomb diamond straight,

see Fig. 1 (g). All 58 candidate sets of parameters were analysed and the closest parameters were used in the simulations of the minimum size transistor and the QDA in the main text.

2 Operation Modes of The Quantum Dot Array

One of the key experiments is the so-called flat band experiment. The idea of this experiment is to apply equal gate-source voltages to all gates with the negative common-mode voltage sweep. The experiments shown here were done on an older generation device with two techniques — direct current measurements, see Fig. 2 (a), and RF-reflectometry measurements, see Fig. 2 (b). The DC measurements demonstrate the conduction-to-nonconduction transition, showing a diagonal pattern similar to the results shown in the main text flat band simulation. The RF-reflectometry doesn't have such a direct connection to the conductance of the structure but demonstrates the different well-configurations discussed in the main text. At low V_{GS} and high V_{CM}, there is one type of pattern evident, but at higher V_{GS} and lower V_{CM} the pattern changes. This was our initial evidence of a transformation in the conduction band.

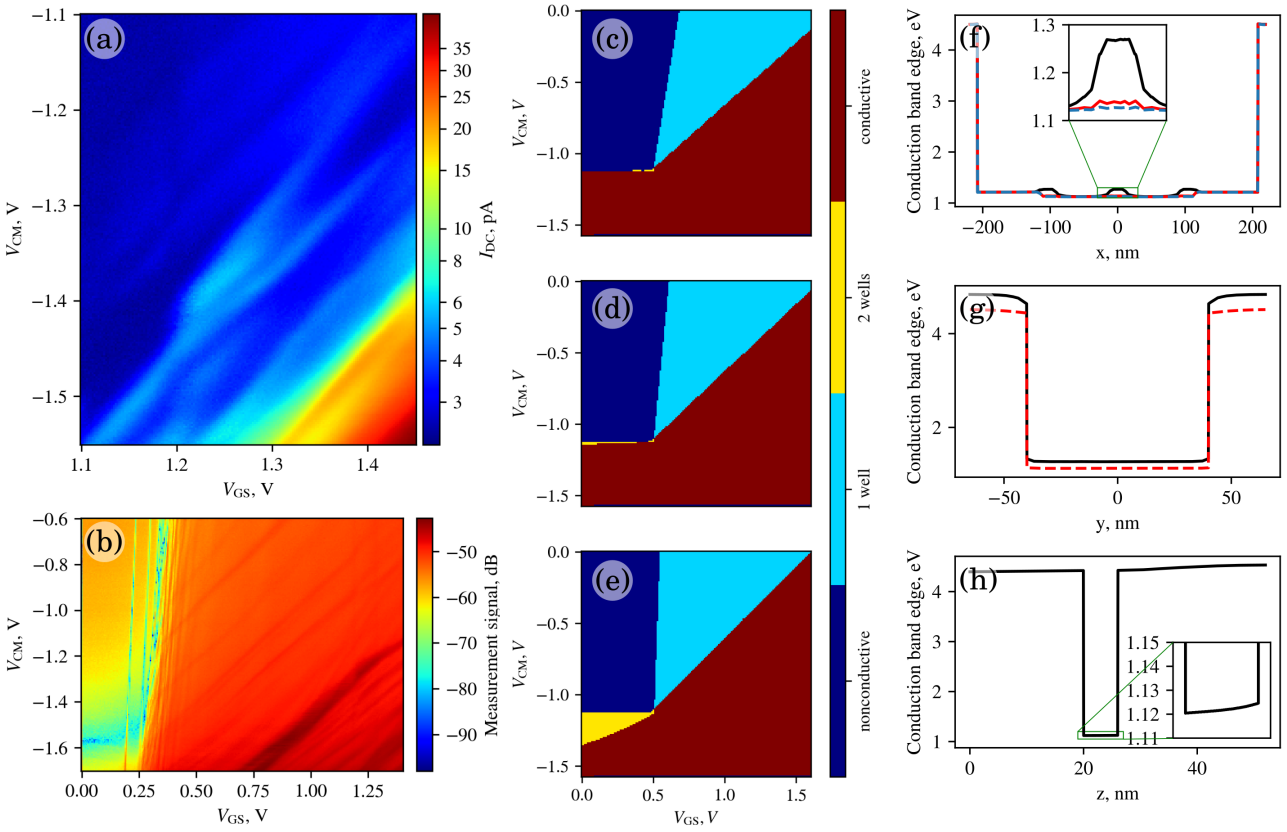

Figure 2. The flat band experimental and simulation results on an older generation device with three barrier gates. (a) 3.6 K DC measurements with $V_{DS} = 20$ mV. The same value of V_{GS} was applied to all three barrier gates for this sweep (b) 3.6 K RF reflectometry measurements with center frequency $f = 236.255$ MHz, and $V_{DS} = 0$. (c) In the flat band QTCAD simulation results (built the same way as the one from the main text), the line cut is taken at the bottom of the silicon channel (close to the buried oxide). (d) A similar graph when the line cut is taken in the middle of the channel. (e) When the line cut is taken close to the top interface. (f) An example of the line cut graphs along the x-axis $V_{GS} = 200$ mV, $V_{CM} = -1.25$ V. The solid black line is close to the interface, the solid red line is in the middle of the channel, and the blue dashed line is taken close to the buried oxide. The inset in the centre is a zoomed-in barrier. (g) The line cuts are taken along the y-axis at the same biasing condition. A solid black line is taken under the gate, the red dashed line is taken between the gates. (h) The z-cut was taken between the gates at the same biasing conditions. The inset is a zoomed-in section showing the bottom of the potential well.

The conduction band edge has a complicated 3D shape, therefore, it is not straightforward to analyse the data obtained from the QTCAD simulations. The confinement was classified at three different Z-level line cuts — close to the buried oxide in Fig. 2 (c), in the geometrical centre of the silicon channel in Fig. 2 (d) and one that is close to the interface below the barrier gates in Fig. 2 (e). The biggest difference is the double-well (yellow) region, where wells are forming between the barrier gates in the channel. This happens because the potential barriers between wells vary strongly with the Z-direction, see Fig. 2 (f) showing X-direction line cuts at the three Z-cuts. Figure 2 (g) shows the Y-cut of the conduction bands under the barrier gates and between the barrier gates which shows strong confinement in this direction. Figure 2 (h) shows the Z-cut of the conduction

band edge between the barrier gates. This shows strong confinement in the Z-direction, however, the bottom of a quantum well has a triangular shape, causing the wavefunction to be closer to the silicon oxide interface below the barrier gates. This may partly explain the high charge noise of this older generation device given the proximity to the upper oxide interface and charge trapping events.

3 Measurement Setup

The RF carrier frequency used is approximately 264MHz and the power of the RF signal is optimized to -50dBm for clearest reflectometry signals. The signal is attenuated at both the 40 K and the 4 K stages of the refrigerator to reduce thermal noise and then also further attenuated by the directional coupler. The signal power incident on the PCB sample board is approximately -80dBm. The RF carrier is reflected by the tank circuit on the PCB sample board and amplified by a cryogenic amplifier at 4 K after the directional coupler. The RF carrier is then amplified again at room temperature, and digitized at 1 GS/s. DC- and low-frequency voltages are generated using a QDevil QDAC-II[3] high-precision low-noise digital-to-analogue converter and transmitted through an 84-pin flex cable from room temperature to the 1K stage. The QDAC-II is triggered by the OPX+, and the DC voltages are loaded to the QDAC-II in advance and swept by trigger signals from the OPX+. This allows for synchronization between DC voltage sweeps and RF reflectometry readout. The experimental setup employed in this study is shown in Fig. 3.

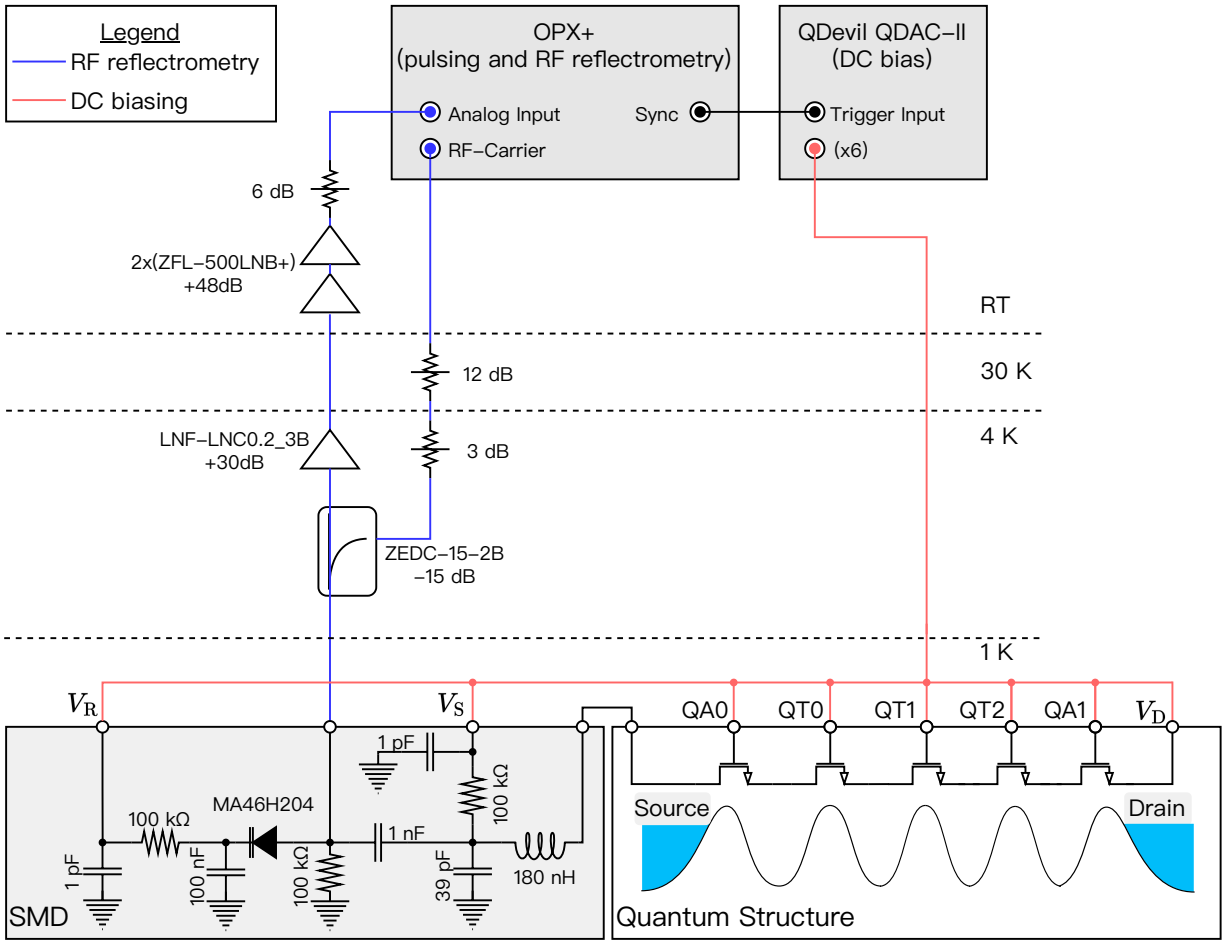

Figure 3. Experimental setup. The cryostat has a base temperature of 1.0 K. A QDevil QDAC-II was utilized to generate the DC signals at low frequencies. A Quantum Machines OPX+ is used for RF reflectometry.

4 Flat Band Zoomed

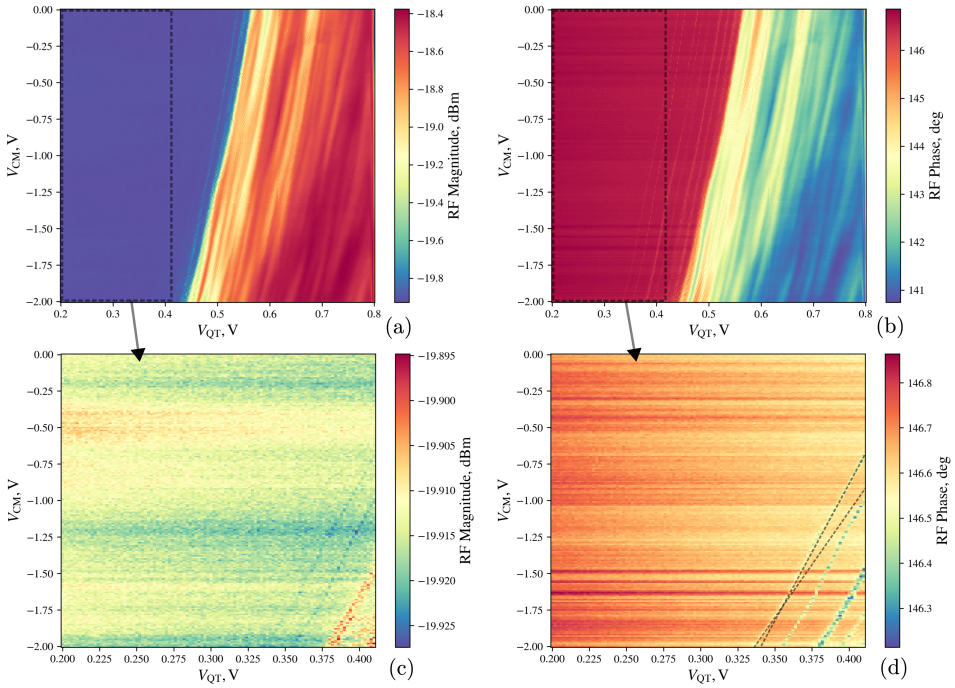

Figure 4. Flat band measurement results showing both magnitude and phase response. The characteristic slope between the conducting and non-conducting regions is clearly visible in the RF magnitude (a) and RF phase measurements (b) for a V_{CM} sweep. Zoomed-in flat band measurement results are shown in (c), and (d) to highlight Coulomb blockade transitions moving towards the fully conducting region.

5 Coulomb Diamond Measurement

A measurement of Coulomb diamonds was made of the device discussed in the main paper. The measurement results are presented below in Fig. 5 along with an example calculation of the leverarm extracted using the slopes of two intersecting lines[2]. The hand calculation shows very close matching with the leverarm predicted by QTCAD simulation (≈ 0.261 eV/V in simulation, see the main text).

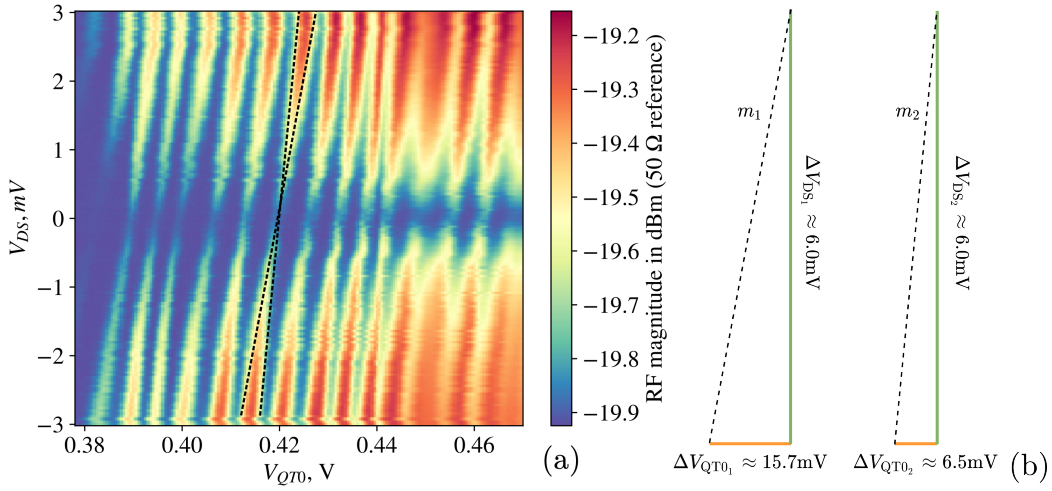

Figure 5. Charge stability diagram of the quantum dot forming between QA0 and QT0.

The details of the hand calculation to extract the leverarm, which is then scaled by the electron charge e.

$$m_1 = \frac{\Delta V_{\mathrm{DS}_1}}{\Delta V_{\mathrm{QT0}_1}} \approx \frac{6}{15.7} \approx 0.3822 \tag{1}$$

$$m_2 = \frac{\Delta V_{\mathrm{DS}_2}}{\Delta V_{\mathrm{QT0}_2}} \approx \frac{6}{6.5} \approx 0.9231 \tag{2}$$

$$\alpha = \frac{m_1 m_2}{m_1 + m_2} \approx \frac{(0.3822)(0.9231)}{0.3822 + 0.9231} \approx 0.2703 \text{ V/V} \tag{3}$$

$$e\alpha = 0.2703 \text{ eV/V} \tag{4}$$

An approximate V_{QT0} distance of 5.4045 mV is measured for the blocked current region to the right of the slopes annotated in Fig. 5, denoted ΔV_{add}. This gives a rough indication of the addition energy, E_{add}, of the quantum dot at this filling using the following formula[4]:

$$E_{\mathrm{add}} = e\alpha\Delta V_{\mathrm{add}} \approx (0.2703)(5.4045 \times 10^{-3}) \text{ eV/V} \approx 1.4608 \text{ meV} \tag{5}$$

This is in reasonable agreement with another device with smaller quantum dots in the literature, which results in somewhat higher addition energies (≈ 5 meV)[5].

References

1. QTCAD: A Computer-Aided Design Tool for Quantum-Technology Hardware, Nanoacademic Technologies Inc. (2022).
2. Venkatachalam, V., Hart, S., Pfeiffer, L., West, K. & Yacoby, A. Local Thermometry of Neutral Modes on the Quantum Hall Edge, DOI: 10.48550/arXiv.1202.6681 (2012). ArXiv:1202.6681.
3. Quantum Machines, www.quantum-machines.co.
4. Kouwenhoven, L. P., Austing, D. G. & Tarucha, S. Few-electron quantum dots. *Reports on Prog. Phys.* **64**, 701–736, DOI: 10.1088/0034-4885/64/6/201 (2001).
5. Lim, W. H., Huebl, H., Angus, S. J., Clark, R. G. & Dzurak, A. S. Electrostatically defined few-electron double quantum dot in silicon. *Appl. Phys. Lett.* 3 (2009).