

Supplementary Information

1 Material parameters

Table 1-2 itemize the material parameters used in Equation 1 - 3 for determining the carrier trap occupation probabilities.

Table 1 Material parameters for Al₂O₃/p-Si interface

Variable	Unit	Description	Value	Ref.
m_e^*	kg	Electron effective mass	$0.36m_0$	[1]
m_h^*	kg	Hole effective mass	$0.81m_0$	[1]
v_n	m/s	Electron thermal velocity	2.3×10^5	[1]
v_p	m/s	Hole thermal velocity	1.65×10^5	[1]
n_i	cm^{-3}	Intrinsic carrier conc.	1.5×10^{10}	[1]
E_i	eV	Intrinsic energy level	0.56	[1]
E_c	eV	Conduction band edge	1.12	[1]
E_v	eV	Valence band bottom	0	-
σ_n	cm^2	Electron trap cross section	1×10^{-17}	user
σ_p	cm^2	Hole trap cross section	1×10^{-15}	user
E_{tA}	eV	Trap level	0.5	user
F_{deg}	NA	Degeneracy Factor	9	user
d	nm	Trap depth	6.4	user

T = 300 K, q = 1.6e-19 C, $\hbar=1.0546e-34$ J-s, $m_0 = 9.11e-31$ kg

Table 2 Material parameters for Al₂O₃/n-InP interface

Variable	Unit	Description	Value	Ref.
m_e^*	kg	Electron effective mass	$0.08m_0$	[2]
m_h^*	kg	Hole effective mass	$0.60m_0$	[2]
v_n	m/s	Electron thermal velocity	3.9×10^5	[2]
v_p	m/s	Hole thermal velocity	1.7×10^5	[2]
n_i	cm^{-3}	Intrinsic carrier conc.	1.3×10^{10}	[2]
E_i	eV	Intrinsic energy level	0.672	[2]
E_c	eV	Conduction band edge	1.34	[2]
E_v	eV	Valence band bottom	0	-
σ_n	cm^2	Electron trap cross section	8.60×10^{-18}	[3]
σ_p	cm^2	Hole trap cross section	3.11×10^{-16}	[3]
E_{tA}	eV	Trap level	0.5	user
F_{deg}	NA	Degeneracy Factor	9	user
d	nm	Trap depth	6.4	user

T = 300 K, q = 1.6e-19 C, $\hbar=1.0546e-34$ J-s, $m_0 = 9.11e-31$ kg

Table 3 outlines the various epitaxial layers used in the III-V/Si micro-ring laser.

Table 3 III-V/Si Epitaxial wafer stack for non-volatile micro-ring laser

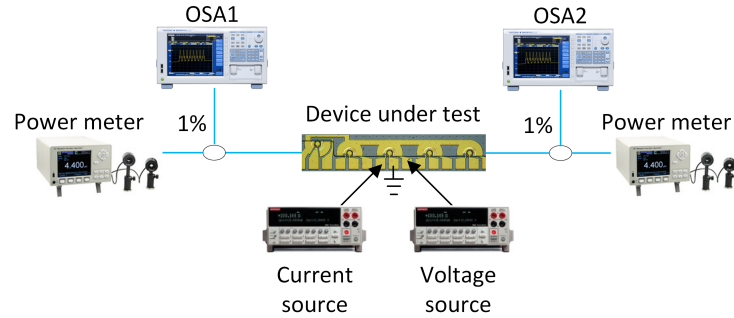
Layer	Material	Al	In	Ga	As	P	Strain (%)	Height (nm)	Doping (/cm ³)
p-contact	InGaAs	0	0.53	0.47	1	0	-	200	Zn:>1E19
p-clad	InP	0	1	0	0	1	-	1500	Zn:2→0.5E18
p-GRIN	InGaAsP	0	0.89	0.11	0.24	0.76	-	100	Zn:5→3E17
p-SCH	InAlAs	0.5	0.5	0	1	0	-	20	Zn:>2E17
i-InGaAsP	InGaAsP	0	0.89	0.11	0.24	0.76	-	50	nid
QW (6x)	InGaAsP	0	0.86	0.14	0.55	0.45	+0.8	6.5	nid
Barrier (7x)	InGaAsP	0	0.84	0.16	0.29	0.71	-0.19	9.0	nid
i-SCH	InGaAsP	0	9.89	0.11	0.24	0.76	-	50	nid
n-contact	InP	0	1	0	0	1	-	110	S:2E18
n-S.L.1 (2x)	InGaAsP	0	0.85	0.15	0.327	0.673	-	7.5	S:2E18
n-S.L.2 (2x)	InP	0	1	0	0	1	-	7.5	S:2E18
n-Bond layer	InP	0	1	0	0	1	-	10	S:2E18
dielectric	Al ₂ O ₃	0	0	0	0	0	-	10	-
Waveguide	Si	0	0	0	0	0	-	300	-

SCH: separate confinement heterostructure, GRIN: graded index, QW: quantum well, S.L.: super-lattice, nid: non-intentionally doped

2 Experimental Section

2.1 Measurement Setup

The 100 mm wafer is vacuum mounted onto a temperature controlled stainless steel chuck via a semi-automatic probe station. The experimental setup is shown in Figure 1. All endurance and cyclability measurements of the non-volatile MRL lasers are all automated with a PC. Current injection and MOSCAP phase tuning (volatile and non-volatile) is performed with a Keithley Source Meter (2400). Light is vertically collected from the devices via grating couplers with a 7° polished fiber array. Optical power is measured with Newport power meters (1936-R) and detectors (818-IG-L-FC/DB). Optical spectra was measured using a Yokogawa AQ6370D. Electrical contact on the micro-ring lasers was performed with a 3 contact DC probe where each contact represent current injection, ground, and voltage for phase tuning.

**Fig. 1** Diagram of measurement setup.

2.2 Fabrication

In-house device fabrications starts with a 100 mm SOI wafer that consists of a 350 nm thick top silicon layer and a 2 μ m buried oxide (BOX) layer. The top silicon was thinned down to 300 nm by thermal oxidation and buffered hydrofluoric (HF) acid etching, thus leaving a clean silicon surface. Silicon waveguides were defined by a deep-UV (248 nm) lithography stepper and boron was implanted to create p ++ silicon contacts as shown in Figure 2. Grating couplers, silicon rib waveguides, and vertical

out-gassing channels (VOCs) were respectively patterned using the same deep-UV stepper and then subsequently etched 170 nm with Cl_2 -based gas chemistry. Next, the silicon wafer moved through a Piranha clean followed by buffered hydrofluoric (HF) acid etching to remove any hard masks. Next, an oxygen plasma clean was performed followed by a SC1 and SC2 clean. The III-V wafer is cleansed with acetone, methanol, and IPA, followed by oxygen plasma cleaning and a $\text{NH}_4\text{OH}:\text{H}_2\text{O}$ (1:10) dip for 1 min. Next a dielectric of Al_2O_3 was deposited onto both III-V and Si wafer via atomic layer deposition (ALD) with a target thickness of 5 nm on each side. ALD deposition temperature happens at 300 °C. The two samples were then mated manually at room temperature and then wafer-bonded under pressure for 300 °C (2 hour ramp) for a total of 15 hours. After wafer-bonding, the backside of the III-V was mechanically lapped until $\sim 100\mu\text{m}$ of III-V was left. Next, a wet etch was used to remove the remaining InP substrate which stops on the p-contact InGaAs layer.

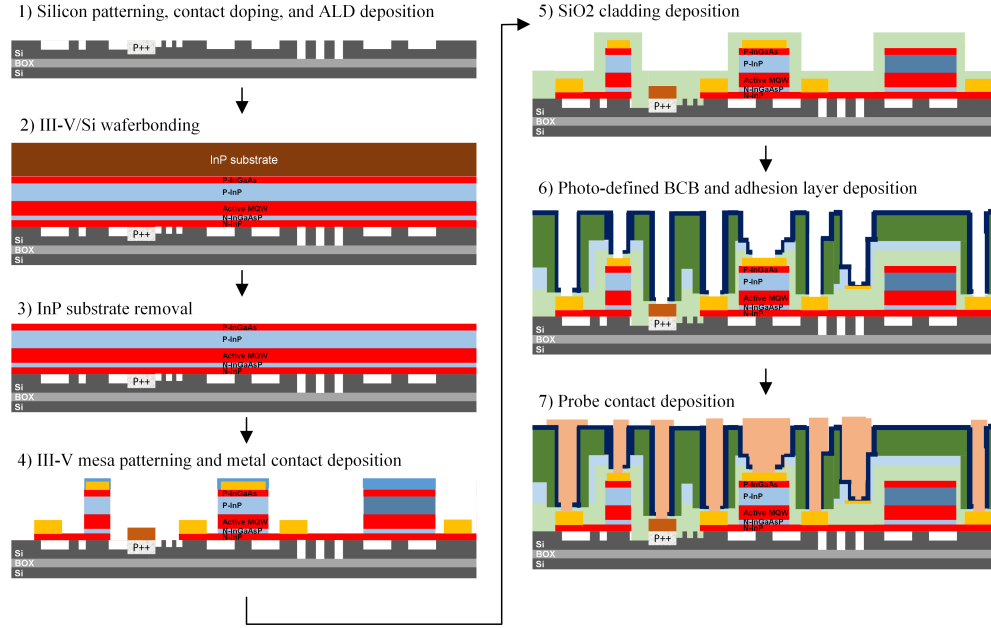


Fig. 2 Fabrication flow of heterogeneous III-V/Si MRL devices.

III-V mesas are defined by etching in an Oxford inductively-coupled plasma (ICP) etcher using a Cl_2 -based gas chemistry stopping right above the active QW regions. The active regions are further defined by an additional lithography step and subsequently wet etched leaving a clean n-contact region consisting of n-InP. A combination of Ge/Au/Ni/Au/Pd/Ti (400/400/240/4000/200/200 Å) was deposited onto the n-InP as an n-contact layer. Metal contact with the p-Si consisted of Ni/Ge/Au/Ni/Au/Ti (50/300/300/200/5000/200 Å). Next, a plasma enhanced chemical vapor deposition (PECVD) SiO_2 was deposited for cladding material. This followed up with etched vias. Next, a thick photo-definable BCB layer was used to minimize electrical parasitics. Finally, Ti/Au metal probe pads were defined for final electrical contacts.

Figure 3 shows a top-view image of various fabricated MRL laser arrays and individual lasers.

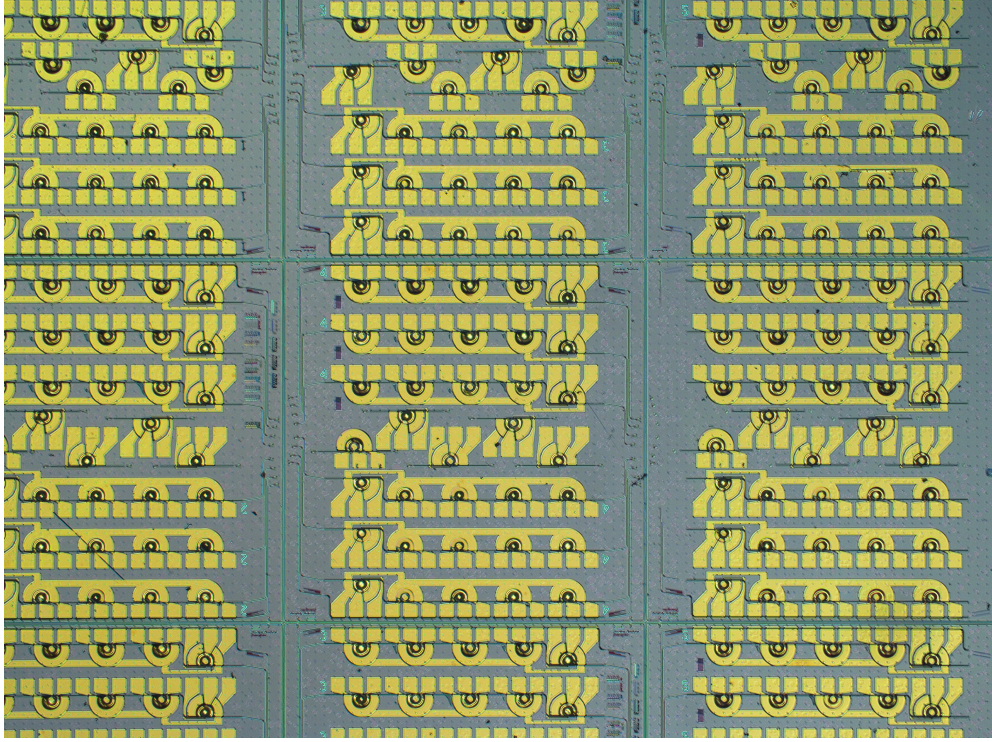


Fig. 3 Top-view of fabricated heterogeneous III-V/Si MRL devices.

3 Improved Charge Trapping Structures

The CTM structure described in this work is based on a single layer of Al_2O_3 where charge trapping can occur either at the semiconductor-dielectric interface or in the bulk dielectric. More complicated structures involving alternating layers of high-k dielectric materials can be used such as n-InP/ Al_2O_3 / HfO_2 / SiO_2 /Si. The Al_2O_3 and SiO_2 serve as the tunneling/blocking oxide while the HfO_2 acts as the charge trap region. For increased trapping density, we can stack multiple layers of CTM structures [4]. The non-volatile operation of these improved CTM structures can be understood by examining the energy-band diagrams of the flat-band and biased regimes as shown in Figure 4 a - b respectively. During the write process, a positive bias is applied to the p-Si region which injects electrons from the highly doped n-GaAs into the lower bandgap HfO_2 layer. The charge traps can exist in the bulk and interface regions, but for simplicity, we model the bulk trap case. After turning the write voltage off, the trapped charges will attract free-carriers at the p-Si/ SiO_2 interface. As a result, this has the effect of causing a negative refractive index change via the plasma dispersion effect. During the erase process, a reverse bias is applied to sweep out the trapped electrons, thus returning the optical CTM cell back to the initial electrical and optical state. The applied bias V_g on the p-Si region can be described by:

$$V_g = \phi_s^{n\text{-InP}} + E_1 d_1 + \int_0^{d_2} E_2(x) dx + E_3 d_3 \quad (1)$$

where $\phi_s^{n\text{-InP}}$ and $\phi_s^{p\text{-Si}}$ is the amount of band bending on the n-InP and p-Si side respectively. E_1 , E_2 , and E_3 , represent the fields in electric fields in the Al_2O_3 , HfO_2 and SiO_2 regions respectively. The electric field in the HfO_2 region is described by:

$$\frac{dE_2}{dx} = -\frac{\rho_2(x, t)}{\epsilon_2} \quad (2)$$

where ϵ and ρ represent the dielectric constant and total trapped charge density respectively in the HfO_2 charge trap region. Once the charges have been trapped, the charge density change for the electrons ΔN_e and holes ΔN_h at the semiconductor interfaces can be described as:

$$\Delta N_e = \Delta N_h = \frac{\epsilon_0 \epsilon_{eff}}{qt_{eff}} \left[V_g - \left(\phi_s^{n-InP} - \phi_s^{p-Si} - \frac{\int_0^{d_2} E_2(x) dx}{C_{total}} \right) \right] \quad (3)$$

where ϵ_0 is the vacuum permittivity, q is the elementary charge, ϵ_{eff} is the effective dielectric constant, t_{eff} is the effective thickness of the capacitance, and C_{total} is the total capacitance. The refractive index change due to charge density change can then be calculated as:

$$\Delta n(x, y) @ 1310 \text{ nm} = -6.2 \times 10^{-22} \Delta N_e(x, y) - 6.0 \times 10^{-18} \Delta N_e(x, y)^{0.8} \quad (4)$$

A 2-D numerical solver (SILVACO ATLAS) was employed to conduct energy-band diagram and charge concentration calculations. This is then used to calculate changes in the optical effective index due to the presence of charge trap densities. The solver numerically calculates the Poisson and charge continuity equations, accounting for defect traps and self-consistently incorporates quantum mechanical tunneling effects. The primary mechanisms contributing to carrier injection include Fowler-Nordheim tunneling, direct tunneling, and hot carrier injection. Evidence of non-volatile behavior can be observed in the hysteresis of capacitance-voltage (C-V) curves as shown in Figure 4 c. Here, the C-V curve is simulated for varying values of trapped charge density Q_{TC} ranging from 0 to $1 \times 10^{20} \text{ cm}^{-3}$. These values are in line with what has been reported in literature [5–7].

The write state is represented by the blue line which requires charging of the trap states from $0 \rightarrow 5 \text{ V}$. The other colors represent a combination of retention ($5 \rightarrow 0 \text{ V}$), erase ($0 \rightarrow -5 \text{ V}$), and return ($-5 \rightarrow 0 \text{ V}$). As an example, if we assume there exists a trap density of $Q_{TC} = 3 \times 10^{19} \text{ cm}^{-3}$, we would apply $0 \rightarrow 5 \text{ V}$ to initiate the write operation as indicated by the blue curve. After, this we would turn off the voltage ($5 \rightarrow 0 \text{ V}$) as indicated by the green curve and observe the retention state. The erase state happens by applying $0 \rightarrow -5 \text{ V}$ indicated by the green curve again and then finally the return state $-5 \rightarrow 0 \text{ V}$. The hysteresis curve defined by the blue and green curve indicate electrical non-volatility due to a charge trap density of $Q_{TC} = 3 \times 10^{19} \text{ cm}^{-3}$. Larger charge trap densities result in a wider opening of the hysteresis curve. The energy-band diagrams for a charge trap density of $Q_{TC} = 3 \times 10^{19} \text{ cm}^{-3}$ are calculated for all 5 states: initial, write, retention, erase, and return as shown in Figure 4 e. The electron and hole concentrations during the retention state is calculated for various Q_{TC} as shown in Figure 4 d. It can be observed that larger values of Q_{TC} result in larger concentration differences at the Si/dielectric interface. These electron and hole concentration values can be utilized to determine a spatial change in the index, as described by Equation 4, where x and y represent the two-dimensional lateral and vertical dimensions. The resulting spatial indices are subsequently applied to an optical finite-difference eigenmode (FDE) solver to calculate the non-volatile effective index changes, $\Delta n_{eff, non-volatile}$, as a function of Q_{TC} , as illustrated in Figure 4 f. We can see that large values of charge trap density can result in effective index changes on

the order of 10^{-3} which can significantly affect the extinction ratio of resonant devices such as MRL lasers. An index change of 1×10^{-3} translates to a wavelength blue-shift of ~ 402 pm, significantly larger than the case of a single Al_2O_3 layer (80 pm).

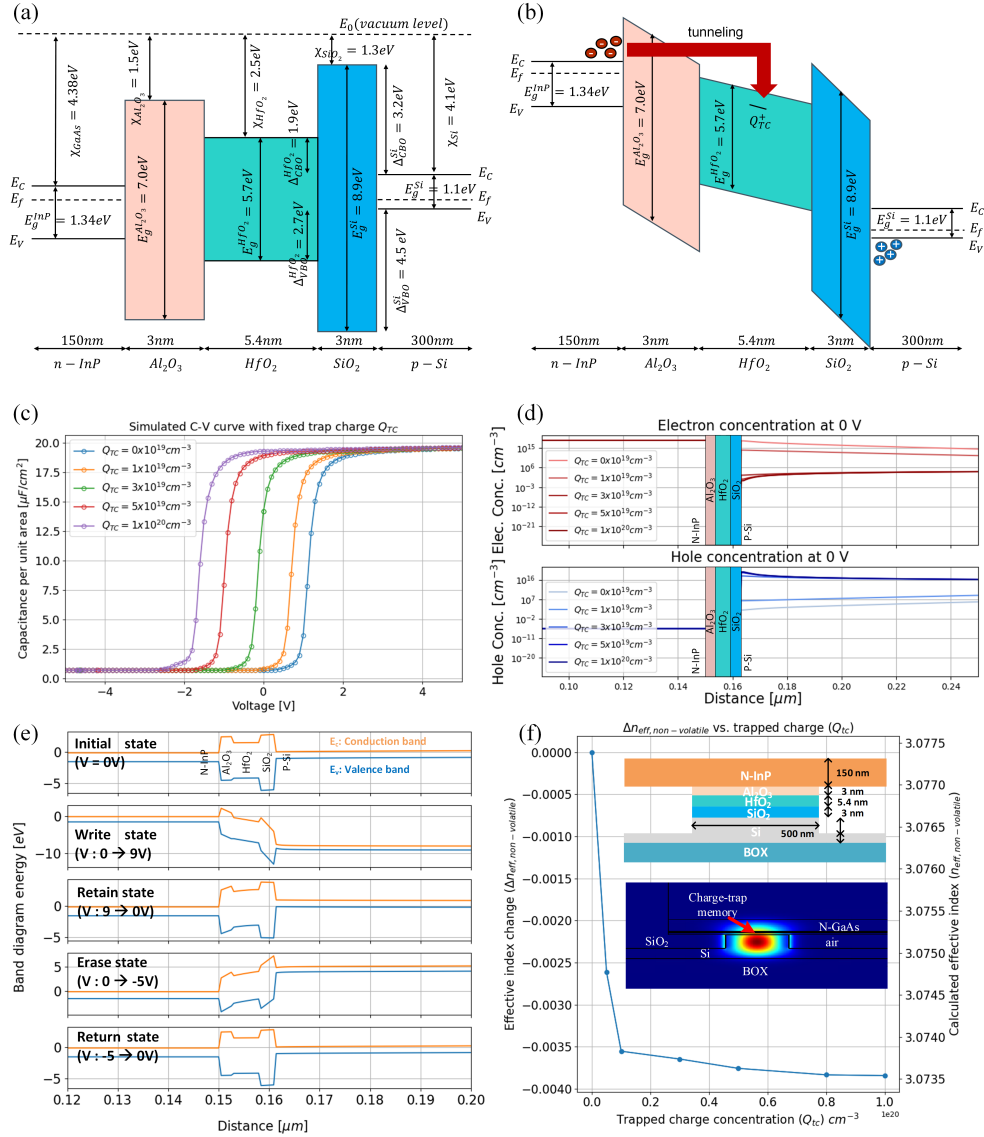


Fig. 4 Schematic of energy-band diagram for n-InP/Al₂O₃/HfO₂/SiO₂/p-Si CTM: **a**, at flat-band condition and **b**, with positive bias on the p-Si side. Simulations for: **c**, C-V curves for various charge densities Q_{TC} **d**, electron and hole concentration profiles at 0 V while in a retention state ($5 \rightarrow 0$ V) **e**, energy-band diagrams of all 5 states: initial, write, retention, erase, and return for a charge trap density of $Q_{TC} = 3 \times 10^{19} \text{ cm}^{-3}$ **f**, non-volatile optical effective index change vs. Q_{TC} .

References

- [1] Sze, S.: Physics of Semiconductor Devices, 4th edn. Wiley, ??? (2021)
- [2] InP - Indium Phosphide. <https://www.ioffe.ru/SVA/NSM/Semicond/InP/>

- [3] Oanh Vu, T.K., Tran, M.T., Tu, N.X., Thanh Bao, N.T., Kim, E.K.: Electronic transport mechanism and defect states for p-inp/i-ingaas/n-inp photodiodes. *Journal of Materials Research and Technology* **19**, 2742–2749 (2022) <https://doi.org/10.1016/j.jmrt.2022.06.028>
- [4] Cheung, S., Liang, D., Yuan, Y., Peng, Y., Tossoun, B., Hu, Y., Xiao, X., Sorin, W.V., Kurczveil, G., Beausoleil, R.G.: Ultra-power-efficient, electrically programmable, multi-state photonic flash memory on a heterogeneous iii-v/si platform. *Laser & Photonics Reviews*, 2400001 (2024) <https://doi.org/10.1002/lpor.202400001>
- [5] Olivares, I., Parra, J., Sanchis, P.: Non-volatile photonic memory based on a sahas configuration. *IEEE Photonics Journal* **13**(2), 1–8 (2021) <https://doi.org/10.1109/JPHOT.2021.3060144>
- [6] Spassov, D., Paskaleva, A., Guziewicz, E., Wozniak, W., Stanchev, T., Ivanov, T., Wojewoda-Budka, J., Janusz-Skuza, M.: Charge storage and reliability characteristics of nonvolatile memory capacitors with hfo₂/al₂o₃-based charge trapping layers. *Materials* **15**(18) (2022) <https://doi.org/10.3390/ma15186285>
- [7] Xiong, H.D., Heh, D., Gurfinkel, M., Li, Q., Shapira, Y., Richter, C., Bersuker, G., Choi, R., Suehle, J.S.: Characterization of electrically active defects in high-k gate dielectrics by using low frequency noise and charge pumping measurements. *Microelectronic Engineering* **84**(9), 2230–2234 (2007) <https://doi.org/10.1016/j.mee.2007.04.094> . INFOS 2007