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Gate structuring on bilayer transition metal dichalcogenides enables ultrahigh current density

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Abstract

The foundry industry and academia dedicated to advancing logic transistors are encountering significant challenges in extending Moore's Law. In the industry, silicon (Si)-based transistors are currently adopting gate-all-around (GAA) structures and reducing channel thickness, even at the cost of decreased mobility, for maximizing gate controllability. To compensate for the reduced mobility, multi-channel structures are essential, making the fabrication process extremely challenging. Meanwhile, two-dimensional (2D) semiconductors are emerging as strong alternatives for the channel material in logic transistors, thanks to their ability to maintain crystallinity even when extremely thin. In the case of 2D semiconductors, introducing a dual gate structure, which has a much lower fabrication complexity, can achieve effects similar to GAA. Through this research, we have identified the fringing field originating from the common structure of elevated top contact in 2D FETs results in a high charge injection barrier. Through simulation and statistical analysis with large-area FET arrays, we confirmed that introducing a dual-gate structure in bilayer MoS_2 FETs effectively compensates for the fringing field. We have confirmed that this leads to a significant boost in on-current. Remarkably, even with conventional contacts and polycrystalline materials, we observed a record-high on-current of 1.55 mA/μm. Additional circuit simulations have confirmed the potential for dual gate bilayer FETs to surpass the performance of Si GAAFETs when possessing a gate length of 5 nm, achievable only with 2D materials. Therefore, here we propose that by using 2D materials, we can focus on extreme gate length scaling and monolithic 3D integration rather than the challenging GAA process for extending Moore’s Law.

Main text

As silicon (Si) transistors approach their atomic limits for gate length scaling, foundry companies and related academic society are focusing on enhancing the electrostatic control capability of the channel. The strategy now being adopted is structurally positioning the gate to have more contact with a larger portion of the channel.[1,2] This progress has occurred incrementally, evolving from the one-sided planar field-effect transistor (FET) to the three-sided Fin-FET, and ultimately to the four-sided gate-all-around (GAA) FET. Simultaneously, there has been a trend towards minimizing the thickness of the channel to gain additional electrostatic controllability. However, it is widely recognized that structural modifications alone will not be sufficient to sustain Moore's law, as the carrier mobility of silicon is expected to decline significantly below a thickness of 5 nm, resulting in a substantial decrease in current.[3] Therefore, to compensate this current reduction, it is essential to adopt a multi-channel configuration.[4] However, fabricating contacts and gates for such a structure requires introducing new processes not used in existing technology, which is very challenging, costly, and yields low. Moreover, future advanced technology nodes below the 1 nm scale lack viable solutions to sustain Moore's Law.[5] Consequently, a “monolayer” crystal semiconductor, so called two-dimensional (2D) transition metal dichalcogenide (TMD), has emerged as a compelling alternative for channel materials because its broken bonds-free surface nature offers a means to mitigate the pronounced short-channel effects observed in silicon.[3,6] 2D TMDs exhibit high gate controllability as their major advantage, with no mobility drop even at channel

thicknesses below 1 nm, theoretically enabling operation at gate lengths of 5 nm or less. Also, since single crystal growth of 2D TMDs on amorphous substrates is possible, sequential fabrication of dual gate structures can be easily implemented.[7] Similarly, due to the thin thickness, the dual gate structure can achieve effects similar to GAA structures. Nevertheless, until now, predictions that the thin nature of 2D materials would allow sufficient electrostatic control with single gate structures and the challenges of depositing high-quality top gates on 2D materials have hindered dual gate research.[8] As a result, TMD-based single gate transistors have not demonstrated significantly improved on-current (I_{on}) performance compared to Si counterparts. So far, substantially high contact resistance between TMDs and metals has been regarded as the primary hurdle for achieving higher I_{on}. In reality, a substantial improvement in I_{on} has been observed by simply identifying appropriate contact metals.[9,10] Consequently, the research community's focus has been centered around an interface engineering between metals and TMDs.

Meanwhile, in this study, we reveal how significantly the introduction of dual gate structures can improve transistor performance with both simulations and experiments. Our circuit simulations demonstrate that with extreme gate length scaling in dual gate structures, performance comparable to Si 3 nm node technology fabricated using GAA processes can be achieved. By adopting planar dual gate FETs instead of the highly complex GAAFETs, similar performance can be achieved. This allows for monolithic 3D integration on arbitrary substrates at low temperatures, creating area gains and paving the way to sustain Moore's Law even at advanced nodes below 1 nm.[11] First, we discovered through simulations an important factor that has been overlooked in 2D TMD-based transistors: the potential barrier caused by the fringing field from the elevated top contact electrodes. We confirmed that the influence of the fringing field is greater in bilayers than in monolayers and that applying a dual gate can partially offset this potential barrier. As a result, introducing a dual gate for bilayer TMDs is expected to increase the current by approximately five times compared to single gate structures. To verify this sudden boost in I_{on} through statistical experiments, we fabricated FET arrays on a 200-mm wafer-scale monolayer and bilayer MoS_2 films and observed the improvement in electrical performance for dual gate structures compared to single gate structures. Experimentally, it was confirmed that the I_{on} of dual gate structures increased by approximately three times compared to single gate structures. Through the extraction of contact resistance (R_C) using the statistical transfer length method (TLM), we confirmed that the reduction of the barrier near the contact electrode due to the introduction of dual gates is particularly pronounced in bilayer MoS_2, aligning perfectly with our simulation results. Remarkably, utilizing polycrystalline MoS_2 and conventional Au contact electrodes, we achieved an astonishing I_{on} of 1.55 mA/μm due to the I_{on} boosting effect from the bilayer, dual-gate configuration. Furthermore, our FET utilizes high-k dielectrics on both top and bottom, effectively lowering the operating voltage compared to conventional TMD-based devices using global back gates, bringing it closer to the industrial Si transistors. Based on this, we conducted additional technology computer-aided design (TCAD) and simulation program with integrated circuit emphasis (SPICE) simulations and confirmed that bilayer MoS_2 dual gate transistors can achieve comparable I_{on} compared to Si transistors at the 3 nm node, especially for gate lengths below 10 nm. We also confirmed the potential for our current device to

operate normally without significant performance degradation compared to a planar Si circuit at the 45 nm node, which has the most similar geometry with our FET.

As gate lengths for 2D TMD-based FETs further decrease, the contacted poly pitch (CPP) also decreases, potentially leading to area gain. This aspect could offer advantages over Si GAAFETs in terms of performance, power, and area (PPA). One of the greatest advantages of 2D materials is not only their extremely thin thickness but also the ability to grow single crystals on amorphous substrates, enabling their use in monolithic 3D integration. Therefore, we have demonstrated for the first time in this study that creating complementary FETs (CFETs) based on dual gate structures, rather than GAAFET processes which have higher fabrication complexities, and integrating these layers in a stacked configuration, may offer advantages when considering costs and performance.[7,11]

On-current and electrical potential in single gate and dual gate MoS 2 FETs as predicted by TCAD simulations

Unlike Si transistors, 2D TMDs lack heavy doping technology so far, necessitating direct metal contact to the undoped channel area. This contact takes the form of an elevated top metal electrode. In such a case, a relatively large fringing field can be expected between the metal and the channel near the metal. Nevertheless, until now, only considered as parasitic capacitance, no one has taken into account its impact on the current in the channel.[12] On the other hand, the electrical band gap of the most common TMD, monolayer MoS_2, is relatively large, which is advantageous for leakage suppression.[13,14] However, it poses challenges in obtaining sufficient carrier mobility, and direct metal contact induces a large Schottky barrier height, leading to significant contact resistance. It is because the smaller band gap of the bilayer induces a lower Schottky barrier height, resulting in superior contact characteristics compared to monolayers.[15] Hence, bilayer MoS_2 could offer more physical space to transport charge carriers in response to the gate bias, resulting in the higher carrier mobility.[16] Therefore, to enhance the performance of the FET further, we opted for a straightforward combination of bilayer MoS_2 and a dual-gate configuration.[17–19] In this study, we systematically analyzed the impact of the fringing field, a factor that has always been present in 2D FETs but has been overlooked so far.

Due to the characteristics of freestanding 2D materials, creating a back gate structure is relatively straightforward. Then, by creating a top gate, a typical MoS_2 dual gate FET is easily fabricated, as shown in the structure depicted in Fig. 1a. For high performance, it is essential that the equivalent oxide thickness (EOT) of the top and bottom dielectrics are balanced. However, forming a high-quality top gate dielectric layer on a 2D material is challenging due to the noble surface, as widely acknowledged.[20] We utilized a low-temperature ALD interlayer deposition method known as the 'nanofog' technique to deposit the high quality top gate dielectric.[8] Furthermore, to align our simulations with our experimental results, we avoided using materials that might react with the 2D material or generate a native oxide layer easily. Therefore, we employed gold (Au) for both the source-drain and gate electrodes. Representative dual

gate device's top view scanning electron microscopy (SEM) image and cross-section transmission electron microscopy (TEM) image are shown in Fig. 1b and 1c, respectively.

Based on the real device geometry, we conducted accurate TCAD simulation modeling as shown in Fig. 1d. In previous TCAD simulations based on 2D materials, the actual shape of the electrodes was not considered accurately.[21–23] Also, they were limited by using silicon-based tools to simulate 2D materials, which only considered changes in thickness and basic properties, leading to significant inaccuracies when compared to the experimental results. To confirm the characteristics of bilayer MoS_2 through simulation, we included the van der Waals gap between the upper and lower MoS_2 layers, which is the most significant difference from Si. Then we designed the simulation to match the known properties of bilayer MoS_2, including band gap and dielectric constant. Based on this modeling, we conducted TCAD simulations for both monolayer and bilayer MoS_2 for both single gate and dual gate FET configurations. Initially, we defined the on-state for all cases with a gate-source voltage (V_{gs}) of 3 V and a drain-source voltage (V_{ds}) of 1 V. Subsequently, we extracted the corresponding currents for each case as shown in Fig. 1e. For the monolayer, the introduction of the dual gate led to a doubling of the gate capacitance. Consequently, the electron density within the channel increased by approximately two-fold, being expected to result in an increase in current of about 2 times. However, in the case of the bilayer, the dual-gate FET exhibited a substantial increase in current, approximately five times higher compared to the single-gate configuration. This is highlighted in Fig. 1e, where the additional increase in current, denoted by the 'question mark', indicates a notable contribution beyond the carrier density increase upon the application of dual gates in bilayer MoS_2. As evident from the calculated transfer curves ($I_{ds} - V_{gs}$) in Extended Data Fig. 1, there is no apparent impact due to the negative shift in the threshold voltage. Instead, the suppression of the short-channel effect in the dual-gate configuration leads to an improvement in subthreshold characteristics. In Fig. 1f and 1g, we illustrated the simulation results of the electrostatic potential within monolayer and bilayer MoS_2 FETs at on-state, respectively. In the enlarged view of the MoS_2 layer vicinity, as depicted in Supplementary Information Fig. S1, differences in modeling between monolayer and bilayer can be observed. In both cases, we observe a significant potential drop around the source electrode in the single gate configuration, and this effect is mitigated when the dual gate is applied. The line profiles of the energy of conduction band edge in the x-direction for monolayer and bilayer MoS_2, along with the corresponding electron density, are plotted in Fig. 1h and 1i, respectively. For bilayer MoS_2, considering that the top layer in direct contact with the top metal contact serves as the main conduction layer, we computed the line profile specifically for this layer. (For potential profile of the bottom layer, see Fig. S2) Under all conditions, pronounced energy barriers are observed around the source electrode, leading to a notable reduction in charge density in this region. This barrier is directly attributed to the fringing field from the elevated contact. We demonstrated the creation of a low fringing field structure, suppressing the fringing field and consequently lowering the barrier. Therefore, as shown in Fig. S3, under the low fringing field conditions for bilayer MoS_2 FETs, a higher on-current can be obtained. Here, a significant distinction between monolayer and bilayer is apparent. In the case of the monolayer, there is minimal change in the barrier height even after the

introduction of dual gates. However, for the bilayer, the dual-gate introduction noticeably compensates for this fringing field. The reason why the fringing field is more effectively compensated in the bilayer MoS_2 with dual gate compared to monolayer can be explained as follows: In monolayer MoS_2, it is already significantly influenced by the back gate, whereas the main conduction layer in bilayer is the top layer, so lower layer screens out some of the effects of the back gate. At the same time, the top layer is more directly affected by the fringing field from the top contact. As a result, bilayer MoS_2 FET is expected to exhibit more than a 2-fold increase in additional I_{on} due to the compensation of the fringing field with the introduction of the dual gate. We further theoretically verified it from the capacitance model described in Fig. S4. As well as on-state characteristics, the introduction of dual gates also significantly improved subthreshold characteristics such as subthreshold swing (SS) and leakage current. (Extended Data Fig. 1)

200-mm wafer scale growth of monolayer and bilayer MoS

Our primary focus has been on achieving the uniform growth of bilayer TMDs across 200-mm wafers, a task not previously demonstrated due to the challenges associated with layer-by-layer growth directly on Si wafers.[24,25] Here, we introduced an additive during growth to enhance adatom diffusion. As a result, we could successfully regulate nucleation and promote lateral growth, achieving uniform growth even with bilayer thickness. As a result of these efforts, we have successfully achieved bilayer-dominated MoS_2 growth across 200-mm wafers. This accomplishment has enabled us to establish wafer-scale arrays of bilayer transistors with dual gating capabilities.

While the growth of uniform monolayer films has been relatively well-established in previous research, there have been only very limited reports on the growth of uniform bilayer films.[24] Therefore, our focus was on adjusting the average thickness to match bilayer thickness for statistical analysis. To achieve uniform bilayer growth, it is necessary to suppress the nucleation of adlayers until the next layer growth is completed. We were able to obtain relatively uniform monolayer and bilayer films in 200-mm wafer scale through the utilization of the metal-organic chemical vapor deposition (MOCVD) method and use of proper growth additives. (See Methods for details) Fig. 2a and 2b respectively display cross-sectional TEM images of the grown monolayer and bilayer. In Fig. 2c, characteristic Raman peaks of monolayer and bilayer MoS_2, including E^1_{2g} and A_{1g} peaks, along with the Si substrate peak near 520 cm^{-1}, are presented. The intensity of the A peak relative to the Si peak is significantly higher in the bilayer than in the monolayer. Moreover, the distance between the E-A peaks directly related to the layer number is precisely in line with the values reported in the literature, measuring 19.8 cm^{-1} for the monolayer and 21.9 cm^{-1} for the bilayer.[26] Of course, it would be challenging to claim that the entire film is strictly monolayer or bilayer, due to the presence of adlayer patches. However, through statistical Raman analysis, we can track the average number of layers. In Fig. 2d, the distribution of the analyzed E-A peak distances from 100 Raman spectra within a 10 cm by 10 cm area of as-grown MoS_2 films is plotted. Also, as evident from the Raman mapping in Extended Data Fig. 2, it can be confirmed that a generally

uniform monolayer and bilayer were fabricated. Therefore, we can statistically consider the two MoS_2 films as predominantly monolayer and bilayer, respectively.

Statistical assessment of monolayer and bilayer MoS FETs with single and dual gate configurations

Based on the growth of wafer-scale monolayer and bilayer films, we succeeded fabricating FET arrays on 200-mm wafers. (Inset of Fig. 3a) The detailed fabrication process is described in Fig. S5 and the Methods section. (For cross-section TEM images of the devices see Fig. S6) To ensure accurate analysis on difference between single gate and dual gate configurations, we measured the same device both before and after the formation of the top gate electrode. In this study, the analysis of the top gate-only configuration is not of significant relevance since the field from the top gate has a limited impact on lowering the contact barrier, while back gate electrostatically dopes contact region at the on-state. This can be observed from the statistical analysis of long-channel devices (L_{ch} > 500 nm) fabricated by only photolithography shown in Extended Data Fig. 3. The measurements of the top-gate-only configuration reveal that it exhibits performance that is more than an order of magnitude lower than that of the back gate, due to the lower quality of top-gate dielectric compared with pre-deposited back-gate dielectric as well as lack of contact gating.

Meanwhile, the transfer curves ($\sigma_{SH} - V_{gs}$) of hundreds of monolayer and bilayer MoS_2 FETs are plotted in Fig. 3a and 3b, respectively. The channel length (L_{ch}) here was varied from 30 nm to 300 nm. In order to normalize the current with channel length and width of the various FETs, the y-axis was represented in sheet conductance (σ_{SH}). The results indicate that both SS and I_{on} are superior in the dual gate configuration compared to the single gate. Also, based on this, the change in I_{on} with respect to L_{ch} was plotted for monolayer and bilayer as shown in Fig. 3c and 3d, respectively. A huge increase in I_{on} of dual-gate FET compared to single-gate FET was observed in all L_{ch} ranges for dual gate FET. It is quite remarkable that the MoS_2 film, despite being polycrystalline, exhibits an average I_{on} of around 700 μA/μm at L_{ch} of 30 nm, simply with the combination of bilayer and dual gates. Interestingly, in bilayers, the increase in I_{on} with dual gate compared to single gate is consistent regardless of L_{ch}, whereas in monolayers, the increase becomes more pronounced as L_{ch} increases. In previous simulation results, the difference of potential barrier height between single and dual gate in monolayers is not significant. Consequently, in the contact-dominant regime of short channels, the difference is around two-fold. However, in long channels, which enter the channel-dominant regime, changes in the channel that were not apparent in simulations seem to be observed. To investigate this further, we conducted TLM analysis for each case using the transfer curves for each L_{ch}, as illustrated in Extended Data Fig. 4. Here, V_{gs} in each transfer curve was converted to overdrive voltage (V_{od}), which was further transformed into carrier density using the capacitance values extracted in the various metal-insulator-metal (MIM) structures, as shown in Fig. S7. As a result, it is able to plot R_C as a function of planar carrier density (n_{2D}), as shown in Fig. 3e and 3f for monolayer and bilayer, respectively. In both cases, the dual gate has a roughly two-fold

higher capacitance than the single gate at the same V_{gs}, resulting in a broader range of n_{2D} for the dual gate. Interestingly, as shown in Fig. 3e, the lowest R_C in the monolayer is comparable between the single gate and dual gate, measuring around 4.1 kΩ•μm and 4.6 kΩ•μm, respectively. This aligns precisely with the simulation results in Fig. 1h, where the difference in charge injection barrier due to the fringing field was minimal. On the other hand, examining Fig. 3f, in the bilayer, the R_C shows a value of 4.3 kΩ•μm under the single gate, which is not significantly different from the monolayer. However, with the introduction of the dual gate, it drastically improves to 1.3 kΩ•μm, aligning precisely with the reduced charge injection barrier observed in the simulation in Fig. 1j. As summarized in Fig. 3g, the I_{on} of dual gate monolayer MoS_2 FET showed an average increase of 2 times compared to a single gate, while in bilayer MoS_2 FET, it shows an increase of around 3.6 times. Surprisingly, this also matches exactly with the predictions made in Fig. 1e. Now, we can attribute the additional increase in the bilayer to the compensation of the fringing field coming from the top gate. In Fig. 3h, we plotted the proportion of R_C and channel resistance (R_{ch}) in the total resistance based on the R_C and sheet resistance (R_{sh}) extracted from TLM in Extended Data Fig. 4. In the shortest FETs with L_{ch} of 30 nm, the current proportion of R_C is significant, and the twofold decrease in resistance in monolayers can be attributed to a rapid decrease in R_{sh} while R_C remains relatively constant. This holds true for bilayers as well, where not only R_C but also the sharp decrease in R_{sh} results in a substantial reduction in overall resistance. The crucial message here is that even with the thin thickness of monolayers, it is challenging to achieve full accumulation throughout the entire channel with only one-sided gating. The use of dual gates is essential to fully utilize the entire channel. Therefore, it implies that the carrier mobility of the channel can vary depending on the gate, even for the same material. This can be observed in Fig. S8, which compares the TLM mobility, excluding contact effect, extracted using the TLM method. Therefore, we have validated the fact that, even with an extremely thin channel material, leveraging the dual gate structure is advantageous.

Benchmarking Ion of dual gate bilayer MoS2 FET

To assess the maximum current level that MoS_2 can handle, we selected the best device of bilayer MoS_2 with dual gate configuration from the previously measured FETs and increased the V_{gs} range up to + 4 V. Transfer curves ($I_{ds} - V_{gs}$) of the best device plotted in semi-log and linear scale are plotted in Fig. 4a. The linear shape in the output curves ($I_{ds} - V_{ds}$) at low V_{ds} regime in Fig. 4b demonstrates that the contact is ohmic, contributing to the record-high I_{on} of 1.55 mA/μm. We benchmarked the obtained I_{on} as a function of V_{ds} from the device in Fig. 4c among n-type 2D FETs. Even with a simple structural change, we achieved higher I_{on} compared to single crystal-based FETs. Of course, while direct comparisons with commercially available silicon-based components are not reasonable, our FET outperforms the I_{on} requirements suggested by IEEE International Roadmap for Devices and Systems (IRDS) 2022 roadmap,[5] being leveraged from the maximum potential of bilayer MoS_2 by introducing dual gate. It is significant that these results were obtained at the lower source-drain bias (V_{ds}) and V_{od} among the high on-current 2D semiconductor-based FETs.[9,10,24,27–31] (Fig. 4c and 4d)

Many studies have shown that low V_{ds} results in high on-current, suggesting the potential to outperform silicon. However, these figures mostly come from fundamental research using global back gates, and thus are measured at high V_{od}, as shown in Fig. 4d. Except for a recent study, our work shows high I_{on} at an operation voltage most similar to silicon, using local gates. This allows for a more accurate comparison with silicon. To address this, we comparatively examined the performance with a 45 nm node Si transistor that has a relatively similar gate length with our FET. The 45 nm node transistor typically has a gate length ranging from approximately 30 nm to 40 nm and uses a V_{dd} of 1 V,[32,33] which are similar to our device. These factors also explain why only a few 2D FET based AC circuits have been reported so far.[22,34,35] To enable a relatively fair comparison under similar conditions, we scaled V_{gs} by our device's EOT to 1 nm from 3.3 nm and applied an arbitrary shift to align the V_{th} of the two devices as shown in Fig. S9. Here, with an I_{off} of 100 nA/μm and V_{dd} of 1 V, the I_{on} is 690 μA/μm, which is about half the level of the Si 45 nm node FET.[32,33] Considering the difference in mobility between bulk Si and our MoS_2, the results can be regarded as quite comparable. We can calibrate the TCAD model of Fig. 4e with our experimentally based I-V curve, as shown in Fig. 4f. Conversely, we can use the TCAD model to simulate I_{on} by reducing the gate length. As shown in Fig. 4d, to compare with the Si 3 nm node, reducing V_{dd} to 0.7 V and the gate length to 12 nm—the limit for Si gate length—results in an I_{on} increase to 1.27 mA/μm. Further reducing the gate length to 5 nm, the limit for bilayer MoS_2, increases Ion to 2.08 mA/μm. The Si transistor in this scenario would likely be in a multi-channel configuration, potentially boosting the on-current further. Nevertheless, due to the large capacitance disadvantage inherent in the GAAFET structure, the AC circuit performance is expected to be comparable to that of planar dual gate MoS_2.

To indirectly demonstrate this, we conducted a simulation comparing the circuit performance of our device with that of a 45 nm node Si planar transistor, which has the most similar geometry to our device. Scaling our device to an advanced node involves making significant assumptions and may introduce inaccuracies, which is why we chose to compare it with the 45 nm node Si planar transistor instead. Nonetheless, the following assumptions are still necessary for comparison between our 2D FET and a 45 nm node Si FET. First, assumptions about the performance of p-type metal-oxide-semiconductors (PMOS) are needed. We simply assumed PMOS by symmetrizing the MoS_2 n-type metal-oxide-semiconductors (NMOS). Given that WSe_2, which is an emerging 2D semiconductor as a PMOS candidate, has higher mobility and I_{on}, we believe this approach is feasible in the future.[3,36] Second, to achieve fair circuit performance, it is assumed that there is no vertical overlap between the source/drain electrodes and the gate electrode. In the actual structure, contact doping is achieved using electrostatic gating of the contacts, while this structure results in excessively high gate capacitance, which leads to significant RC delay in the circuit. Instead, gate-dependent contact resistance was separately incorporated into the model using the experimental values from Fig. 3f. To create a process design kit (PDK), which is crucial for SPICE circuit simulation, compact modeling of the 2D FET is necessary. Among these, the I-V curve can be calibrated using the experimental data from our Fig. S9 to fit the appropriate model. After applying a channel width of 500 nm and using the Verilog-A MIT Virtual Source model (MVS) to calibrate the transfer curves and output curves, we confirmed that the results fit well, as

shown in Fig. 4f.[37,38] However, as previously mentioned, we assumed a structure without overlap between source/drain and gate metal to optimize circuit performance, so we cannot use experimental C-V curve for circuit simulation. Therefore, based on the device structure in Fig. 4e, we extracted the gate capacitance curve (C_{gg} - V_g) through TCAD simulation, and the results are shown in Fig. 4g. These results are very similar to the curve calculated using the MVS model, indicating their excellent reliability. Based on these results, we were able to proceed with compact modeling of our 2D FET and simulate a 5-stage ring oscillator. The frequency is 3.56 GHz and 11.05 GHz, corresponding to a delay per stage of 28.1 and 9.1 ps for V_{dd} of 1 V and 2 V, as shown in Fig. 4h and i, respectively, which is comparable to Si 45 nm node's performance (6 ps).[32] (Fig. S10 and Fig. S11 for gate capacitance and ring oscillator performance of the FETs with overlapped gate, respectively) As we benchmarked our simulated ring oscillator delay in Fig. 4j, there is still a significant difference between the experimentally obtained performance and the calculated performance. This is because the technology based on 2D materials is still underdeveloped, making it challenging to achieve balanced CMOS fabrication, and the lack of doping technology leads to the absence of spacer processes, resulting in high parasitic capacitance that limits circuit performance. From a device perspective, it is also necessary to engineer the interface with the dielectric and reduce contact resistance. This will not only improve performance but also ensure uniformity and reliability. Hence, for now, since the alternative target for 2D semiconductors is Si nanosheets with channel thicknesses of 4 nm or less, directly surpassing bulk Si planar transistors may not be feasible. Nevertheless, our computational objective was to demonstrate that 2D FETs can achieve performance levels similar to silicon as much as possible.

Conclusions

Through this study, we confirmed that the fringing field arising from the elevated contact in 2D FETs forms a significant barrier around the source, hindering the charge injection in 2D semiconductors. In particular, for bilayer MoS_2, the introduction of a dual-gate structure compensates for this fringing field to some extent, leading to a significant boost in current compared to the single gate. This phenomenon was confirmed through simulations to be due to the two layers of bilayer MoS_2 being separated, unlike in Si. The resulting current boost was observed in both simulation and experiment. Furthermore, we demonstrated through TLM methods that the introduction of dual gates not only reduces the charge injection barrier but also increases channel mobility by opening additional electrical paths, even in extremely thin channels. An important point is that, unlike results analyzed from individual unit devices, the reliability of our results is enhanced by statistically comparing hundreds of devices processed through the same 200-mm wafer fabrication process. In essence, by demonstrating the benefits brought about by the introduction of dual gates, we have justified the adoption of GAA structures in 2D FETs, similar to Si. Lastly, our best device, despite utilizing polycrystalline MoS_2, achieved a DC I_{on} record of 1.55 mA/μm. We conducted simulations to evaluate the performance of our FET when applied to actual planar FETs, as our device achieved high I_{on} while operating at industrially viable voltage levels. Using TCAD, we fitted our experimentally obtained transfer curves and calculated the capacitance. Based on this, we performed compact modeling to implement a 5-stage ring oscillator. The delay per stage was

9.1 ps at V_{dd} of 2 V, which is comparable to that of the 45 nm node Si with similar dimensions. Moreover, in gate lengths below a few nanometers, where there is no degradation in mobility in an extremely thin channel, our device is expected to have a clear advantage over Si nanosheet transistors.

Methods

TCAD Simulation

We use the multi-subband Boltzmann transport equation (MSBTE) solver, implemented in our in-house simulator. It calculates the Schrödinger equation perpendicular to the transport direction and one-dimensional MSBTE for each subband. Mode decomposition is used to reduce the computational burden at the realistic device scale, and periodic boundary condition is applied for the width direction. Layer-dependence effective mass and bandgap are considered as in Table 1, and a multi-layer model considering the van der Waals (vdW) gap is used to accurately reflect the electrostatic effects depending on the device structure. DFT results show that the MoS_2 layer has a high dielectric constant, while the vdW layer has a low dielectric constant.[39,40] This causes most of the potential drop to occur in the vdW layer, resulting in a significant difference in the electrical operation of monolayer and multilayer devices. The MSBTE solver is a semi-classical transport equation that cannot originally consider tunneling effects. However, the tunneling current is accurately included as nonlocal intravalley interaction based on the WKB tunneling model.[41] This allows for the accurate consideration of the source-induced injection barrier. In bilayer modeling, another challenge is calculating the current path correctly. In a few-layer top-contact device, the main current path is the top layer, as carriers with small electric field are rarely injected from the source to the bottom layer. However, the MSBTE solver considers the 1D transport equation and imposes the injection boundary condition on the sides, leading to the misleading conclusion that most of the current path is formed in the bottom layer, which is less susceptible to the source fringe field effect. To mimic the low current injection to the bottom layer by tunneling through the vdW layer, a thin tunneling layer is added to the bottom layer as in Fig. S2. Through these detailed modeling efforts, the origin of the substantial gain of I_{on} and decrease of the R_C when using dual-gate in a bilayer device is clearly identified.

MOCVD of monolayer and bilayer MoS_2

The growth of 200 mm scale monolayer MoS_2 was conducted under the same conditions as in our previous studies.[42–44] We used a shower-head-type cold-wall MOCVD reactor for the growth of MoS_2, utilizing $Mo(CO)_6$ as the Mo precursor and $(C_2H_5)_2S_2$ as the S precursor. The flow rates of the precursors were 0.001 sccm for $Mo(CO)_6$, 0.007 sccm for $(C_2H_5)_2S_2$, and 100 sccm for H_2, all of which were precisely regulated by individual mass-flow controllers and electronic pressure controllers. The chamber pressure and wafer temperature were maintained at 5.0 torr and 600 ^oC, respectively, during the growth process. We used KI as an additive to improve adatom diffusion, placing it upstream in the reactor. Growth time was controlled from 12 minutes to 1 hour to control the layer number.

Fabrication of 200-mm wafer scale FETs

First, we started device fabrication with a 200 mm Si wafer and create a 100 nm SiO_2 layer through thermal oxidation. Next, we pattern the bottom gate electrode using photolithography with a stepper. At this stage, the negative process using the image reversal photoresist AZ5214 is utilized, followed by a lift-off process. For the bottom gate metal, 5 nm of Ti and 20 nm of Au are used. The creation of the bottom gate structure is completed by depositing 10 nm of HfO_x using atomic layer deposition (ALD). Next a MoS_2 film grown by MOCVD is transferred onto the substrate. As in our previous study,[43] a semi-automatic transfer stage is utilized at this stage. After that, another photolithography process is carried out to pattern the active channel area of MoS_2. The exposed areas of MoS_2 are etched using O_2 reactive ion etching (RIE) or a plasma asher. Next, we patterned fine source/drain electrodes for the short-channel device using e-beam lithography. In this case, a 495k PMMA A2 / 950k PMMA A2 bilayer is utilized as an e-beam resist for smooth lift-off. In this case, Au 20 nm is used as the contact metal. Another round photolithography, metal deposition, and lift-off are carried out to create metal leads connecting the pads for subsequent measurements. It is important to perform e-beam lithography first in this process, as PR residue can significantly degrade contact resistance of resulting FETs. To facilitate the deposition of dielectric on top of the MoS_2 for the fabrication of the top gate, an interlayer is deposited using a method known as the "nanofog" technique.[8,45] Top gate dielectric, 10 nm HfO_x, is deposited using ALD. Then, similar to the bottom gate process, patterning is carried out to form the top gate dielectric, completing the device fabrication. See Fig. S5 for visualized fabrication processes.

Compact modeling and 5-stage ring oscillator simulation

It is crucial to extract I-V and C-V characteristics of 2D FET for obtaining a PDK, assuming that elements like interconnections are similar to existing Si technology. Firstly, in actual devices, electrostatic doping is necessary due to the lack of doping techniques in the contact region. This results in significant parasitic capacitance from the overlap between the source/drain electrodes and the gate electrode. Therefore, we assumed no gate overlap and separately applied the gate-dependent contact resistance to the I-V calibration. Then, we were able to obtain the C-V curve for the assumed structure without overlap using TCAD. The experimentally obtained I-V curve was also utilized with the Verilog-A MVS model. Based on the completed PDK for the 2D FET, we conducted a SPICE simulation of a 5-stage ring oscillator. The load capacitance per stage used in this simulation was 1.2 fF, identical to the value used in previously reported ring oscillators based on 45 nm node Si transistors.[46,47]

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Figures

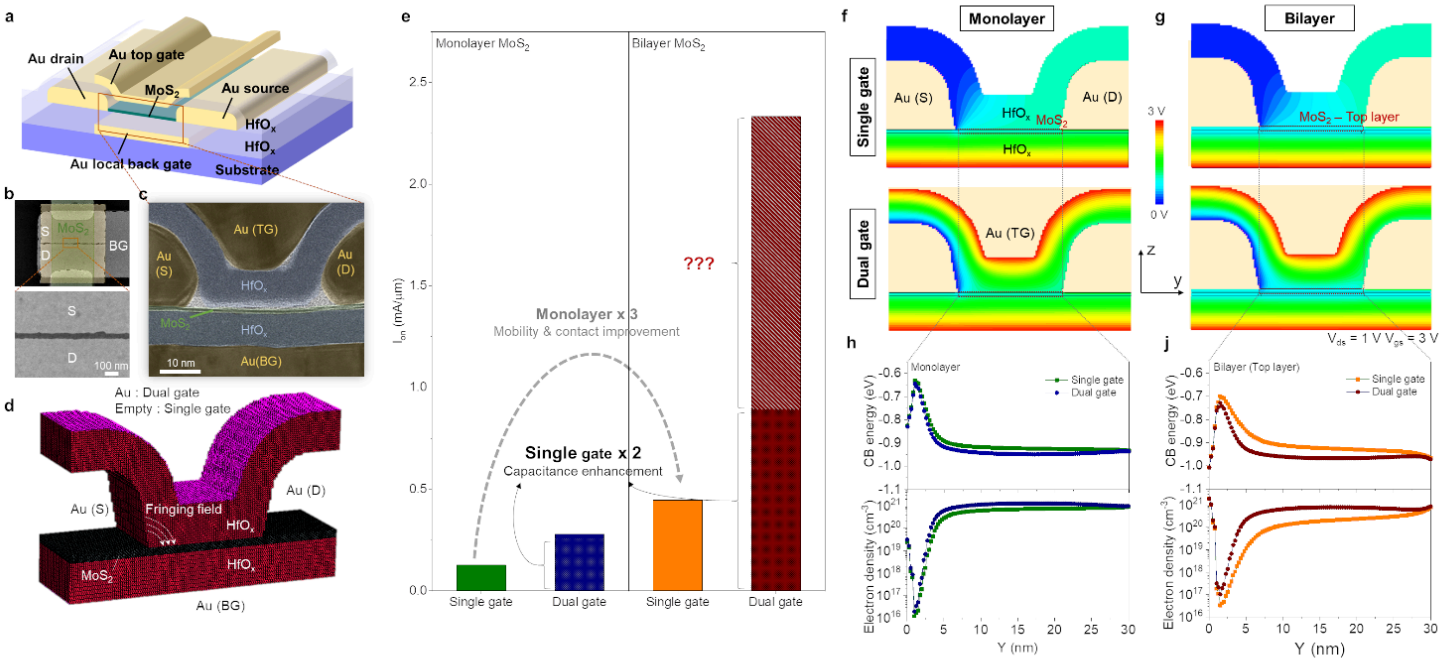


Figure 1

TCAD simulation results based on the actual MoS_2 dual-gate FET

a. Schematic illustrating MoS_2 dual-gate FET with elevated Au contacts.

b. False-color top view SEM images of a device with L_{ch} of 30 nm among the actually fabricated MoS_2 FETs before the fabrication of the top gate.

c. False-color cross-sectional TEM image of a representative MoS_2 dual-gate FET

d. TCAD simulation model of the MoS_2 dual-gate FET fabricated based on the observed TEM image. MoS_2 is represented in black, HfO_x in red, and the source (S), drain (D), and back gate (BG) metals are implemented in the form of the potential touching the surface. The top surface, represented in purple, is calculated as empty in the case of single gate simulation and with the potential of the Au in the case of dual gate simulation. The reproduction of such an elevated contact structure in the simulation enables the calculation of the role played by the fringing field.

e. The I_{on} values calculated through TCAD modeling for single gate and dual gate configurations in monolayer and bilayer MoS_2 FETs. The on-state is defined at V_{ds} = 1 V and V_{gs} = 3 V. Primarily, due to the smaller band gap in bilayer MoS_2, approximately a threefold increase in I_{on} was calculated in the same single gate configuration compared to the monolayer. A twofold increase in I_{on} in the dual gate compared to the single gate is expected due to the twofold gating effect. However, in the case of bilayer, more than a twofold unidentified increase in I_{on} is observed.

f. Visualized electrical potential of a monolayer MoS_2 FET in HfO_x and MoS_2 at the on-state (V_{ds} = 1 V, V_{gs} = 3 V) for both single gate and dual gate configurations.

g. Visualized electrical potential of a bilayer MoS_2 FET in HfO_x and MoS_2 at the on-state for both single gate and dual gate configurations.

h. Line profile along the y-direction of the conduction band (CB) energy and corresponding electron density within monolayer MoS_2. While the presence of a fringing field-induced barrier near the source electrode is evident, the difference between single and dual gate configurations is not substantial.

i. Line profile along the y-direction of the CB energy and corresponding electron density within the top layer of bilayer MoS_2. The reduction in the barrier due to the introduction of the dual gate through the fringing field is clearly evident.

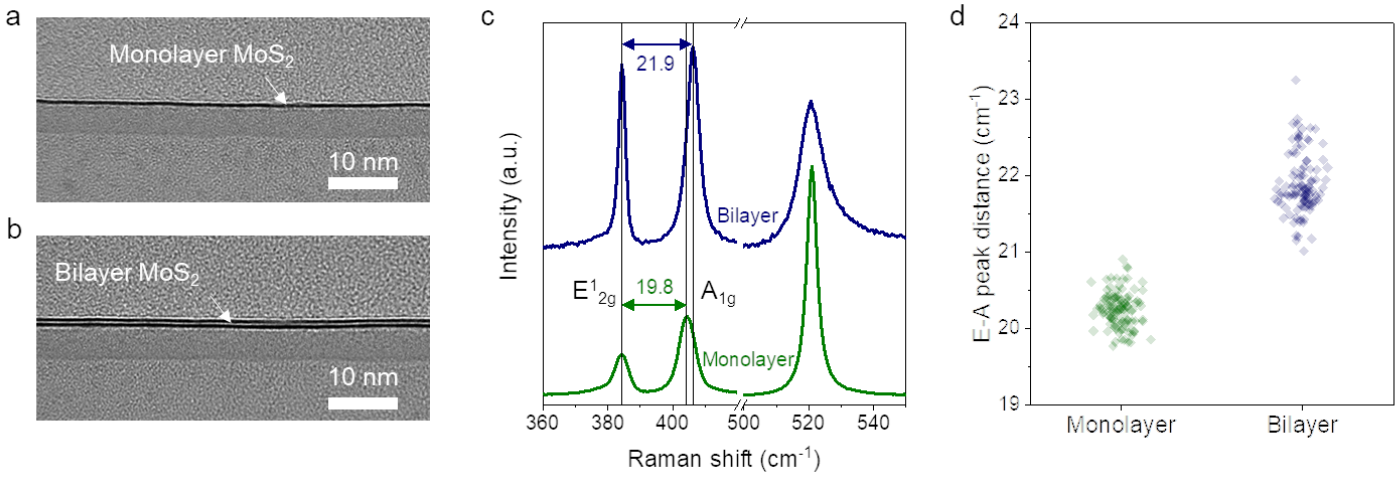


Figure 2

Characterization of 200-mm scale MoS_2 film

a. Cross-sectional TEM image of a monolayer MoS_2 film.

b. Cross-sectional TEM image of a bilayer MoS_2 film.

c. Representative Raman spectra of monolayer (green) and bilayer (navy) MoS_2 film. A clear blue shift of the A_{1g} peak resulted from the increase in the layer number, leading to the enhanced distance between peaks A_{1g} and E^1_{2g}. The peak around 520 cm^{-1} on the far right is attributed to the Si peak, and, likewise, an increase in the layer number leads to both broadening and a decrease in intensity.

d. Distribution of E-A peak distances obtained from Raman spectra at 1 cm intervals across a 10 cm x 10 cm area for monolayer and bilayer MoS_2 films. The distinct separation of film thickness is clearly evident on average.

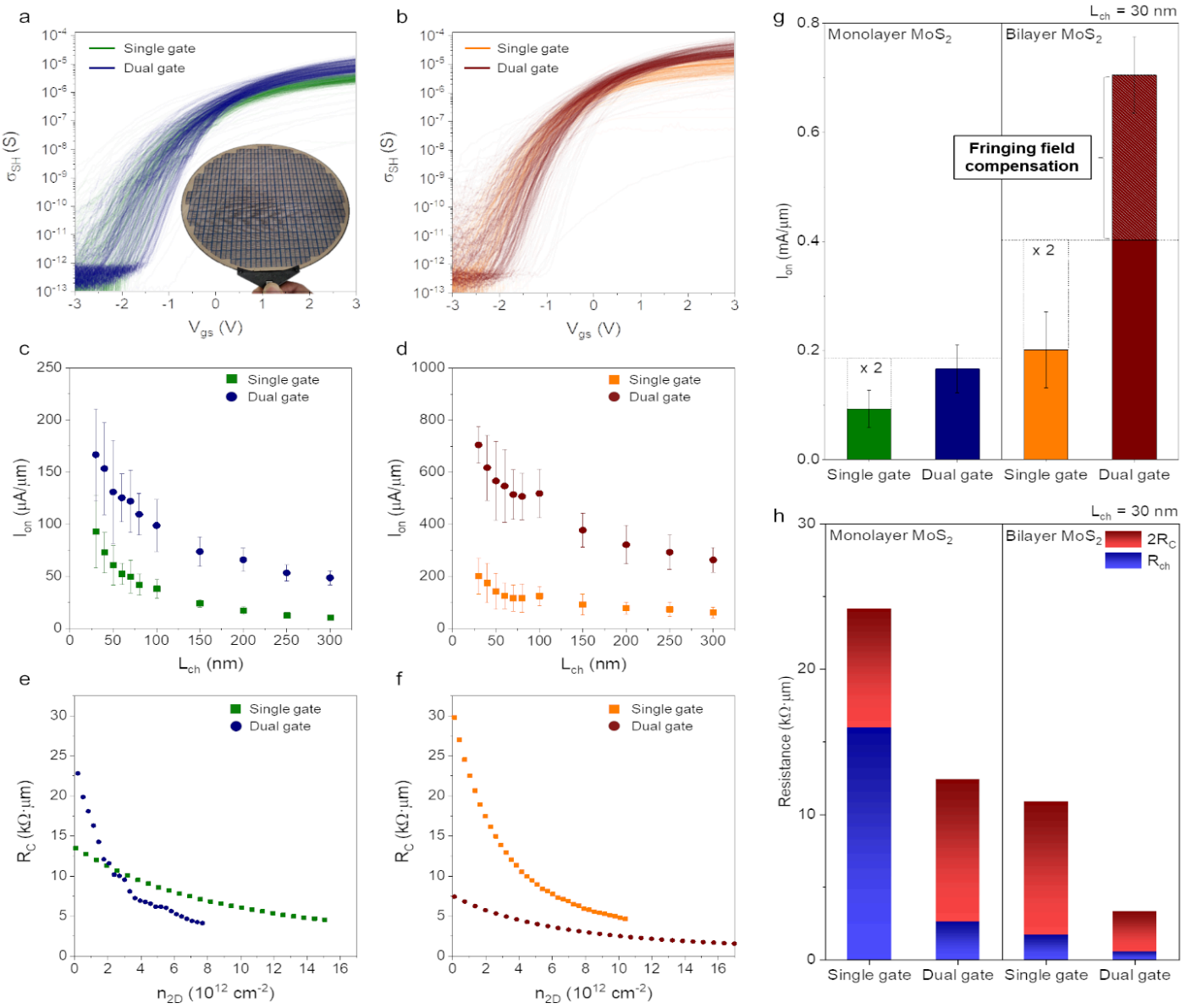


Figure 3

Statistical electrical property analysis of a 200-mm scale FET array.

a. Transfer curves ($\sigma_{SH} - V_{gs}$) of fabricated monolayer MoS_2 FETs with single-gate (green) and dual-gate (navy) configurations. The transistor's L_{ch} varies from 30 nm to 300 nm, and the channel width varies from 500 nm to 3 mm. To normalize for the various channel dimensions, the y-axis is plotted in terms of conductance. The inset is a photo showing the MoS_2 FET array fabricated on a 200-mm wafer.

b. Transfer curves of bilayer MoS_2 FETs with single-gate (orange) and dual-gate (wine) configurations.

c. A graph plotting the I_{on} values extracted from transfer curves of a monolayer MoS_2 FET array as a function of L_{ch}.

d. The same graph of a bilayer MoS_2 FET array.

e. A graph plotting the statistically extracted R_C from the monolayer FET array using the TLM method as a function of the plane carrier density (n_{2D}). The minimum R_C values for single gate and dual gate configurations are at a similar level.

f. The same graph for the bilayer FET. A significant drop in R_C is cleanly observed in the dual gate configuration.

g. The average on-current for both single gate and dual gate configurations in bilayer and monolayer MoS_2 FET arrays with a 30 nm L_{ch}. As predicted in the simulation, a roughly twofold increase in current was observed in the dual gate compared to the single gate in monolayer, and similarly, a more than twofold increase in current was observed in bilayer. As validated by the simulation, it was discovered that this additional increase in current is due to the compensation of the fringing field by the top gate.

h. Resistances of single gate and dual gate configurations for monolayer and bilayer FETs with a L_{ch} of 30 nm. $2R_C$ (red) and channel resistance (R_{ch}) (blue) extracted through TLM are shown.

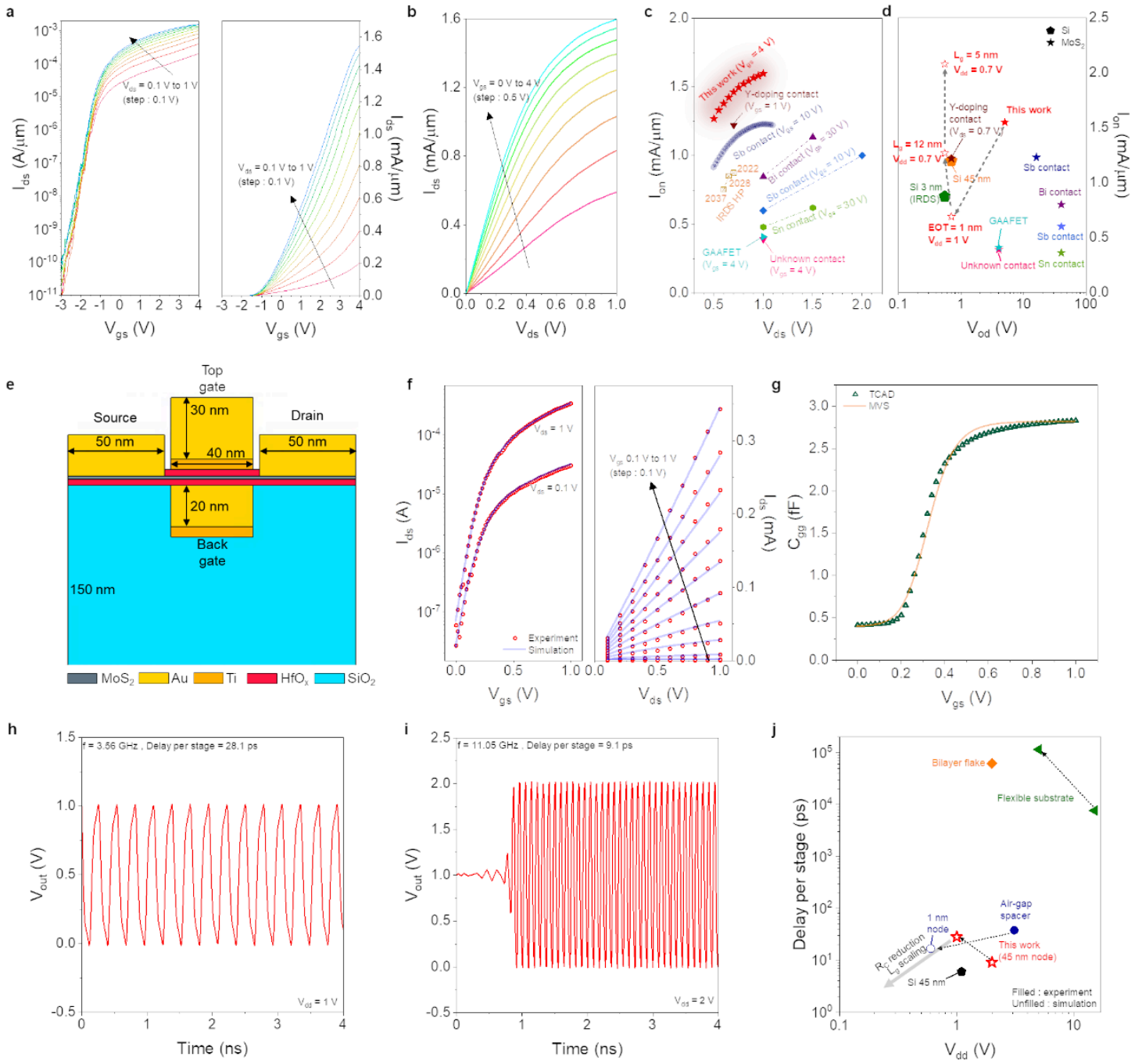


Figure 4

Benchmarking of the best dual-gate bilayer MoS_2 FET and simulation results of a ring oscillator

a. Transfer curves (I_{ds} – V_{gs}) of the best bilayer MoS_2 dual-gate FET measured under V_{ds} varying from 0.1 V to 1 V with a step of 0.1 V, plotted in semi-log scale (left) and linear scale (right).

b. Output curves (I_{ds} – V_{ds}) of the same FET plotted in linear scale under V_{gs} varying from 0 V to 4 V with a step of 0.5 V. The observation of linear curves in the sub-saturation regime for all curves suggests the formation of ohmic contacts.

c. A benchmark plot comparing the record-high on-current observed in our device with other studies as a function of V_{ds}.[9,10,27,28,48,49] Despite being obtained at lower V_{ds} compared to results using other single crystals, our on-current is the highest. The yellow boxes represent the I_{on} and V_{dd} requirements for IRDS HP in the years 2022, 2028, and 2037,[5] respectively. While direct comparison with the advanced Si transistors is not possible due to the broad operating voltage range of our device, it can be demonstrated that the 2D channel allows for sufficiently high current.

d. A plot benchmarking the I_{on} of MoS_2 FETs from c based on overdrive voltage ($V_{od} = V_{gs} - V_{th}$). MoS_2 FETs are represented by star symbols, and Si FETs are represented by pentagon symbols.[33] Notably, the actual I_{on} of our best device are represented by filled red star symbols, while the unfilled red star symbols indicate how the I_{on} change as the EOT, operating voltage, and gate length are adjusted to advanced technology nodes.

e. Device structure for TCAD simulation. A structure with no overlap between the source/drain electrodes and the gate electrode was assumed. The thickness of the bilayer MoS_2 was set to 1.5 nm, and the thickness of HfO_x, with an EOT assumed to be 1 nm, was set to 3.1 nm.

f. The experimentally obtained (red circles) and the calibrated through the Verilog-A MIT virtual source (MVS) model (blue line) transfer curves (left) and output curves (right). The experimental values here were obtained from the transfer curves and output curves in **a** and **b**, assuming EOT scaling and V_{th} shift. The actual width of the device, 500 nm, was included to convert to the actual current.

g. Gate capacitance curves (C_{gg} - V_{gs}) calculated using TCAD (green triangle) for structure of e and those calculated using the MVS model (yellow line).

h. Simulated output signal of a 2D CMOS-based 5-stage ring oscillator at V_{dd} = 1 V. The frequency was measured at 3.56 GHz, and the delay per stage was calculated to be 28.1 ps.

i. Plot similar to **h** obtained at V_{dd} = 2 V. The frequency was extracted as 11.05 GHz, and the delay per stage was 9.1 ps.

j. Plot benchmarking the delay per stage of our ring oscillator as a function of V_{dd}. Experimental results are indicated by filled symbols, while simulation results are represented by unfilled symbols.[22,33,35,50,51]

Supplementary Files

This is a list of supplementary files associated with this preprint. Click to download.

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- SupplementaryInformationfinal.pdf