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## Article

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# Hybrid memristor-CMOS neurons for *in situ* learning in fully hardware memristive spiking neural networks

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## Abstract:

Spiking neural network, consisting of spiking neurons and plastic synapses, is a promising but relatively underdeveloped neural network for neuromorphic computing. Inspired by the human brain, it provides a unique solution for highly efficient data processing. Recently, memristor-based neurons and synapses are becoming intriguing candidates to build spiking neural networks in hardware, owing to the close resemblance between their device dynamics and the biological counterparts. However, the functionalities of memristor-based neurons are currently very limited, and a hardware demonstration of fully memristor-based spiking neural networks supporting *in situ* learning is very challenging. Here, a hybrid spiking neuron by combining the memristor with simple digital circuits is designed and implemented in hardware to enhance the neuron functions. The hybrid neuron with memristive dynamics not only realizes the basic leaky integrate-and-fire neuron function but also enables the *in situ* tuning of the connected synaptic weights. Finally, a fully hardware spiking neural network with the hybrid neurons and memristive synapses is experimentally demonstrated for the first time, with which *in situ* Hebbian learning is achieved. This work opens up a way towards the implementation of spiking neurons, supporting *in situ* learning for future neuromorphic computing systems.

## Introduction

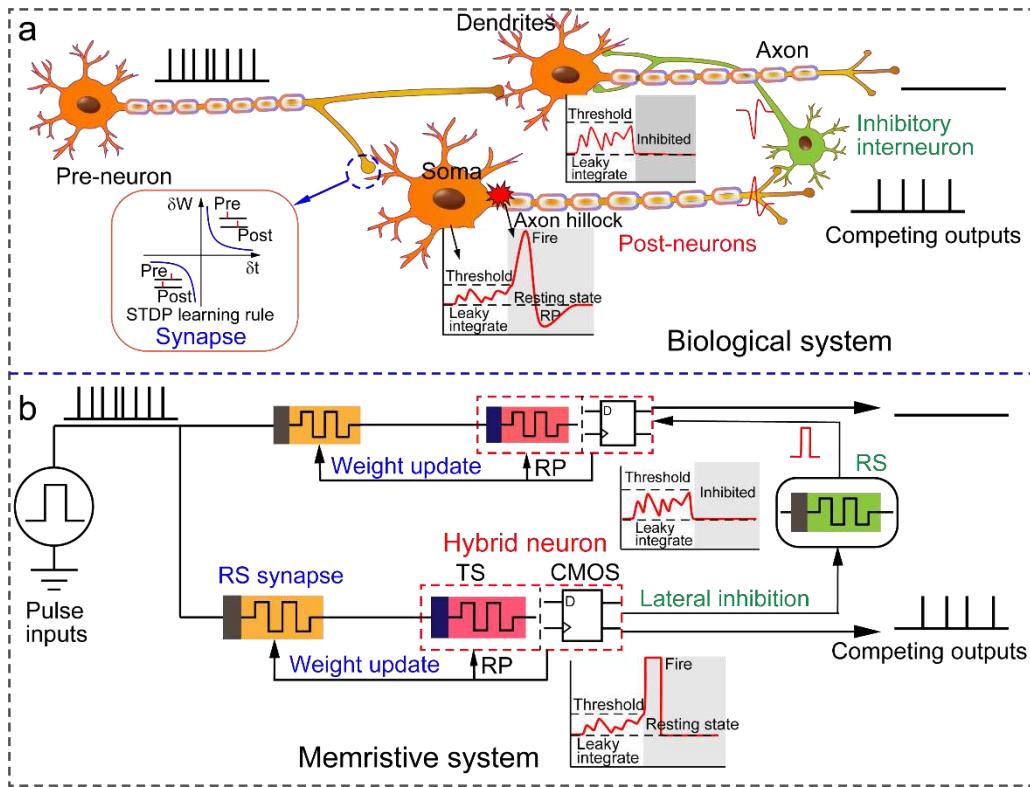
Inspired by the human brain, the spiking neural networks (SNNs) encode timing signals into the computing process, where the spike-based temporal processing allows sparse and efficient information transfer, conversion, and storage<sup>1,2</sup>. Building an SNN system in hardware is promising and attractive for performing edge tasks with great efficiency in the big-data era<sup>3</sup>. Lately, significant efforts with impressive progress have been made towards the implementation of SNN chips based on CMOS (complementary metal-oxide-semiconductor) technology, such as TrueNorth from IBM<sup>4</sup>, Loihi from Intel<sup>5</sup>, and Tianjic from Tsinghua University<sup>6</sup>, et al. Nevertheless, due to the lack of similarities between CMOS devices and biological components at physical mechanism level, the CMOS devices without the intrinsic neuronal dynamics can only simulate rather than faithfully emulate neurons functions. Even the simplest simulation of neuron functions would require such silicon neurons to have a fairly complex circuit<sup>7-9</sup>, which further grows quickly with more fidelity and functionalities<sup>10,11</sup>. Therefore, compared to the biological neurons, these bulky neuron circuits are less area or energy efficiency, which will limit its edge applications due to energy constraints as well as its cloud application due to the limited number of neurons that can be integrated on chips.

To achieve the area and energy efficiency comparable to the neurons in the human brain, nanoscale emerging memristive devices, such as ion-based threshold switching (TS) devices<sup>12-15</sup>, Mott-transition devices<sup>16-20</sup>, resistive switching (RS) memory<sup>21-23</sup>, phase-change memory<sup>24,25</sup>, magnetic memory<sup>26-28</sup>, and ferroelectric memory<sup>29-32</sup>, have recently been demonstrated to emulate spiking neurons. For example, Tuma et al<sup>24</sup> used a single phase-change device to realize an integrate-and-fire neuron function with stochastic

dynamics and the detection of temporal correlations. Subsequently, the same group further combined this neuron with phase-change synapses and demonstrated the detection of multiple temporal correlations through using level-tuned neuronal characteristics<sup>25</sup>. Wang et al<sup>12</sup> used the dynamic migration of Ag in a host dielectric material to emulate the stochastic leaky integrate-and-fire (LIF) process in neurons and demonstrate a fully memristive SNN system with unsupervised learning. Attributing to the intrinsic dynamics in a single memristive device, neurons in these works are more energy and area efficient than CMOS-based ones. However, these memristor-based neurons focus on the emulation of single neuron's functionalities, without considering the actual requirements for system realization in hardware. Thus, the functional diversity (such as generating *in situ* learning and lateral inhibition signals) of these neurons remains to be demonstrated, the stability (such as firing under continuous stimuli inputs) needs great improvement, and the fully hardware system-level demonstration is primitive.

Here, we design a hybrid memristor-CMOS leaky integrate-and-fire (LIF) spiking neuron to enhance the fidelity and functionality of memristor-based neurons. In this neuron circuit, a single TS memristor serves as the dynamic integrator of the post-neurons to collect input signals from the pre-neurons and determines whether to fire or not. Simple digital circuits detect the fire event and output reproducible spike signals, as well as ensuring the stable firing of the memristor under pulse train inputs by supplying a refractory period (RP) signal. In the hybrid neuron, the TS memristor provides the dynamics for neuromorphic functions, and transistors supply the signal amplification to enable larger and multilayer networks. For performing *in situ* learning operations on memristive synapses, potentiation, depression, and lateral inhibition signals are

introduced into the neuron successfully, and a lateral inhibition array (LIA) is specifically designed. Using the hybrid neurons and LIA, we further experimentally demonstrate a  $30 \times 10 \times 10$  fully hardware multilayer SNN (MSNN) with RS synapses. In this MSNN, the training processes are *in situ*, 10 hidden neurons perform feature extraction with the LIA in the first layer, and 10 output neurons serve for further recognition in the second layer. The experimental results show that the hybrid neurons could perform *in situ* tuning on RS synapses and have the potential to build self-adaptive spiking neuromorphic systems.



**Fig. 1. Biological neural system vs. memristive system.** **a**, Schematic of a biological neural system. The post-neuron receives input signals from the pre-neurons through the connected synapses and changes its membrane potential. An action potential generates at the axon hillock once the membrane potential surpasses a threshold value. The fired neuron could inhibit neighboring neurons through interneurons. The relative timing of pre- and postsynaptic spikes could *in situ* modify the synaptic strength, i.e., the spike-timing-dependent plasticity (STDP)

learning rule. **b**, Frame diagram of the hybrid neuron driven memristive system. The resistive switching (RS) memristor serves as synapses and lateral inhibition connection. The hybrid neuron contains a threshold switching (TS) memristor and simple digital units (CMOS), in which the TS devices perform the leaky integrate-and-fire neuron function, and the digital units generate active spikes, refractory period (RP) signals, *in situ* weight updating signals, and lateral inhibition signals.

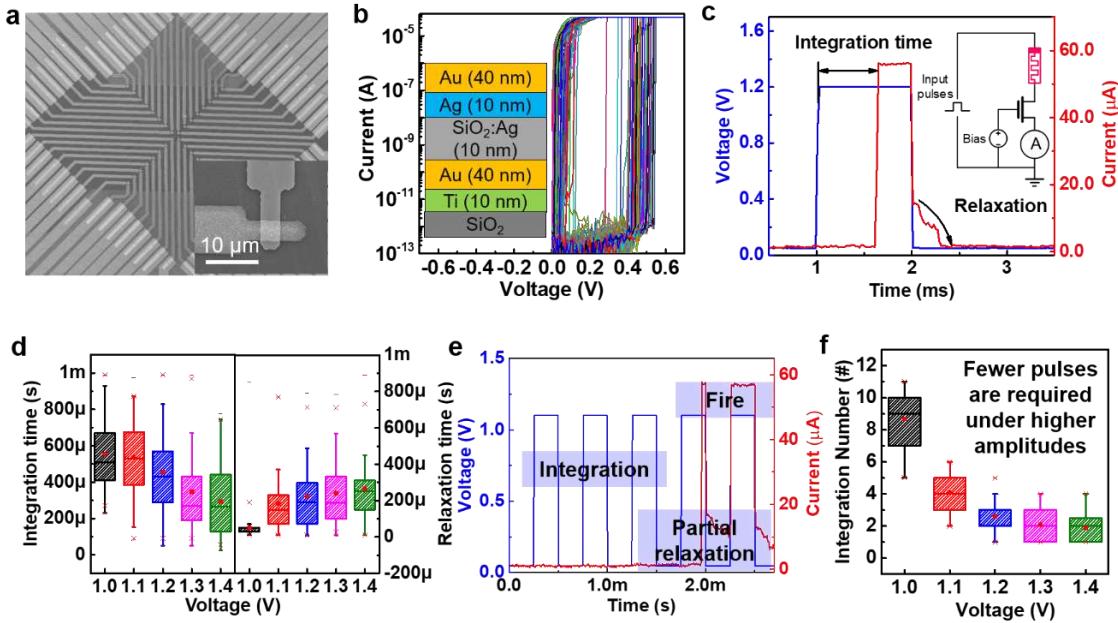
## Results

### Design principles of the neuron circuits

Figure 1a shows the schematic of a biological neural system, constructed with a variety of neurons and connected plastic synapses. In such a system, a typical neuron mainly includes numerous dendrites, a soma, and an axon<sup>33,34</sup>. Together with the soma, the dendrites of post-neurons receive and integrate the excitatory or inhibitory signals from pre-neurons and raise the membrane potential<sup>34,35</sup>. Once the membrane potential surpasses a threshold, the axon hillock generates an “all-or-none” action potential (AP) through the opening or closing of the voltage-gated ion channels. The “all-or-none” feature of AP makes the biological neuron perform the signal gain function and ensure the AP transmission in a deep network. After firing, the membrane potential recovers to the resting state within a refractory period and prepares for the next spiking event. Thus, the neuron could fire continuously under a string of AP inputs. The axon-terminals (of the pre-neuron) and dendrite-terminals (of the post-neuron) form the synapses whose strength (synaptic weight) dictates the intensity of the signal passing from the pre-neurons to the post-neurons. Importantly, the synaptic weight can be *in situ* modified according to the relative timing of pre- and postsynaptic spikes (spike-timing-dependent plasticity (STDP) learning rule)<sup>36-38</sup>, which is believed to be one of the key mechanisms

for organisms to learn and dynamically adapt to the external environment. Furthermore, the lateral inhibition between post-neurons through inhibition interneuron is another key feature in biological systems, in which the excited neurons inhibit other nearby or connected neurons<sup>39</sup>. The lateral inhibition behavior enables the brain to manage the sensory inputs, avoid information overload, and support a network to perform competitive learning<sup>39,40</sup>.

Inspired by the biological system, we design a hybrid spiking neuron to construct a memristive SNN in hardware, as schematically shown in Fig. 1b. In this neuron circuit, the TS memristor serves as a gated membrane to dynamically integrate the input signals through the growth of Ag filaments and induce a fire event determined by the TS switching nature of the device (abrupt switching from a highly resistive OFF state to a highly conductive ON state). The CMOS units shape a fixed output spike for performing the signal gain function and ensure the continuously firing behavior of the TS memristor under pulse train stimuli through supplying a refractory period (RP) feedback signal. Within the RP, the device spontaneously relaxes back to its initial state, without needing any reset operation. This is attributed to the self-rupture of Ag-channel by interfacial energy minimization between Ag and dielectrics, or Thomson-Gibbs effect<sup>12,41,42</sup>. Under the help of the CMOS units, the weight updating signals are successfully introduced into the neuron circuits to *in situ* modulate the RS synaptic weights. Furthermore, to support competitive learning in a network, the CMOS units also supply a lateral inhibition signal to other neurons through RS devices (more circuit details are presented in Fig. 3).



**Fig. 2. Characteristics of the TS device.** **a**, Scanning electron microscope (SEM) image of the TS array, includes 32 discrete devices ( $4 \mu\text{m} \times 4 \mu\text{m}$ ). The inset shows a zoom-in image of a single device. **b**, 100 typical I-V switching curves of the device under positive voltage sweeps. Inset: the device structure used in this work. **c**, The current response of the device under a 1.2 V pulse (1 ms width) followed by a 0.05 V monitor voltage. Inset: the schematic of the testing circuit. **d**, The statistical data of the integration time and relaxation time as a function of the pulse amplitudes under 1 ms pulse width. **e**, The integration behavior of the TS device under multiple pulses (1.1 V, 250  $\mu\text{s}$  width, 250  $\mu\text{s}$  interval time) with 0.05 V monitor voltage between pulses. After the first fire, the device cannot completely return to its initial HRS due to the interval time is not enough for finishing a complete relaxation, and thus induces a sub-threshold firing. **f**, The statistical data of the required pulse number for the first firing under different pulse voltages (with 250  $\mu\text{s}$  width and interval time). Fewer integration pulses are required under higher voltages.

### Neural characteristics of the TS memristor

As mentioned before, the TS memristor plays a key role in the hybrid neuron. To obtain a stable spiking behavior of the neuron and apply it for networks, a TS memristor array that

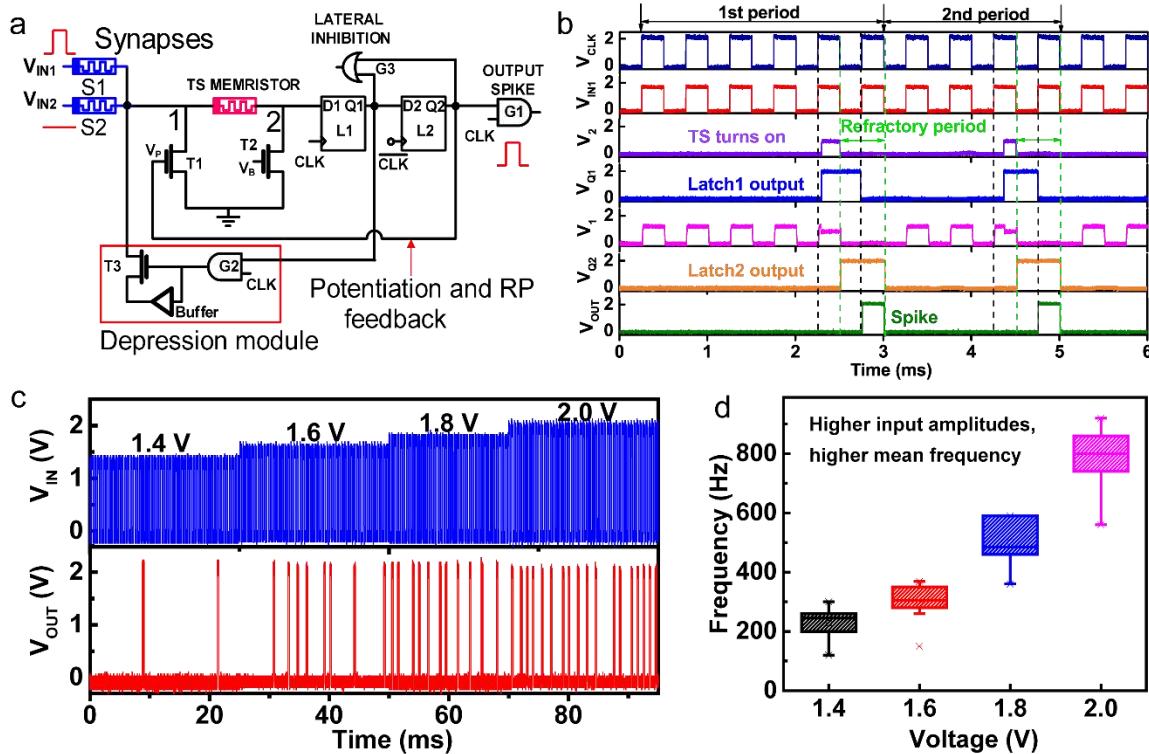
contains 32 discrete devices was fabricated, as shown in Fig. 2a, and the TS device with Au/Ag/SiO<sub>2</sub>:Ag/Au structure is shown in the inset of Fig. 2b. Initially, the device is in a high resistance state (HRS) and features forming-free owing to the doping technology<sup>43-45</sup>, which is important for large-scale integration. The fabrication process is described in Methods. Fig. 2b shows typical volatile I-V switching curves of the TS memristor under 100 positive voltage sweeps. During the switching process, once the applied voltage surpasses a threshold, the device switches from an HRS to a low resistance state (LRS) because the Ag-channel(s) is formed within the SiO<sub>2</sub> dielectric<sup>46-49</sup>. When the applied voltage is below a hold value, the device relaxes back to an HRS due to the Ag-channel's spontaneous rupture<sup>42,46,49,50</sup>. It should be noted that the growth and rupture processes of the Ag-channel have stochastic physical dynamics, indicating the switching voltages between each cycle follow a probability distribution function (see statistical data in Supplementary Fig. 1). This provides the stochastic neuronal behavior inherent to the memristor-based neuron, thus does not need any external random number generators required in CMOS-based neurons<sup>11</sup>.

To further study the device characteristics for emulating LIF neurons, we switched the device with pulses, as shown in Fig. 2c. During the measurement, we used a transistor instead of a fixed resistor to limit the current to protect the TS device (inset of Fig. 2c). The transistor also serves as a read-out resistor that is beneficial for integration in the designed hybrid neuron. The dynamic response of the device under a 1.2 V/1 ms post-synaptic pulse monitored by 0.05 V read voltage was observed. Within a certain delay time, the Ag atoms gradually accumulate in the SiO<sub>2</sub> dielectric layer with the effect of the electric field and redox reaction<sup>41,46,47,51</sup>, corresponding to the integration process.

Eventually, an Ag-channel forms and induces an LRS of the device, representing the fire behavior of neurons. When the applied trigger voltage is ceased, the device relaxes back to its HRS spontaneously, indicating the “leaky” feature of the biological neuron membrane. Compared with the non-volatile memristor-based neuron<sup>24</sup>, the TS device’s volatile feature allows our artificial neuron to automatically recover to its resting state after firing and without the need for extra reset operations, just like the biological neurons, thus reduces the circuit complexity and energy consumption. To study the effect of the pulse amplitude on integration time and relaxation time, pulses with different amplitudes but fixed 1 ms width were applied on the device, and the statistical data are shown in Fig. 2d. The results show that with increasing the pulse amplitudes from 1.0 V to 1.4 V, the integration time decreases while the relaxation time increases. In other words, a higher post-synaptic voltage needs a shorter time to fire the post neurons and vice versa, which is similar to what observed in biological neurons<sup>33</sup>. Both the required integration time and relaxation time under different amplitudes show a probability distribution (see Supplementary Fig. 2) because of the stochastic growth and rupture processes of the Ag-channel(s). These features equip the TS memristors with the highly desirable stochastic neuronal dynamics and spontaneous repolarization capabilities in biological neurons<sup>52</sup>. Recently, the stochasticity has been successfully demonstrated in PCM-based neurons and presents the potential for population code<sup>24</sup>.

Here, for performing the LIF behavior of neurons under multiple stimuli, pulses with shorter width (250  $\mu$ s) and interval time (250  $\mu$ s) were operated as the input signals, as shown in Fig. 2e. Four pulses are required to trigger the first fire event, indicating a multiple pulse LIF process. The statistical data of the pulse number for firing under

different pulse amplitudes is shown in Fig. 2f. Fewer integration pulses are required under higher amplitudes. Hence, the neuron firing rates can be modulated by the post-synaptic action potential that depends on the connected synaptic weights. It is worth noting that, to prepare for the next LIF behavior, the waiting time after firing must be longer than the device's relaxation time. Therefore, after the first firing event (Fig. 2e), the device cannot decay to its initial HRS before the next input pulse coming because the interval time is insufficient. This phenomenon indicates that the simple TS device cannot fire continuously under pulse train stimuli, which is a general challenge observed in capacitor-less memristor-based neurons<sup>12,15,18,30,32</sup>. For pursuing a practical application, a refractory period is needed to enable the device to recover to its HRS and perform continuous LIF behavior under the pulse train inputs. Thus, in this work, we introduce an RP feedback signal into the hybrid neuron circuit to solve this problem (more details are presented in Fig. 3).



**Fig. 3. Hybrid memristor-CMOS neuron circuit and characteristics.** **a**, Schematic of the hybrid neuron circuit. A single TS device serves as the gated membrane for performing the leaky integrate-and-fire neuron function. Two D-type latches (L1 and L2) and a AND gate (G1) are used to shape the fire signal to a fixed spike signal. The output signal from L2 is applied to the gate terminal of T1 to make the node 1 virtual ground, which is for performing synaptic potentiation operation and supplying a refractory period (RP). A buffer, a transistor T3, and a AND gate (G2) construct the depression module. An OR gate G3 that receives inputs from L1 and L2 serves as the lateral inhibition output. **b**, The sequence diagram of the output values on five key nodes under continuous input pulses (1.8 V, 2 kHz, 250  $\mu$ s width) within two continuous firing cycles when disabling the depression feedback circuit. **c**, The continuous spiking behavior under different input voltages on  $V_{IN1}$ . **d**, The statistical results of spiking frequencies as the function of the input pulses amplitudes, the frequency increases with increasing the input pulse amplitudes.

### Hybrid neuron circuit and the characteristics

Figure 3a shows the details of the hybrid neuron circuits, whose area is estimated to be about  $50 \times$  less than a 1 pF NMOS capacitor on a 14 nm technology node<sup>24</sup>. The CMOS units include two D-type latches (L1 and L2), an AND gate (G1), an OR gate (G3), and a depression module. The G1 generates the output spike signal, and G3 generates the lateral inhibition signal. The output of the L2 serves as both the potentiation and refractory period signal to control the transistor T1. The output of L1 triggers the depression feedback circuit that consists of a AND gate (G2), a buffer, and a switch transistor T3. Under a resting state, the transistor T1 is in an off-state, and the electrical potential of node 1 is the post-synaptic action potential. When the TS device fires, a feedback signal from L2 makes the T1 in an on-state, and node 1 is a virtual ground. The

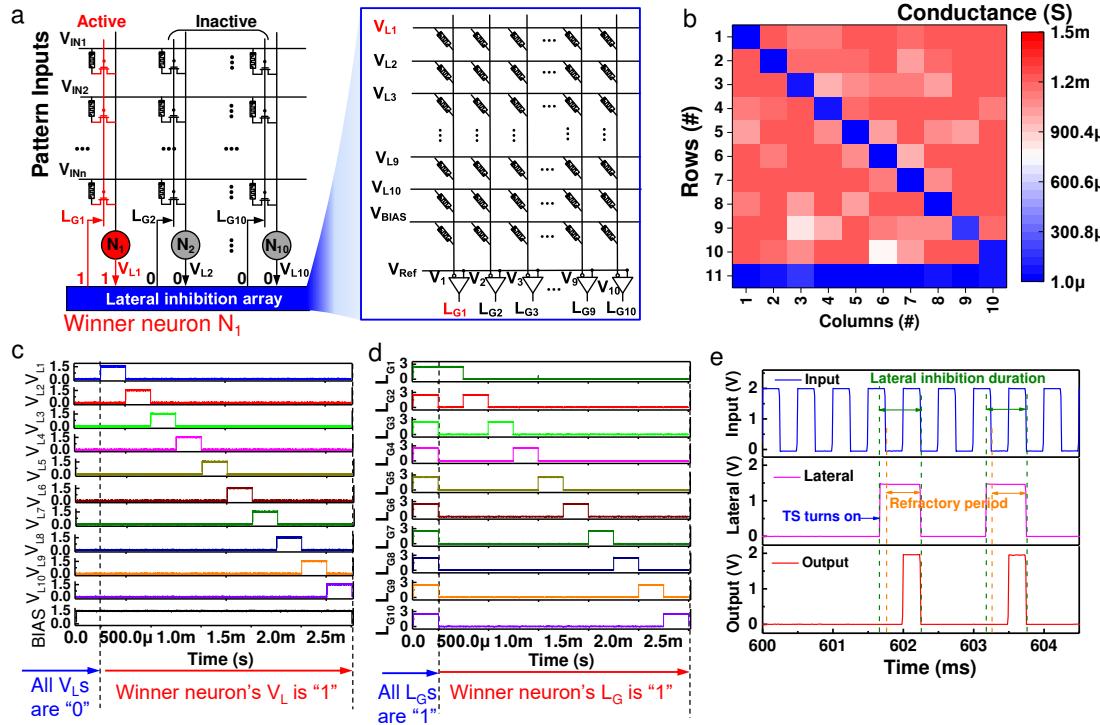
virtual ground of node 1 leaves a refractory period for TS memristor relaxing back to its HRS and potentiates the related synaptic weights that with input pulses. Initially, the depression module can be considered as an open circuit because the voltage on the T3 gate is zero. When the TS device fires, the output signal from L1 activates the depression module and lifts the potential of node 1 (see Supplementary Fig. 3), thus depressing the synapses whose inputs are zero. Given the opening of T1 and T3 happens within two different clock periods, the potentiation and depression operations do not conflict with each other, and the neuron could support an optimized Hebbian learning rule<sup>36,53</sup> (see Supplementary Fig. 4). Fig. 3b shows the measured output sequence diagram of five critical nodes in the neuron circuit within two adjacent firing cycles. Noting that for clearly present the voltage evolution on critical nodes, the depression module is disabled during the measurement. Here, two fixed resistors are performed as RS synapses ( $S1 = 10\text{ k}\Omega$  and  $S2 = 40\text{ k}\Omega$ ).  $V_{IN1}$  receives input pulses, and  $V_{IN2}$  is grounded. On the fifth input pulse within the first firing cycle, the TS memristor fires, leading to an abrupt increment of the voltage on node 2. Then voltage on node 2 serves as the input of L1 and induces a high-level output of L1 under the control of the CLK signal. Subsequently, the output of L1 (the input of L2) activates the L2 to output a high-level voltage that turns on the T1. When the T1 is on, the potential on node 1 is nearly zero, which offers the TS memristor a sufficient time (refractory period ( $500\text{ }\mu\text{s}$ ) + interval time ( $250\text{ }\mu\text{s}$ )) to decay to its initial HRS state and prepare for the next firing event. During this period, the G1 generates an output spike by carrying out the ‘AND’ logic operation of ‘L2 OUTPUT’ and ‘CLK’. The CLK signals are provided by a global (shared) signal generator, with 2 kHz and 50% duty cycle. All output spikes are identical because the output spike results from the

“AND” operation of the L2 output and the global CLK signal. Thus, the circuit could output a fixed spike signal, emulating the “all-or-none” feature of the action potential in biological neurons<sup>33</sup>.

The continuous firing behavior of the neuron under pulse train with different amplitudes (from 1.4 V to 2.0 V, 2 kHz frequency, 250  $\mu$ s width) are shown in Fig. 3c, equivalent to the firing behaviors under identical input pre-neuron pulses but different synaptic weights. Intuitively, the spiking frequency increases with increasing the amplitudes, demonstrating that the neuron could classify different stimuli intensity by giving a different spiking frequency. Identical forms of all output spikes are observed (2.0 V, 250  $\mu$ s width, the visual error results from the read fluctuation, see the zoomed-in view in Supplementary Fig. 5). Figure 3d shows the spiking frequency’s statistical results as a function of the input pulse amplitudes, further confirming that the neural spiking frequency increases with increasing the input pulse amplitudes. Besides, attributing to the active digital components, the hybrid neuron could enable the adjacent neurons directly. The spiking behavior of two connected neurons was tested (see supplementary Fig. 6). The results indicate that the proposed hybrid neuron could propagate the spiking signals in multilayer networks through connected synapses, just like what observed in biological systems.

To further demonstrate the neuron’s feasibility for performing *in situ* learning, two RS synapses (Ta/HfO<sub>2</sub>/Pd) are connected to the neuron circuits (see Supplementary Fig. 3a). Initially, the synapses S1 and S2 are programmed into a medium resistance state (~ 400  $\mu$ S @ 0.2 V). Then a series of pulses are applied on the input terminal V<sub>IN1</sub>, and V<sub>IN2</sub> is zero. Compared to Wang’s work<sup>12</sup>, both the synaptic potentiation and depression

operations are performed within the neuron and avoid using any external depression control circuits, which in some certain decrease the system hardware overhead and more faithfully implement the Hebbian learning process in the biological system<sup>36,53</sup>. During learning, the increased potential of node 1 is clearly observed (Supplementary Fig. 3b), which used to depress the synapse S2. After learning, the synapses S1 and S2 are respectively programmed into an LRS (~980  $\mu$ S @ 0.2 V) and an HRS (~42  $\mu$ S @ 0.2 V), as shown in Supplementary Fig. 3c. Corresponding to the evolution of S1 and S2, the output spiking frequency increases with increasing the input pulse counts during the learning process (Supplementary Fig. 3d), demonstrating the *in situ* learning capability of the hybrid neuron.



**Fig. 4. Lateral inhibition circuits for the winner-take-all learning rule.** **a**, Schematic of the lateral inhibition array (LIA) circuit for ten neurons, which contains a resistive switching (RS) array and comparators. The outputs of LIA are applied to the shared gates of 1T1R synapses to

implement lateral inhibition. The lateral inhibition signals ( $V_{L1}$ – $V_{L10}$ ) from neurons serve as the inputs of the LIA, and the outputs of the comparators are applied to the shared gates of 1T1R synapses.  $V_{BIAS}$ : 1.5 V,  $V_{Ref}$ : 50 mV. **b**, The pre-programmed weight conductance of the memristor array used in the LIA circuit for ten neurons. **c**, Two input conditions of the LIA while performing lateral inhibition operation, the input signals are the neurons' lateral inhibition signals. **d**, The corresponding outputs of all the LIA ( $L_{G1}$ – $L_{G10}$ ) when two conditions in **c** serve as the inputs of the LIA. **c & d**, The Y-axis unit is volt (V). **e**, The moment when the neuron outputs lateral inhibition signal. Two firing cycles are presented.

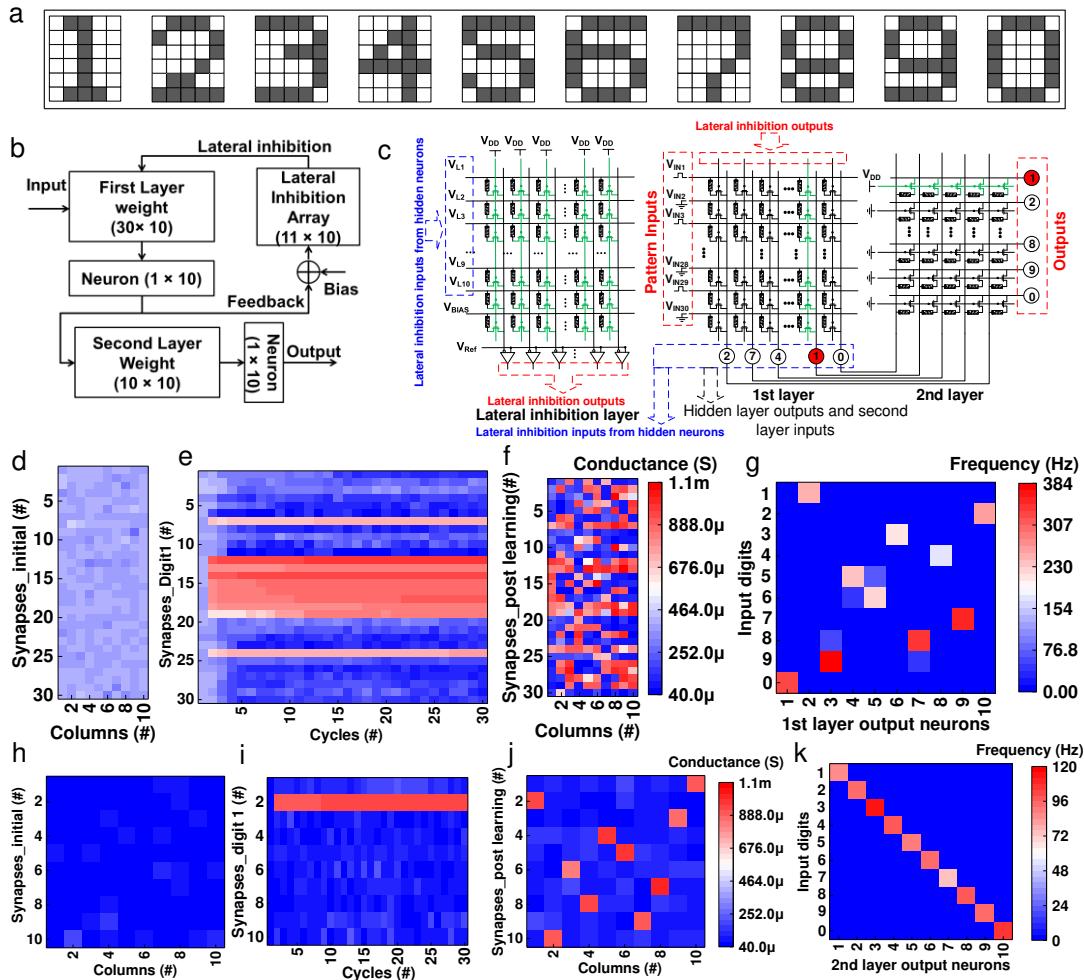
### Lateral inhibition circuits for the WTA learning rule

Lateral inhibition is a crucial feature for unsupervised learning<sup>40</sup>, and it could support the implementation of the winner-take-all (WTA) learning rule. The WTA rule indicates that once the winner neuron fires, other neurons are inhibited. To perform the WTA learning rule using the proposed neuron circuits, we design a lateral inhibition array (LIA) contains RS array and comparators, as shown in Fig. 4a. The LIA for ten post-neurons is presented and will remain feasible within thousands of neurons by simply increasing the array size ( $n \times (n+1)$ ,  $n$  is the WTA neuron numbers). For carrying out the lateral inhibition operation within post-neurons, the LIA should possess two features: First, when no neuron fires, all lateral inhibition signals from neurons ( $V_{L1}$ – $V_{L10}$ ) are “0”. Thus, all outputs of the LIA ( $L_{G1}$ – $L_{G10}$ ) should be “1” to active all synapses for an inference operation. Second, when the winner neuron fires (i.e.,  $N_1$ ), the lateral inhibition signal of  $N_1$  is “1”, and all other neurons' lateral inhibition signals are “0”. In this case, the  $L_{G1}$  of the LIA outputs should be “1” and other outputs ( $L_{G2}$ – $L_{G10}$ ) are “0”. Correspondingly, only the winner neuron's synapses are active, and other neurons' synapses are inhibited,

followed by the *in situ* learning operation on the winner neuron's synapses. Here, a bias input is introduced into the LIA to make the lateral inhibition weights valid (see mathematical analysis in Supplementary Note1). It is worthy to note that the comparators' positive terminals serve as the reference terminals, and the negative terminals receive signals from the RS array. In such a method, negative weight values could be avoided to reduce the hardware overhead of using differential resistor pairs<sup>54</sup>. Fig. 4b shows the pre-programmed weight conductance of the LIA according to the calculated weight value.

To demonstrate the performance of the LIA, we carried out the test on LIA under two input conditions: all neurons'  $V_{LS}$  are "0" (0 V), and only the winner neuron's  $V_L$  is "1" (1.5 V), as shown in Fig. 4c. In detail, for the input condition that all neurons'  $V_{LS}$  are "0", no neuron fires at the beginning, and the lateral inhibition outputs ( $V_{L1}-V_{L10}$ ) are "0" (0 V). Thus, the inputs of the lateral inhibition array are "0" (0 V), except that the bias input is "1" (1.5 V) (left part of Fig. 4c). In this case, all the LIA outputs ( $L_{G1}-L_{G10}$ ) are "1" (3 V), which is used to activate all synapses, as shown in the left part of Fig. 4d. The input condition under which only the winner neuron fires, corresponding to the case when only the winner neuron's lateral inhibition signal is "1" (1.5 V) and other neurons are silent (right part of Fig. 4c). In this case, only the winner neuron's  $L_G$  is "1" (3 V), while other LIA outputs that correspond to loser neurons are "0" (0 V), as shown in the right part of Fig. 4d. Thus, only the winner neuron's synapses could be programmed. It is clear that the lateral inhibition signal of the fired neuron happens when the TS device switches on (Fig. 4e), indicating that the lateral inhibition signal is triggered timely. These experimental results show that the LIA circuits actually possess two features as

mentioned above, thus are decent for supporting the proposed hybrid neuron to perform the lateral inhibition operation and unsupervised learning with the WTA rule.



**Fig. 5. Fully hardware multilayer SNNs.** **a**, The digital patterns used for learning, every pattern includes 30 pixels ( $6 \times 5$ ). **b**, Frame diagram of the constructed SNNs ( $30 \times 10 \times 10$ ). The first layer is constructed with a  $30 \times 10$  array and the second layer is with a  $10 \times 10$  array. A  $11 \times 10$  array with a bias input is used for lateral inhibition of the first layer output neurons. **c**, The detailed circuit schematic of the whole system. **d & h**, The initialized weight map of the first layer and second layer before learning. **e & i**, The evolution of the synaptic weights of the neuron “1” after 30 firing events when the digit “1” as input pattern. **f & j**, The final weight map of the first and second layers after learning, respectively. Clear weight distribution is observed. **d, e, f, h,**

**i & j**, Presented under the same color bar. **g & k**, The firing rates of the output neurons in first and second layers under different input digits with noise pixels during inference processes.

### Fully hardware multilayer SNNs

Based on the proposed hybrid neurons and the lateral inhibition circuits, we further demonstrate a fully hardware multilayer SNN for performing *in situ* learning. Fig. 5a shows the digital patterns that are used for learning. Each pattern includes 30 pixels ( $6 \times 5$ ). In real operations, the black pixels are recognized as “1” and then programmed into positive pulses (1.6 V, 250  $\mu$ s width, and 2 kHz). The white pixels are recognized as “0” and thus grounded. The network is constructed with a  $30 \times 10 \times 10$  structure, as shown in Fig. 5b. The 10 winner-take-all hidden neurons receive input signals from the 30 input neurons of the first layer, which can program the  $30 \times 10$  RS synapses in an unsupervised way with the help of the introduced LIA circuits. The second layer ( $10 \times 10$ ) is used for digits recognition with supervised learning. Fig. 5c illustrates the detailed circuit schematic of the SNN, and the related hardware image is shown in Supplementary Fig. 7.

We first performed the unsupervised learning on the first layer to pre-encode the input pattern (see Methods for more details). Before training, for clearly demonstrating the evolution of the synaptic devices, we set the device conductance to a medium value (~400  $\mu$ s), as shown in Fig. 5d. During training, the weight modulation (conductance change) follows the optimized Hebbian rule (Supplementary Fig. 4). Fig. 5e shows the evolution of the synaptic weights of neuron “1” after 30 firing events when the digit “1” is used as the input. The conductance of synapses is clearly programmed upon the firing events. Supplementary Fig. 8 shows the synaptic weights of the other neurons under different input digital patterns. The weight map after learning is shown in Fig. 5f, a clear

conductance distribution is observed. Furthermore, the inference firing rates under different input digits with noise pixels are shown in Fig. 5g and Supplementary Fig. 9. The results show that both neuron “6” and neuron “5” fire when the input digit is “5” (or digit “6”), as well as neuron “8” and neuron “9” when input digit is “8” (or digit “9”). This is because the hamming distance between these patterns is small<sup>55</sup>, which results in nearly the same post-synaptic membrane potential (see Supplementary Fig. 10). It is worth noting that attributing to the stochasticity of neurons, the ‘greedy’ neuron is successfully suppressed during the learning process, which is critical to perform the WTA rule with an unsupervised way<sup>52,56</sup>. For comparison, a simulation is performed on the neurons without stochasticity. The results show that all patterns are trapped by a greedy neuron and cannot carry out clustering normally (see Supplementary Fig. 11).

Then, we trained the second layer in a supervised way by applying a constant voltage on the shared gates of 1T1R synapses of the corresponding post-neurons (see methods in the experimental section). The conductance of synapses is initialized to  $\sim 40 \mu\text{S}$  (low conductance state), as shown in Fig. 5h. Fig. 5i shows the corresponding synaptic conductance evolution of digit “1” in the first 30 training iterations after applying the output signals from neuron 2 in the hidden layer. We noted that the potentiation operation of the target synapses is done within one-cycle, indicating a fast learning process, which is because the input pulse is strong enough to directly set the synaptic devices. This one-cycle learning might limit the pattern amounts learned in a large scale network but could be alleviated by adopting some optimized methods. Such as, using faster TS devices<sup>48,49</sup> that support shorter pulses to achieve analog switching of synaptic devices<sup>57</sup>, or introduce the synaptic switching probability into the learning process<sup>56,58</sup>, which requires further

study. The other corresponding synaptic devices, whose input terminals are grounded, remain nearly unchanged because the initial low conductance cannot be further programmed. The synaptic weight evolutions of the other neurons are shown in Supplementary Fig. 12. After training, the weight map of the second layer is shown in Fig. 5j. In each neuron's synapses, only one related synapse is potentiated. The locations of the potentiated synapses just right cater to the neurons with the highest rate in the hidden layer. Fig. 5k shows the firing rates of the second layer neurons under different input digital patterns with noise pixels, where clear recognition results are observed (see Supplementary Fig. 13 for spike outputs). These results demonstrate that the proposed neuron circuit could successfully perform *in situ* learning on RS synapse networks, suggesting that the hybrid neuron circuit has the potential to build a high-dense spiking neuromorphic machine with *in situ* learning capability.

## Discussion

In this work, a hybrid memristor-CMOS stochastic LIF neuron is designed to enable fully hardware implementation of SNNs. The hybrid neuron is equipped with two key features: first, the TS device brings in the highly desirable diffusion dynamics for efficiently and faithfully performing the leaky integrate-and-fire functions. Second, the simple digital circuits serve as an active pump to output “all-or-none” spikes, as well as introducing potentiation, depression, refractory period, and lateral inhibition signals into the neuron circuit. These features render the compact neurons capable of tuning synaptic weights for *in situ* Hebbian learning. Moreover, the digital module makes the neuron circuit active, which could be used to enable deep spiking neural networks.

It is worthy to note that the pulse parameter used in this study is just an example of a demonstration. The pulse width that serves as input could be scaled to  $\mu$ s, even ns level according to recent experimental data of the TS memristor<sup>48,49</sup>, and thus could implement faster computing. Furthermore, the presented hybrid design concept may extend to other memristor technologies, such as NbO<sub>2</sub> and VO<sub>2</sub> that have shown promising dynamics for emulating spiking neurons<sup>17,20</sup>.

To perform unsupervised learning with the WTA rule, an LIA circuit that consists of an RS array and comparators is devised to work with the hybrid neurons. By combining the LIA circuit and hybrid neurons, we further experimentally demonstrated a fully hardware two-layer ( $30 \times 10 \times 10$ ) SNNs, on which *in situ* learning operations has been successfully performed. This work paves the way towards hardware implementation of sophisticated and yet highly efficient spiking processors by leveraging the advantages of both emerging and CMOS devices.

## Methods

*TS memristor fabrication:* The TS memristor used in the demonstration were fabricated on p-type (100) Si wafers with 100 nm thick thermal oxide. The fabrication processes of the Ti/Au/SiO<sub>2</sub>:Ag/Ag/Au devices are as follows. First, vertical lines of Ti/Au (10/40 nm) as bottom electrodes were deposited on the SiO<sub>2</sub>/Si substrate by e-beam evaporation after the first lithography process and released by the first lift-off process. Then, after the second lithography process, 10 nm SiO<sub>2</sub> co-sputtered with Ag was deposited to form the functional layer followed by the second lift-off process. Finally, after the last lithography step, horizontal lines of Ag/Au (10/40 nm) as top electrodes were deposited on the SiO<sub>2</sub> film by magnetron sputtering, and then the Ti/Au/SiO<sub>2</sub>:Ag/Ag/Au devices were released

by the third lift-off process. The area of the devices used for experimental demonstration is  $4 \mu\text{m} \times 4 \mu\text{m}$ .

*Synaptic devices fabrication:* The synaptic devices and lateral inhibition array used in the system are a 1T1R array with Pd/HfO<sub>2</sub>/Ta structure offered by the University of Massachusetts. The front-end and part of the back-end process for the transistor array were implemented in a commercial fab. Before fabricating the RS devices, argon plasma treatment was performed to remove the native metal oxide layer to make a good connection between the fab metal layers and the memristors. Then Ta/Pd (5/60 nm) bottom electrodes were deposited by sputtering and patterned by lift-off. The 10 nm HfO<sub>2</sub> switching layer was deposited by atomic layer deposition at 250°C. The patterning of the switching layer was operated by photolithography and reactive ion etching. At last, the top electrodes of 50 nm Ta were sputtered and lifted off.

*Measurement method:* In the electrical experiment, the electrical characteristics evaluation experiments of a single Ti/Au/SiO<sub>2</sub>:Ag/Ag/Au device are performed on an Agilent B1500A. During the pulse measurement, an external transistor (BS170) was connected to the TS device by a transfer box, and a DC power source was connected to the gate of the transistor. For the neuron circuit measurement in Fig. 3, we manufactured a printed circuit board (PCB) first, as shown in Supplementary Fig. 4. The TS memristors are connected to the PCB by a chip holder. The model numbers and the supplied source voltages of the used CMOS digital chips are listed in Supplementary Table SI. A Keysight 81160A pulse generator was used as the power source to generate input signals, and a Keysight InfiniiVision MSO-X 3104T oscilloscope was performed to measure the signal evolution of different nodes. As to the system measurement, the synaptic devices

were connected by the probes, and we directly connected the neurons to the synaptic array by electrical cables. Then we used the MATLAB to control the Keysight 81160A pulse generator to generate input signals. A PicoScope 4000 series oscilloscope and an InfiniiVision MSO-X 3104T oscilloscope were performed to measure 10 channels signals simultaneously. The digital models and circuit parameters used in this work are presented in Supplementary Table I.

*Training method:* The experimental processes include two parts: the learning process and the inference process. For the learning process, due to the limited number of measurement channels (10 channels) at the same time, we trained the SNNs one by one layer. To train the first layer with the WTA learning rule, the patterns in Fig. 5a were utilized as the learning object. The white pixels in patterns are recognized as “0”, thus the inputs corresponding to these pixels are grounded. The black pixels in the patterns are recognized as “1” and mapped to 1.6 V inputs pulses (2 kHz, 250  $\mu$ s width). For getting the evolution of the synaptic devices, the synaptic devices are initialized to a medium value ( $\sim$  400  $\mu$ s). Then the input pulse number that applied on the input terminals increases gradually until a fire event is observed, as shown in Supplemental Fig. 7b. During training the second layer with supervised learning, the synaptic devices are initialized to a low value ( $\sim$  40  $\mu$ s). The shared gate of synapses of the target neuron is activated by applying a 3.0 V voltage, and other gates are inhibited by grounding. Then the input pulse number that applied on the selected input terminals increases gradually until a fire event is observed, as shown in the Supplemental Fig. 7c. The simulation for Supplementary Fig. 11 is conducted on a Matlab platform, in which the neurons have no stochasticity.

## **Supporting Information**

Supporting Information accompanies this paper at....

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## **Author contributions**

X.Z. and Q.L. designed the experiments. X.Z. carried out the electrical experiments. X.Z., J. L. and J. W. designed the hybrid neuron circuits and fabricated the PCB. X.Z. designed the LIA circuit. X.Z., R. W. and. Q. L. designed and fabricated the TS devices. T. S., C. D., Z. W, D. S, and G. X. helped with data analysis. X.Z., and Q. L. prepared the paper. Q.L. and M.L. supervised the research.

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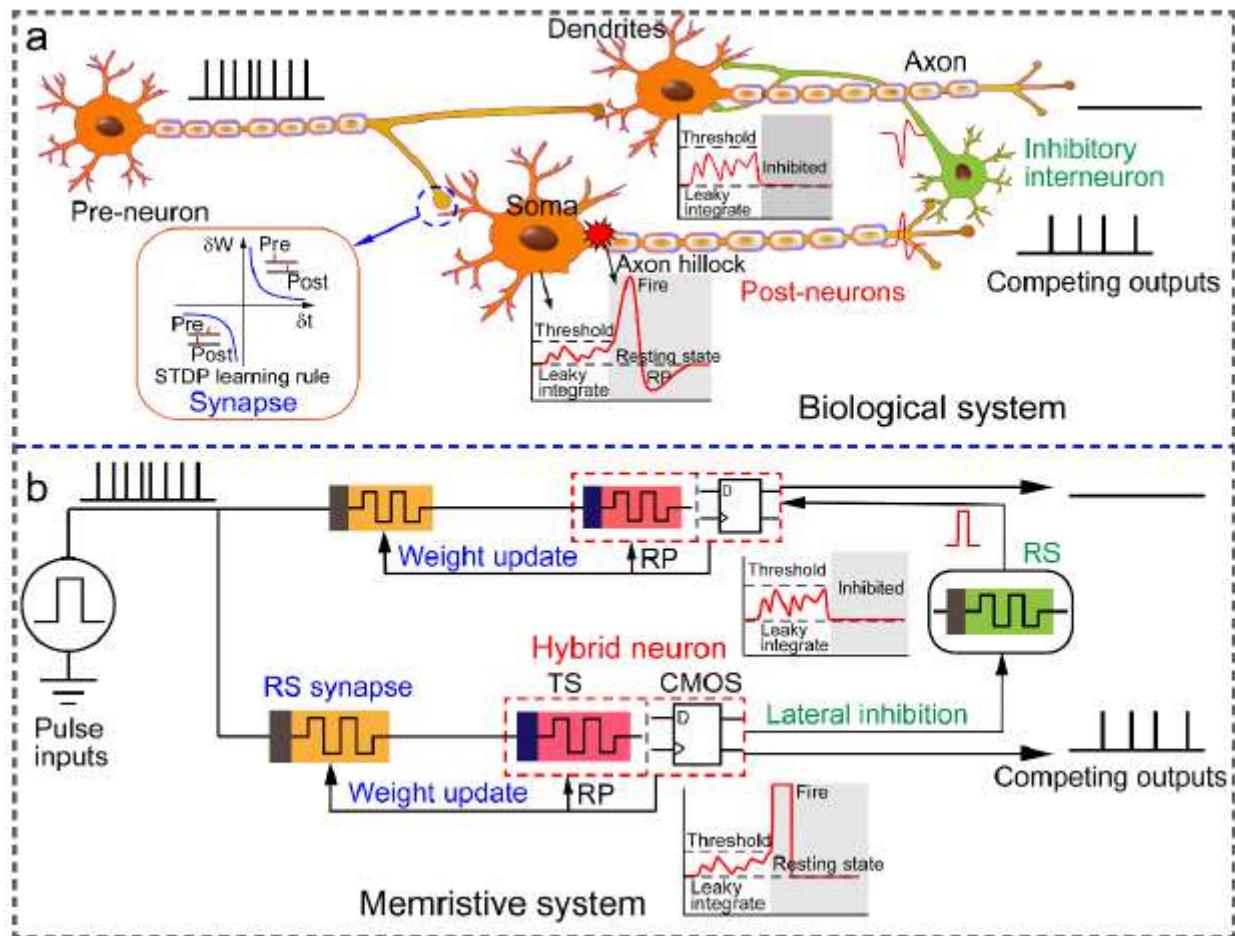
## References

1. Maass W. Networks of spiking neurons: The third generation of neural network models. *Neural Netw.* **10**, 1659-1671 (1997).
2. Roy K, Jaiswal A, Panda P. Towards spike-based machine intelligence with neuromorphic computing. *Nature* **575**, 607-617 (2019).
3. Lavalle S, *et al.* Big Data, Analytics and the Path From Insights to Value. *MIT Sloan Management Review* **52**, 21-32 (2011).
4. Merolla PA, *et al.* A million spiking-neuron integrated circuit with a scalable communication network and interface. *Science* **345**, 668-673 (2014).
5. Davies M, *et al.* Loihi: A Neuromorphic Manycore Processor with On-Chip Learning. *IEEE Micro.*, 82-99 (2018).
6. Pei J, *et al.* Towards artificial general intelligence with hybrid Tianjic chip architecture. *Nature* **572**, 106-111 (2019).
7. Indiveri G, *et al.* Neuromorphic silicon neuron circuits. *Front. Neurosci.* **5**, 73 (2011).
8. Xinyu W, Vishal S, Kehan Z, Sakkarapani B. A CMOS Spiking Neuron for Brain-Inspired Neural Networks With Resistive Synapses and *In Situ* Learning. *IEEE Transactions on Circuits and Systems —II: EXPRESS BRIEFS* **62**, (2015).
9. Ishii M, *et al.* On-Chip Trainable 1.4M 6T2R PCM Synaptic Array with 1.6K Stochastic LIF Neurons for Spiking RBM. In: *2019 Ieee International Electron Devices Meeting (IEDM)*, 14.2.1-14.2.4 (2019).
10. Wijekoon JH, Dudek P. Compact silicon neuron circuit with spiking and bursting behaviour. *Neural Netw.* **21**, 524-534 (2008).
11. Cassidy AS, *et al.* Cognitive Computing Building Block: A Versatile and Efficient Digital Neuron Model for Neurosynaptic Cores. In: *2013 International Joint Conference on Neural Networks (IJCNN)* (IEEE) (2013).
12. Wang Z, *et al.* Fully memristive neural networks for pattern classification with unsupervised learning. *Nat. Electron.* **1**, 137-145 (2018).
13. Zhang XM, *et al.* An Artificial Neuron Based on a Threshold Switching Memristor. *Ieee Electron Device Lett.* **39**, 308-311 (2018).
14. Wang Z, *et al.* Capacitive neural network with neuro-transistors. *Nat. Commun.* **9**, 3208 (2018).
15. Zhang Y, *et al.* Highly Compact Artificial Memristive Neuron with Low Energy Consumption. *Small*, e1802188 (2018).
16. Pickett MD, Medeiros-Ribeiro G, Williams RS. A scalable neuristor built with Mott memristors. *Nat. Mater.* **12**, 114-117 (2013).
17. Yi W, *et al.* Biological plausibility and stochasticity in scalable VO<sub>2</sub> active memristor neurons. *Nat. Commun.* **9**, 4661 (2018).
18. Stolar P, *et al.* A Leaky-Integrate-and-Fire Neuron Analog Realized with a Mott Insulator. *Adv. Funct. Mater.*, 1604740 (2017).
19. Lin J, *et al.* Low-voltage artificial neuron using feedback engineered insulator-to-metal-transition devices. In: *2016 Ieee International Electron Devices Meeting (IEDM)*, 34.5.1-34.5.4 (2016).
20. Zhang X, *et al.* An artificial spiking afferent nerve based on Mott memristors for neurorobotics. *Nat. Commun.* **11**, 51 (2020).

21. Mehonic A, Kenyon AJ. Emulating the Electrical Activity of the Neuron Using a Silicon Oxide RRAM Cell. *Front. Neurosci.* **10**, 57 (2016).
22. Wang JJ, *et al.* Handwritten-Digit Recognition by Hybrid Convolutional Neural Network based on HfO<sub>2</sub> Memristive Spiking-Neuron. *Sci. Rep.* **8**, 12546 (2018).
23. Huang HM, *et al.* Quasi-Hodgkin-Huxley Neurons with Leaky Integrate-and-Fire Functions Physically Realized with Memristive Devices. *Adv. Mater.* **31**, e1803849 (2019).
24. Tuma T, *et al.* Stochastic phase-change neurons. *Nat. Nanotechnol.* **11**, 693-699 (2016).
25. Pantazi A, Wozniak S, Tuma T, Eleftheriou E. All-memristive neuromorphic computing with level-tuned neurons. *Nanotechnology* **27**, 355205 (2016).
26. Torrejon J, *et al.* Neuromorphic computing with nanoscale spintronic oscillators. *Nature* **547**, 428-431 (2017).
27. Sengupta A, *et al.* Magnetic Tunnel Junction Mimics Stochastic Cortical Spiking Neurons. *Sci. Rep.* **6**, 30039 (2016).
28. Wu MH, *et al.* Extremely Compact Integrate-and-Fire STT-MRAM Neuron: A Pathway toward All-Spin Artificial Deep Neural Network. *In: 2019 Symposium on VLSI Circuits (VLSI)*, T34-T35, Ieee (2019).
29. Mulaosmanovic H, *et al.* Mimicking biological neurons with a nanoscale ferroelectric transistor. *Nanoscale* **10**, 21755-21763 (2018).
30. Chen C, *et al.* Bio-Inspired Neurons Based on Novel Leaky-FeFET with Ultra-Low Hardware. *In: 2019 Symposium on VLSI Circuits (VLSI)*, T136-T137, Ieee (2019).
31. Dutta S, *et al.* Biologically Plausible Ferroelectric Quasi-Leaky Integrate and Fire Neuron. *In: 2019 Symposium on VLSI Circuits (VLSI)*, T140-T141, Ieee (2019).
32. Luo J, *et al.* Capacitor-less Stochastic Leaky-FeFET Neuron of Both Excitatory and Inhibitory Connections for SNN with Reduced Hardware Cost. *In: 2018 Ieee International Electron Devices Meeting (IEDM)*. 6.4.1-6.4.4, Ieee (2019).
33. Purves D, *et al.* Neuroscience, 3rd ed. Sinauer Associates (2012).
34. Tang J, *et al.* Bridging Biological and Artificial Neural Networks with Emerging Neuromorphic Devices: Fundamentals, Progress, and Challenges. *Adv. Mater.* **31**, 1902761 (2019).
35. Urbanczik R, Senn W. Learning by the dendritic prediction of somatic spiking. *Neuron* **81**, 521-528 (2014).
36. Song S, Miller KD, Abbott LF. Competitive Hebbian learning through spike-timing-dependent synaptic plasticity. *Nat. Neurosci.* **3**, 919-926 (2000).
37. Froemke RC, Dan Y. Spike-timing-dependent synaptic modification induced by natural spike trains. *Nature* **416**, 433-438 (2002).
38. Shouval HZ, Wang SS, Wittenberg GM. Spike timing dependent plasticity: a consequence of more fundamental learning rules. *Front. Comput. Neurosci.* **4**, (2010).
39. Amari SI. Dynamics of Pattern Formation in Lateral-Inhibition Type Neural Fields. *Biol. Cybern.* **27**, 77-87 (1977).
40. Diehl PU, Cook M. Unsupervised learning of digit recognition using spike-timing-dependent plasticity. *Front. Comput. Neurosci.* **9**, 99 (2015).

41. Valov I, *et al.* Nanobatteries in redox-based resistive switches require extension of memristor theory. *Nat. Commun.* **4**, 1771 (2013).
42. Wang W, *et al.* Surface diffusion-limited lifetime of silver and copper nanofilaments in resistive switching devices. *Nat. Commun.* **10**, 81 (2019).
43. Pan F, *et al.* Recent progress in resistive random access memories: Materials, switching mechanisms, and performance. *Mat. Sci. Eng. R-Reports* **83**, 1-59 (2014).
44. Long BM, Mandal S, Livecchi J, Jha R. Effects of Mg-Doping on HfO<sub>2</sub>-Based ReRAM Device Switching Characteristics. *Ieee Electron Device Lett.* **34**, 1247-1249 (2013).
45. Mondal S, *et al.* Effect of Ti doping concentration on resistive switching behaviors of Yb<sub>2</sub>O<sub>3</sub> memory cell. *Appl. Phys. Lett.* **101**, 083506 (2012).
46. Wang Z, *et al.* Memristors with diffusive dynamics as synaptic emulators for neuromorphic computing. *Nat. Mater.* **16**, 101-108 (2016).
47. Liu Q, *et al.* Real-Time Observation on Dynamic Growth/Dissolution of Conductive Filaments in Oxide-Electrolyte-Based ReRAM. *Adv. Mater.* **24**, 1844-1849 (2012).
48. Midya R, *et al.* Anatomy of Ag/Hafnia-Based Selectors with 10<sup>10</sup> Nonlinearity. *Adv. Mater.* **29**, 1604457 (2017).
49. Zhao X, *et al.* Breaking the Current-Retention Dilemma in Cation-Based Resistive Switching Devices Utilizing Graphene with Controlled Defects. *Adv. Mater.* **30**, 1705193 (2018).
50. Sun H, *et al.* Direct Observation of Conversion Between Threshold Switching and Memory Switching Induced by Conductive Filament Morphology. *Adv. Funct. Mater.* **24**, 5679-5686 (2014).
51. Yang Y, *et al.* Electrochemical dynamics of nanoscale metallic inclusions in dielectrics. *Nat. Commun.* **5**, 4232 (2014).
52. Maass W. Noise as a Resource for Computation and Learning in Networks of Spiking Neurons. *Proceedings of the Ieee* **102**, 860-880 (2014).
53. Caporale N, Dan Y. Spike timing-dependent plasticity: a Hebbian learning rule. *Annu. Rev. Neurosci.* **31**, 25-46 (2008).
54. Alibart F, Zamanidoost E, Strukov DB. Pattern classification by memristive crossbar circuits using ex situ and in situ training. *Nat. Commun.* **4**, 2072 (2013).
55. Ge N, *et al.* An efficient analog Hamming distance comparator realized with a unipolar memristor array: a showcase of physical computing. *Sci. Rep.* **7**, 40135 (2017).
56. Serb A, *et al.* Unsupervised learning in probabilistic neural networks with multi-state metal-oxide memristive synapses. *Nat. Commun.* **7**, 12611 (2016).
57. Jiang H, *et al.* Sub-10 nm Ta Channel Responsible for Superior Performance of a HfO<sub>2</sub> Memristor. *Sci. Rep.* **6**, 28525 (2016).
58. Srinivasan G, Sengupta A, Roy K. Magnetic Tunnel Junction Based Long-Term Short-Term Stochastic Synapse for a Spiking Neural Network with On-Chip STDP Learning. *Sci. Rep.* **6**, 29545 (2016).

# Figures



Biological neural system vs. memristive system. a, Schematic of a biological neural system. The post neuron receives input signals from the pre neurons through the connected synapses and changes its membrane potential. An action potential generates at the axon hillock once the membrane potential surpasses a threshold value. The fired neuron could inhibit neighboring neurons through interneurons. The relative timing of pre and postsynaptic spikes could *in situ* modify the synaptic strength, i.e., the spike timing dependent plasticity (STDP) learning rule. b, Frame diagram of the hybrid neuron driven memristive system. The resistive switching (RS) memristor serves as synapses and lateral inhibition connection. The hybrid neuron contains a threshold switching (TS) memristor and simple digital units (CMOS), in which the TS devices perform the leaky integrate-and-fire neuron function, and the digital units generate active spikes, refractory period (RP) signals, in situ weight updating signals, and lateral inhibition signals.

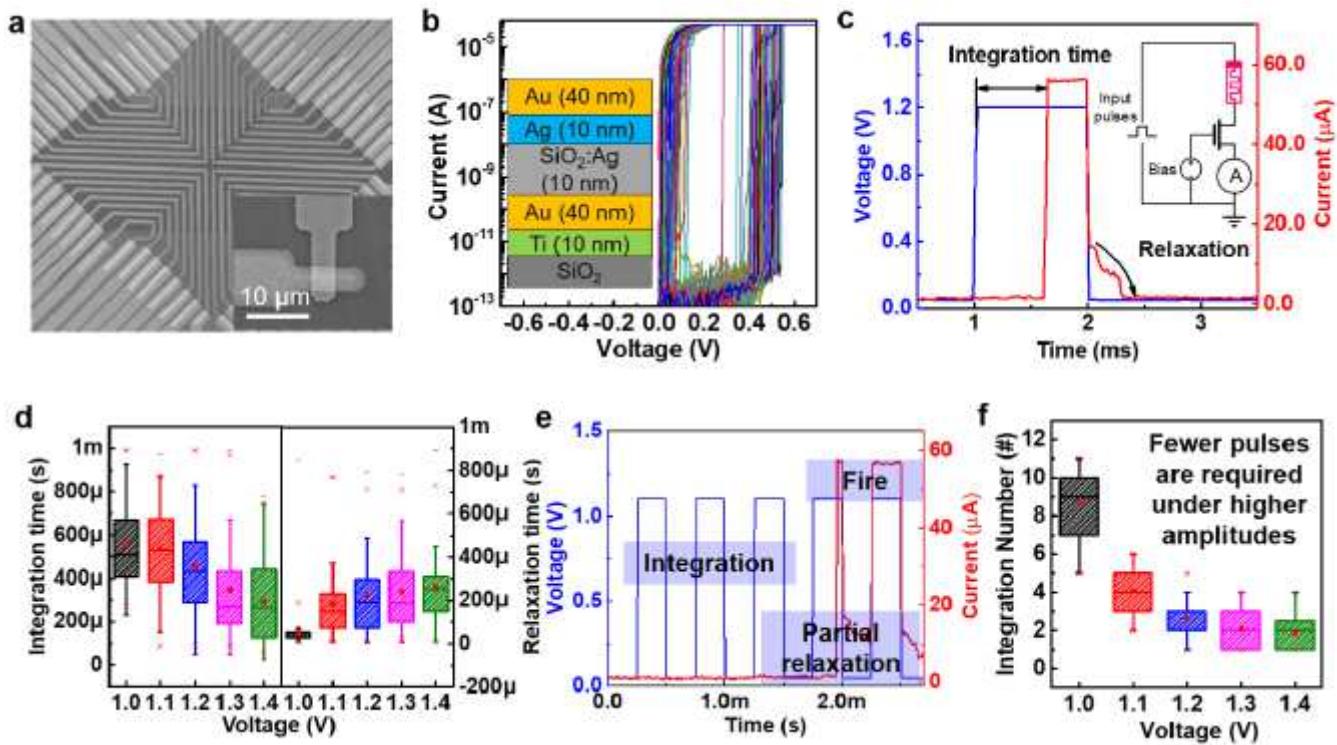
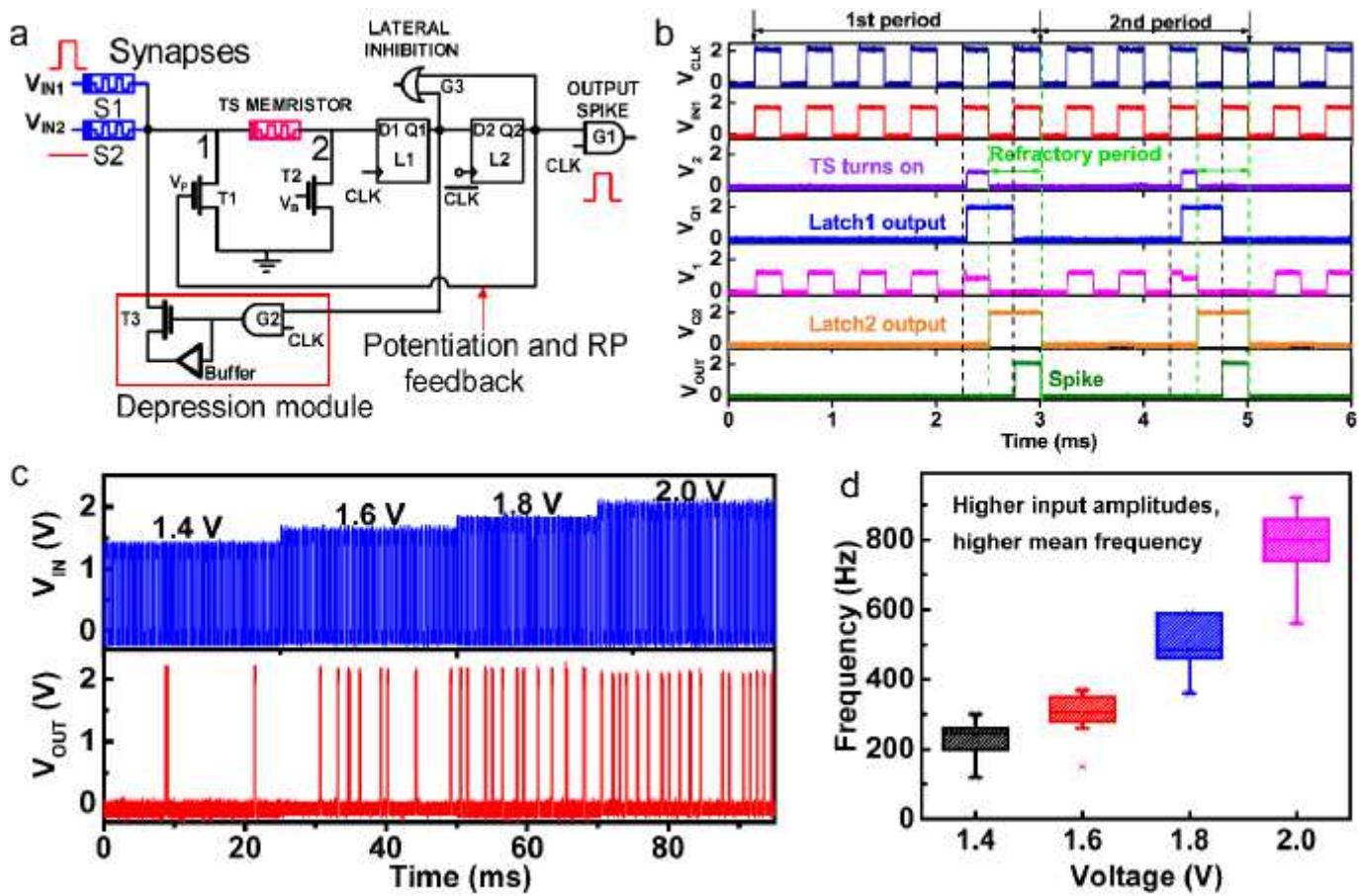


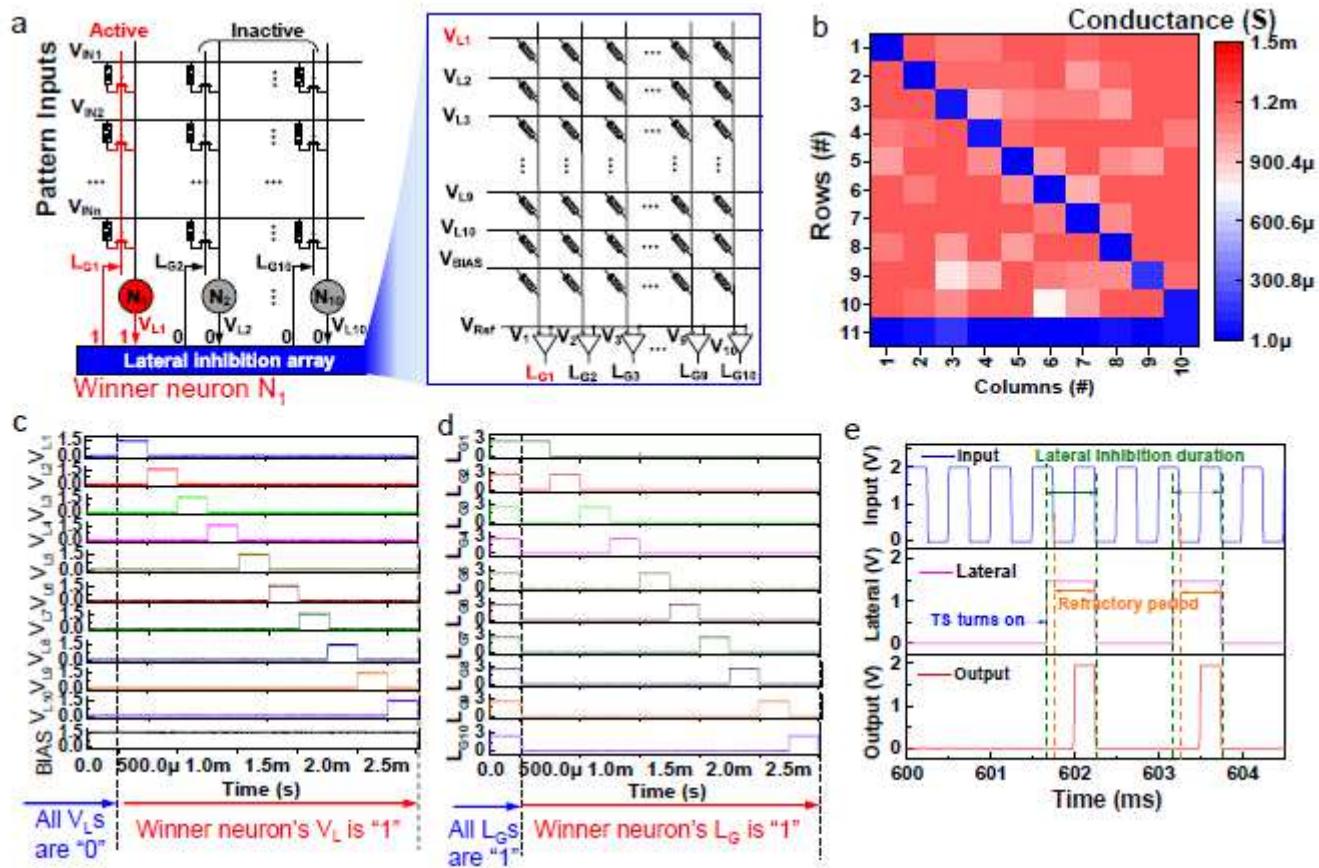
Figure 2

Characteristics of the TS device. a, Scanning electron microscope (SEM) image of the TS array, includes 32 discrete devices ( $4 \mu\text{m} \times 4 \mu\text{m}$ ). The inset shows a zoom in image of a single device. b, 100 typical I-V switching curves of the device under positive voltage sweeps. Inset: the device structure used in this work. c, The current response of the device under a 1.2 V pulse (1 ms width) followed by a 0.05 V monitor voltage. Inset: the schematic of the testing circuit. d, The statistical data of the integration time and relaxation time as a function of the pulse amplitudes under 1 ms pulse width. e, The integration behavior of the TS device under multiple pulses (1.1 V, 250  $\mu\text{s}$  width, 250  $\mu\text{s}$  interval time) with 0.05 V monitor voltage between pulses. After the first fire, the device cannot completely return to its initial HRS due to the interval time is not enough for finishing a complete relaxation, and thus induces a sub-threshold firing. f, The statistical data of the required pulse number for the first firing under different pulse voltages (with 250  $\mu\text{s}$  width and interval time). Fewer integration pulses are required under higher voltages.



**Figure 3**

Hybrid memristor CMOS neuron circuit and characteristics. a, Schematic of the hybrid neuron circuit. A single TS device serves as the gated membrane for performing the leaky integrate-and-fire neuron function. Two D-type latches (L1 and L2) and a AND gate (G1) are used to shape the fire signal to a fixed spike signal. The output signal from L2 is applied to the gate terminal of T1 to make the node 1 virtual ground, which is for performing synaptic potentiation operation and supplying a refractory period (RP). A buffer, a transistor T3, and a AND gate (G2) construct the depression module. An OR gate G3 that receives inputs from L1 and L2 serves as the lateral inhibition output. b, The sequence diagram of the output values on five key nodes under continuous input pulses (1.8 V, 2 kHz, 250  $\mu$ s width) within two continuous firing cycles when disabling the depression feedback circuit. c, The continuous spiking behavior under different input voltages on  $V_{IN1}$ . d, The statistical results of spiking frequencies as the function of the input pulses amplitudes, the frequency increases with increasing the input pulse amplitudes.



**Figure 4**

Lateral inhibition circuits for the winner take all learning rule. a, Schematic of the lateral inhibition array (LIA) circuit for ten neurons, which contains a resistive switching (RS) array and comparators. The outputs of LIA are applied to the shared gates of 1T1R synapses to implement lateral inhibition. The lateral inhibition signals ( $V_{L1}$ – $V_{L10}$ ) from neurons serve as the inputs of the LIA, and the outputs of the comparators are applied to the shared gates of 1T1R synapses.  $V_{BIAS}$ : 1.5 V,  $V_{Ref}$ : 50 mV. b, The pre programmed weight conductance of the memristor array used in the LIA circuit for ten neurons. c, Two input conditions of the LIA while performing lateral inhibition operation, the input signals are the neurons' lateral inhibition signals. d, The corresponding outputs of all the LIA ( $LG1$ – $LG10$ ) when two conditions in c serve as the inputs of the LIA. c & d, The Y axis unit is volt (V). e, The moment when the neuron outputs lateral inhibition signal. Two firing cycles are presented.

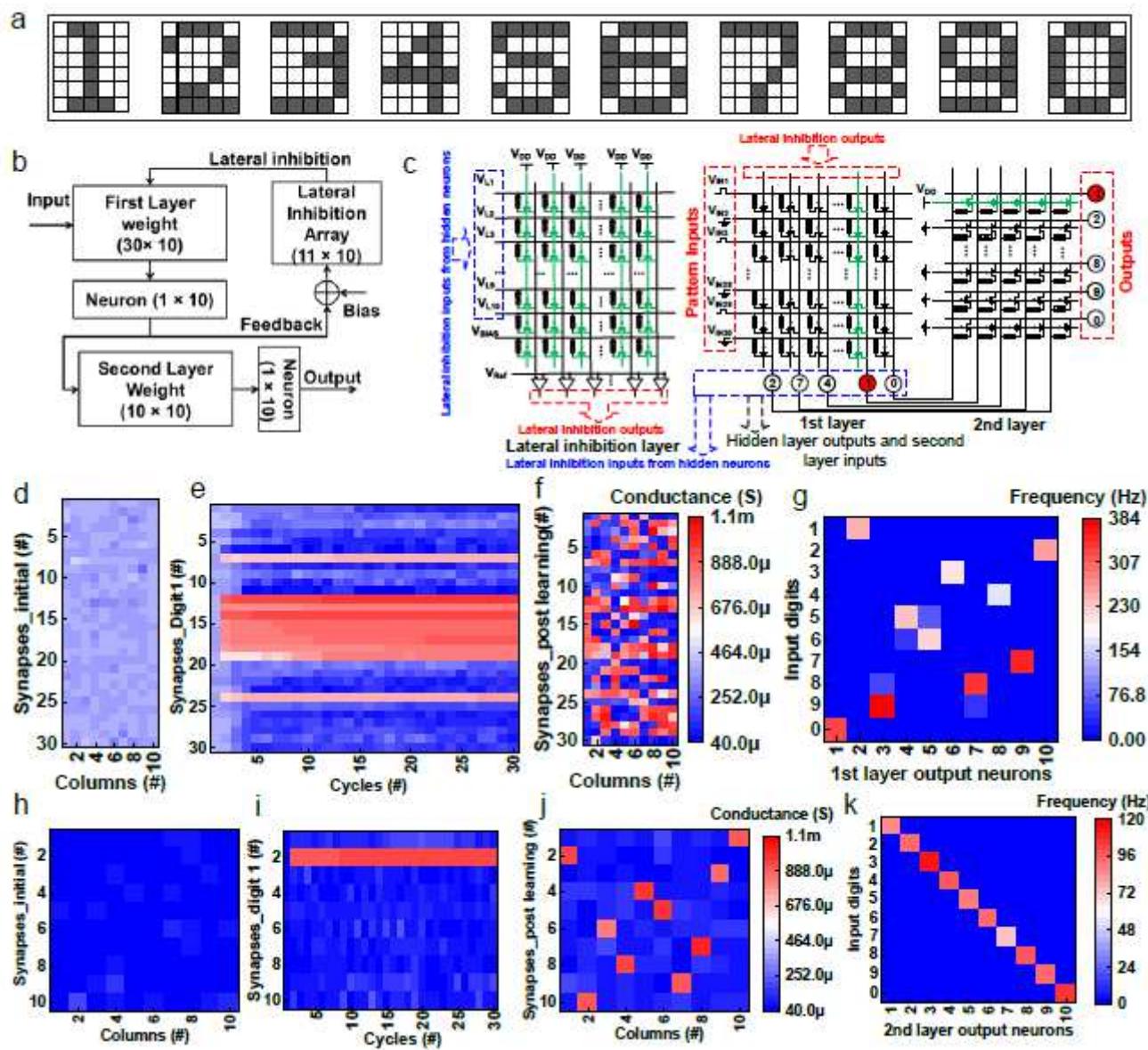


Figure 5

Fully hardware multilayer SNNs. a, The digital patterns used for learning, every pattern includes 30 pixels ( $6 \times 5$ ). b, Frame diagram of the constructed SNNs ( $30 \times 10 \times 10$ ). The first layer is constructed with a  $30 \times 10$  array and the second layer is with a  $10 \times 10$  array. A  $11 \times 10$  array with a bias input is used for lateral inhibition of the first layer output neurons. c, The detailed circuit schematic of the whole system. d & h, The initialized weight map of the first layer and second layer before learning. e & i, The evolution of the synaptic weights of the neuron "1" after 30 firing events when the digit "1" as input pattern. f & j, The final weight map of the first and second layers after learning, respectively. Clear weight distribution is observed. d, e, f, h, i & j, Presented under the same color bar. g & k, The firing rates of the output neurons in first and second layers under different input digits with noise pixels during inference processes.

## Supplementary Files

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