

1. Supplementary Methods

1.1 Photolithography

The grown gallium nitride (GaN) wafers on sapphire substrates are placed in a cleaning basket and sequentially cleaned with acetone and isopropyl alcohol to remove surface impurities, which are then confirmed to be absent using an optical microscope. Subsequently, the clean GaN/sapphire substrates are spin-coated with photoresist, followed by the standard Photolithography process to transfer the pattern from the mask onto the GaN substrate material. The procedure concludes with exposure and development treatments.

1.2 Mesa Etching

The processed GaN substrates are introduced into an ion beam etching system (IBE) to perform the etching of pixel mesas. Following the etching process, the photoresist on the GaN wafers is removed with acetone, and the surfaces are thoroughly cleaned. The optical microscopy platform is utilized to confirm the absence of any residues post-cleaning. This completes the etching of the pixel array mesas on the GaN substrate material.

1.3 Anode Deposition

The etched chips with pixel mesas undergo a second round of photolithography to protect the etched pixels on their surfaces. After standard photolithographic processing, a sequential deposition of metallic electrodes is performed using magnetron sputtering, starting with a ITO/Ti/Al/Ni/Cr/Pt/Au(100/50/350/100/500/500/5000Å) stack.

1.4 Passivation Of SiO₂

The chips are immersed in acetone to soften the photoresist, which is subsequently removed with an acetone gun. A layer of silicon dioxide is then deposited as a passivation layer.

1.5 Etching Ohmic Pore

Ohmic contacts on the chip are created through a process involving photolithography and IBE technology.

1.6 Connected to the IC

Lastly, a layer of ITO is grown on top as a conductive electrode after the ohmic contact holes have been opened. Subsequently, the chip was connected to the IC circuit by using the flip-chip bonder.

2. Supplementary figures

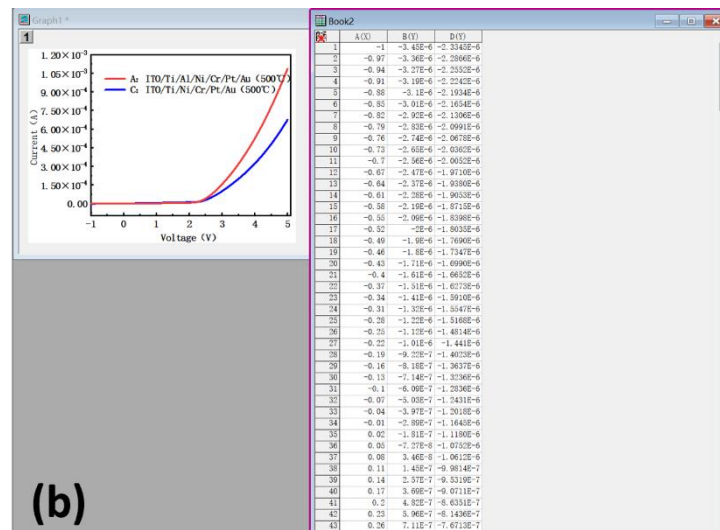
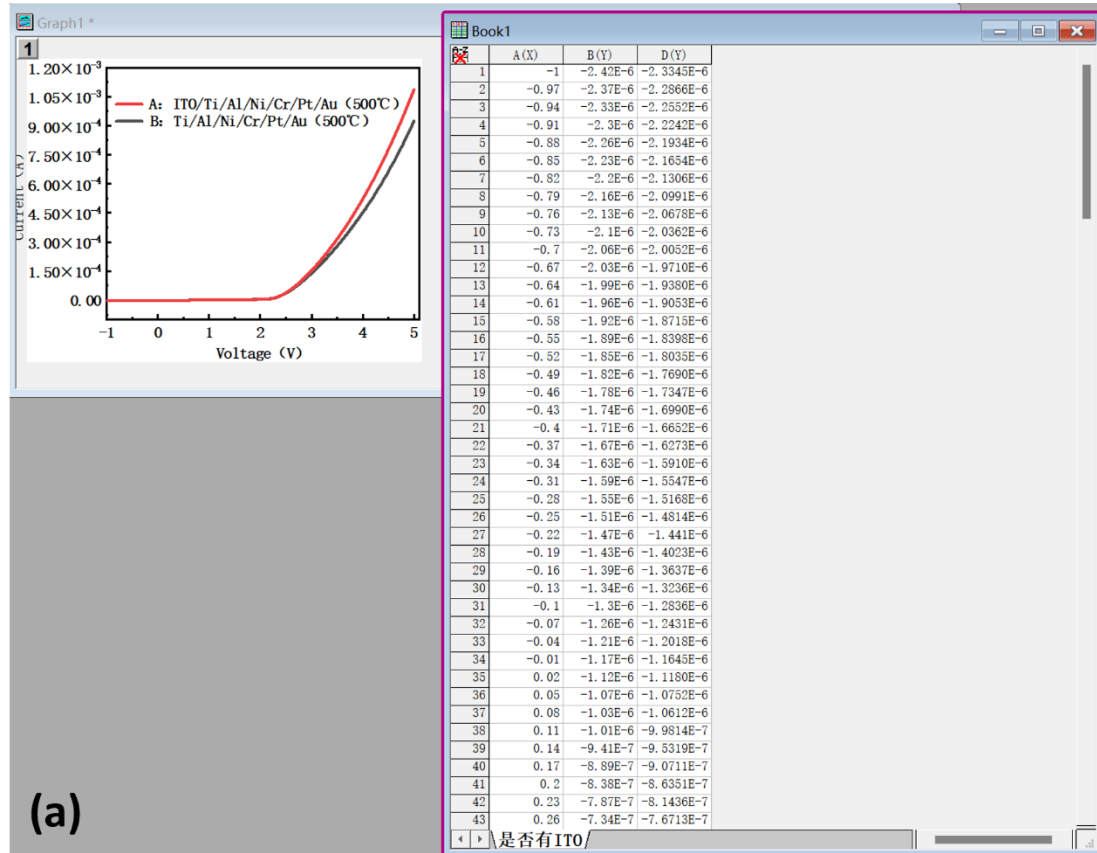


Figure 1s. The current-voltage characteristics of the devices. **(a)** The current-voltage curves of device A and device B. **(b)** The current-voltage curves of sample A and sample C.

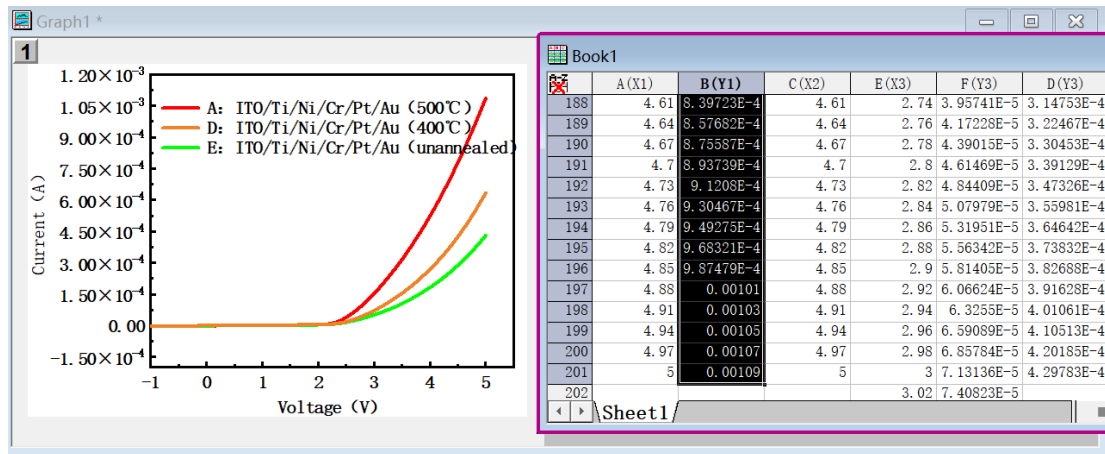
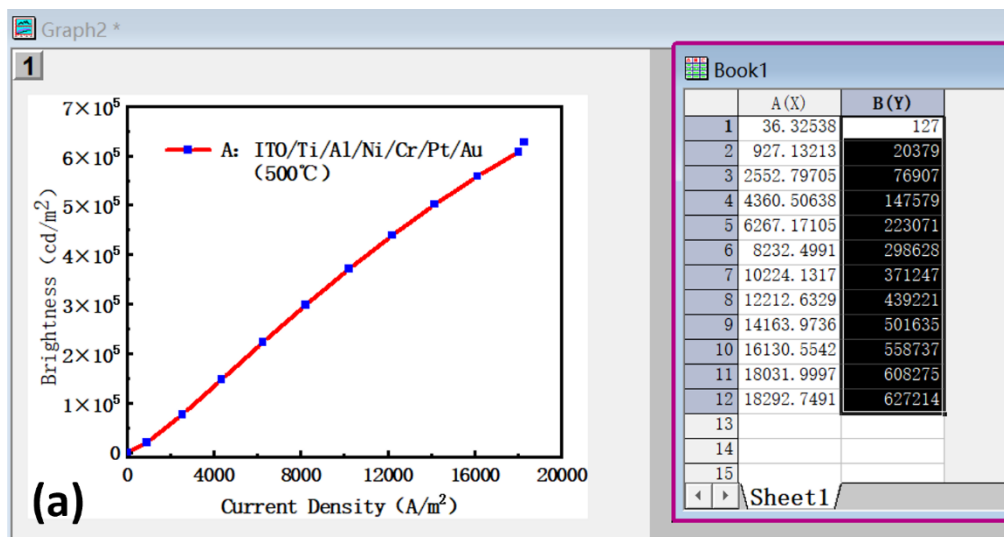
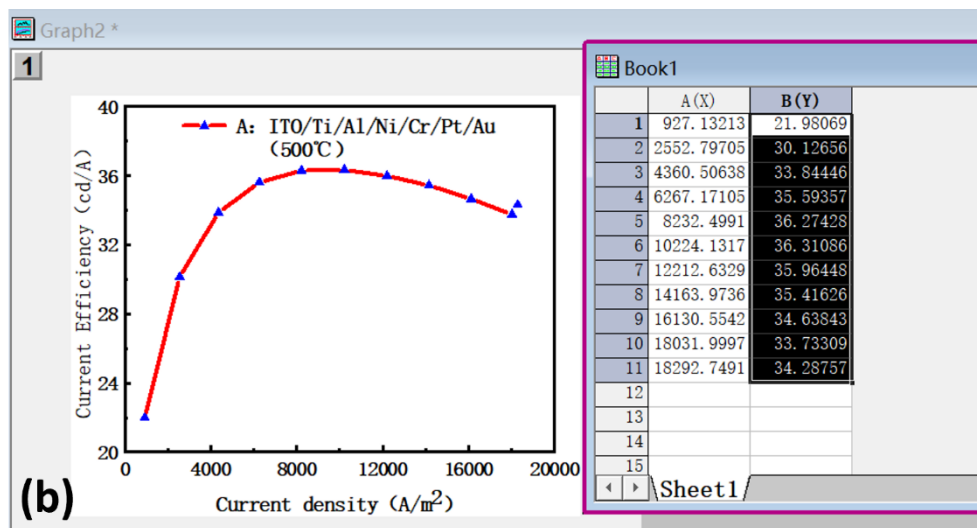


Figure 2s. The electrical properties of the devices with different annealing temperatures.



(a)



(b)

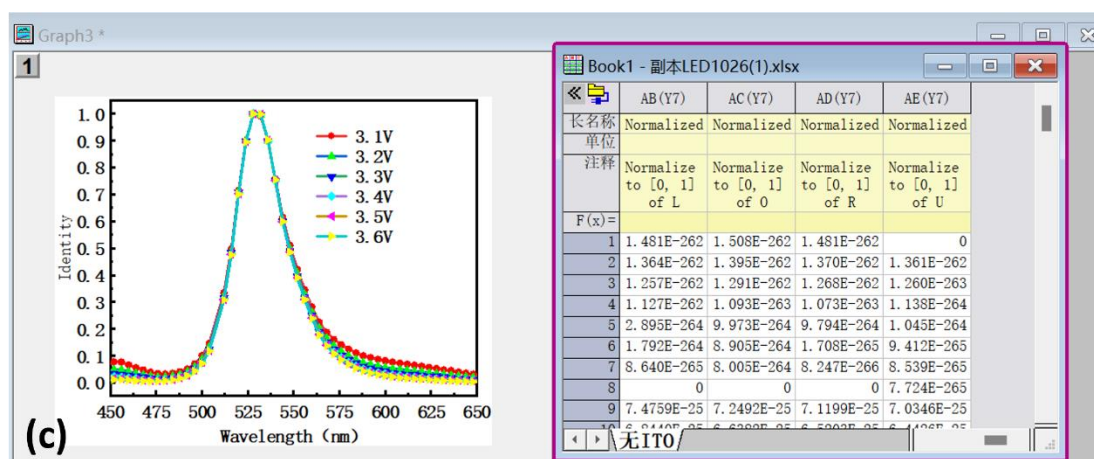


Figure 3s. The optical properties of the device. **(a)** the light brightness-voltage graph of device A. **(b)** the efficiency-current density graph of device A. **(c)** The normalized emission wavelength-voltage graph of the device A