Variability and High Temperature Reliability of Graphene Field-Effect Transistors with Thin Epitaxial CaF_2 Insulators (Supporting Information)

Yury Yu. Illarionov,[*,†,‡,¶] *Theresia Knobloch,*[‡] *Burkay Uzlu,*[§] *Alexander G. Banshchikov,*[¶] *Iliya A. Ivanov,*[¶] *Viktor Sverdlov,*[‡] *Martin Otto,*[§] *Stefanie Linda Stoll,*[§] *Mikhail I. Vexler,*[¶] *Michael Waltl,*[‡] *Zhenxing Wang,*[§] *Bibhas Manna,*[‡] *Daniel Neumaier,*[§,‖] *Max Lemme,*[§,⊥,¶] *Nikolai S. Sokolov,*[¶] *and Tibor Grasser*[*,‡]

†*Southern University of Science and Technology, 1088 Xueyuan Blvd, 518055 Shenzhen, China*

‡*Institute for Microelectronics (TU Wien), Gusshausstrasse 27–29, 1040 Vienna, Austria*

¶*Ioffe Institute, Polytechnicheskaya 26, 194021 St-Petersburg, Russia*

§*AMO GmbH, Otto-Blumenthal-Strasse 25, 52074 Aachen, Germany*

‖*Bergische Universitat Wuppertal, Gaussstrasse 20, 42119 Wuppertal, Germany*

⊥*RWTH Aachen University, Otto-Blumenthal-Strasse 25, 52074 Aachen, Germany*

E-mail: illarionov@sustech.edu.cn; grasser@iue.tuwien.ac.at

Structural characterization of our GFETs with CaF_2

In Fig.S1a we show the atomic force microscopy (AFM) image obtained at the edge of the metal stack after lift off and the corresponding height profile. No corner edge is visible,

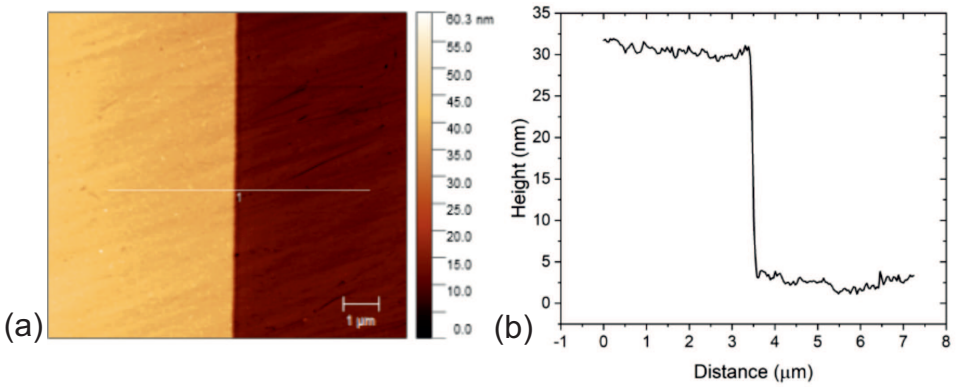

Figure S1: (a) AFM image obtained at the edge of the metal stack after lift off and the height profile extracted along the marked line (b). No lift-off corner edge is observed.

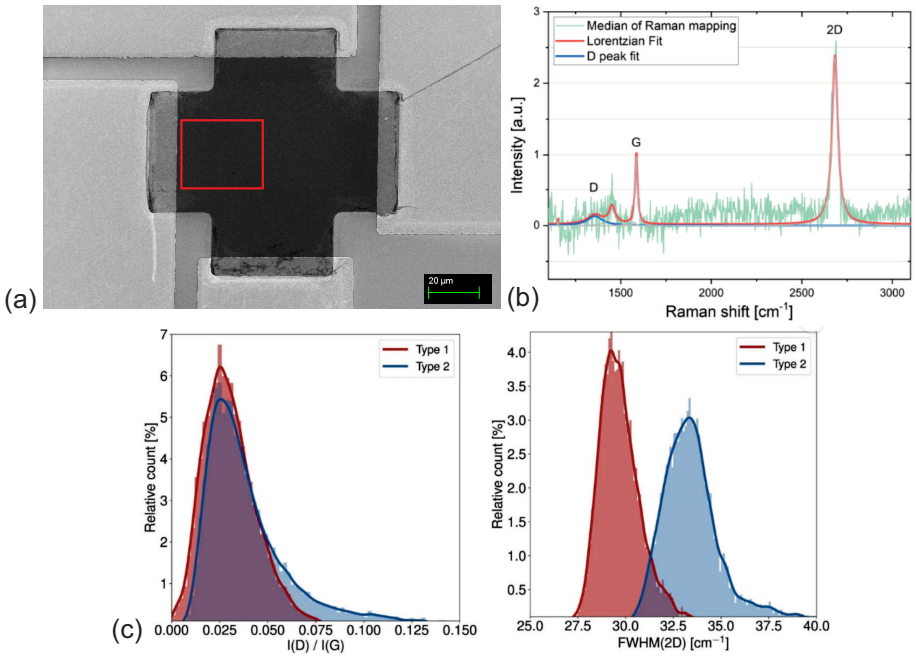

Figure S2: (a) SEM image of our GFET with an 80/160 L/W ratio. The red box indicates the region for the 36 measurement points of the Raman spectrum. (b) The median Raman spectrum represents measurements from 36 points on the GFET (green). A Lorentzian fit of the Raman spectrum is depicted in red, while the fit for the D peak is illustrated in blue. The FWHM of the 2D peak was measured as 37 cm^{-1}, and the I(D)/I(G) ratio was determined to be 0.112. (c) I(D)/I(G) ratio (left) and FWHM (right) of two different graphene grades on oxide substrates studied in our previous work[1].

which confirms the high quality of our metallization and lift-off processes.

In Fig.S2a we show the scanning electron microscopy (SEM) image of the channel of our GFET with CaF_2 and in Fig.S2b the Raman spectrum obtained using 36 measurement points taken inside the red box. We can see that there is no prominent D peak, which confirms relatively good quality of our transferred graphene. However, we can also see that median full width at half maximum (FWHM) of the 2D peak measured as $37\,\mathrm{cm}^{-1}$ and its I(D)/I(G) of 0.112 are larger as compared to the same values obtained for two different grades of graphene studied in our previous work.[1] This could indicate that some strain was introduced into the transferred graphene film by chemically inert CaF_2 surface.

Device-to-device variability

In Fig.S3 we show the full set of the I_D-V_G characteristics measured for 33 GFETs with $80\,\mu\mathrm{m} \times 50\,\mu\mathrm{m}$ channel dimensions. While in overall a sizable device-to device variability is observed, some devices have nearly identical characteristics. Thus, by further optimizing the device fabrication techniques in future it may be possible to considerably suppress this variability, which may be caused by grain boundaries in CVD-grown graphene, as well as by not well adjusted contact processing or local inhomogeneities in the CaF_2 layers.

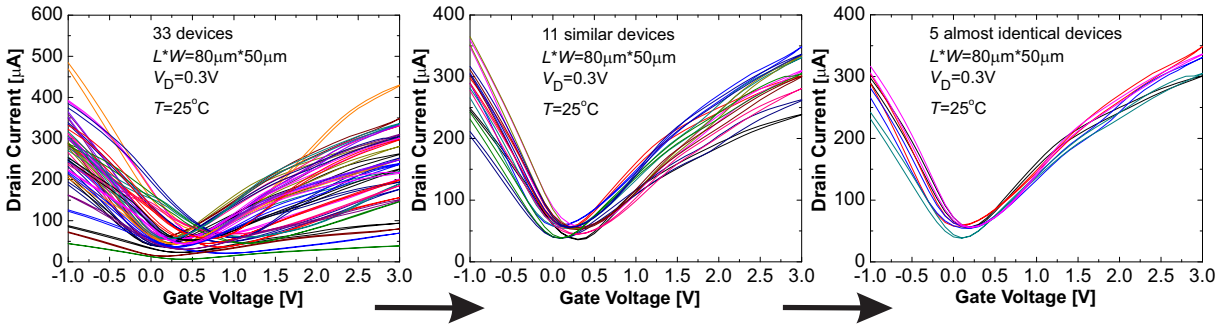

Figure S3: I_D-V_G characteristics of our 33 GFETs from Batch#1 with $80\,\mu\mathrm{m} \times 50\,\mu\mathrm{m}$ channel dimensions. Among these devices, 11 look very similar and 5 nearly identical.

In Fig.S4 we show contact resistance vs. V_G extracted for three GFETs using the four-

probe method. Some variability is present even between nominally identical devices with the same channel dimensions. This confirms that the device-to-device variability visible in Fig.S3, in particular in I_{D} values, can be also attributed to imperfections introduced during contact processing.

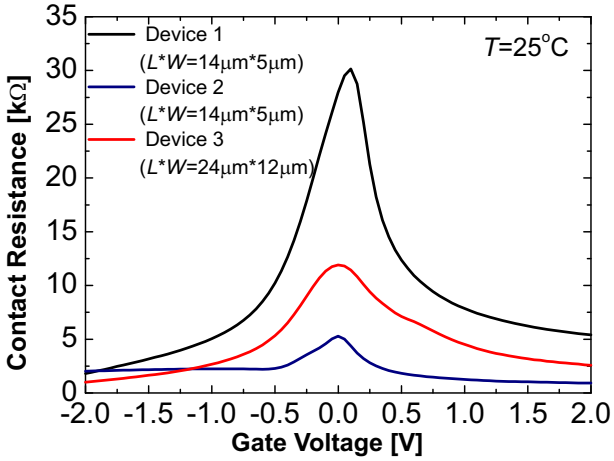

Figure S4: Contact resistance measured for three GFETs. Considerable variability is observed.

In Fig.S5a we show the I_{D}-V_{G} characteristics of our Batch#2 GFETs fabricated using new highly-doped Si substrates. Due to initially excessive p-doping with very positive V_{Dirac} above 3 V these devices had to be subjected to initial annealing for 2 days at 100°C and subsequently for 5 hours at 175°C before the first measurement round. Despite some variability among 82 devices, we can select 14 very similar ones. At the same time, variability in V_{Dirac} among all measured devices is rather small (Fig.S5b), even though the shape of the I_{D}-V_{G} characteristics and drain current values may be different.

In Fig.S6a we show the I_{D}-V_{G} measured for our 13 reference GFETs with 36 nm Al_2O_3 insulators. In contrast to GFETs with CaF_2, these devices suffer from sizable variability of V_{Dirac} (Fig.S6b) with simultaneously similar values of the drain current.

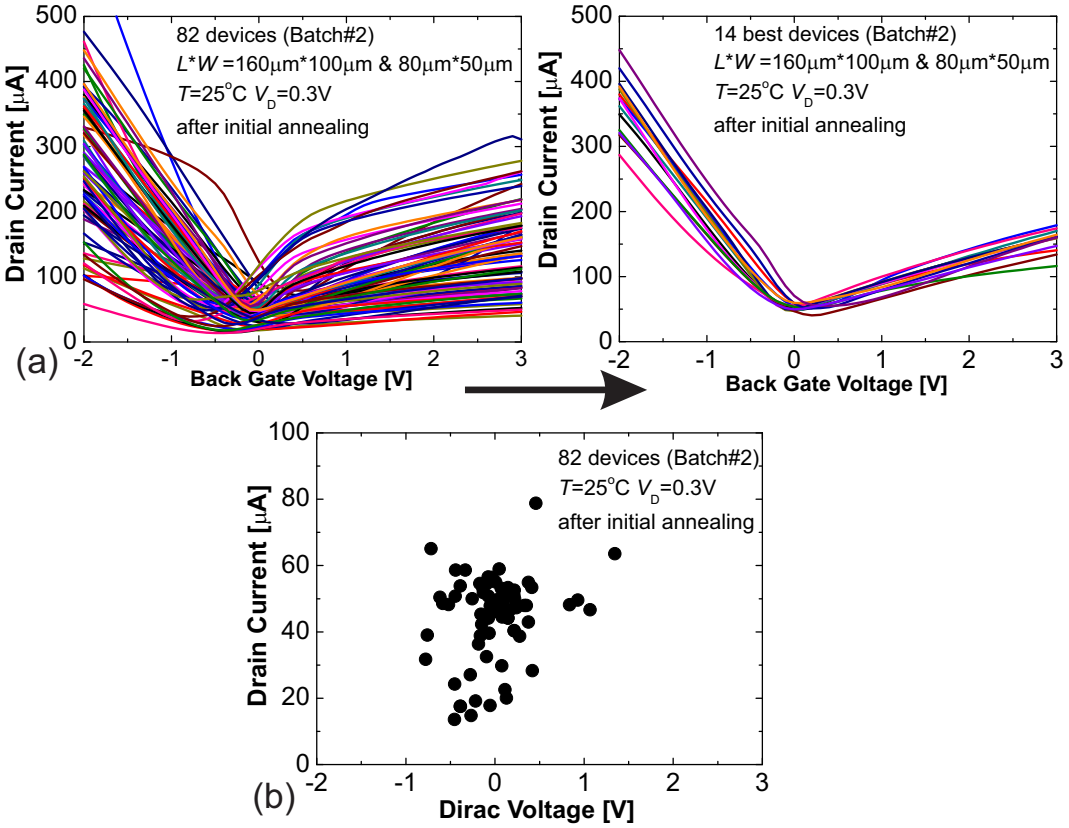

Figure S5: (a) I_{D}-V_{G} characteristics of our 82 GFETs from Batch#2 with 160 μm $\times$100 μm and 80 μm $\times$50 μm channel dimensions. Among these devices, 14 look nearly identical. (b) Distribution of I_{Dirac} vs. V_{Dirac} for all 82 devices.

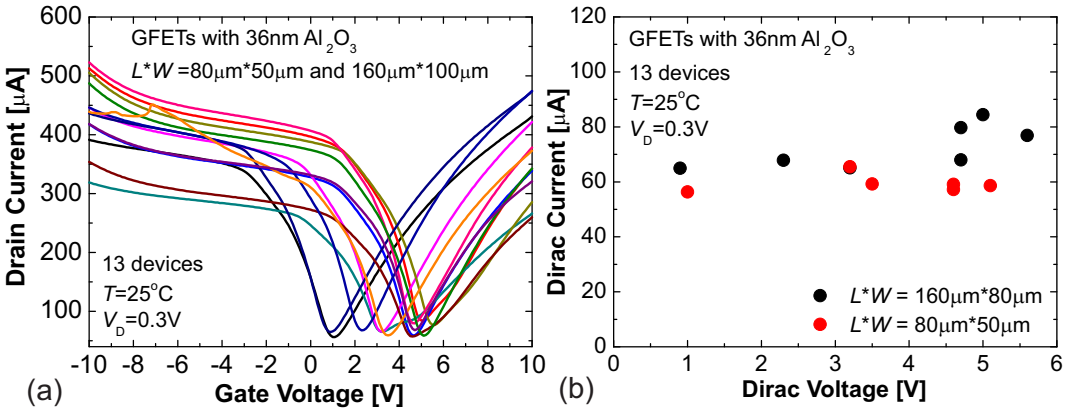

Figure S6: (a) I_{D}-V_{G} characteristics of our 13 GFETs with 36 nm Al_2O_3 insulators. (b) The corresponding distribution of I_{Dirac} vs. V_{Dirac}.

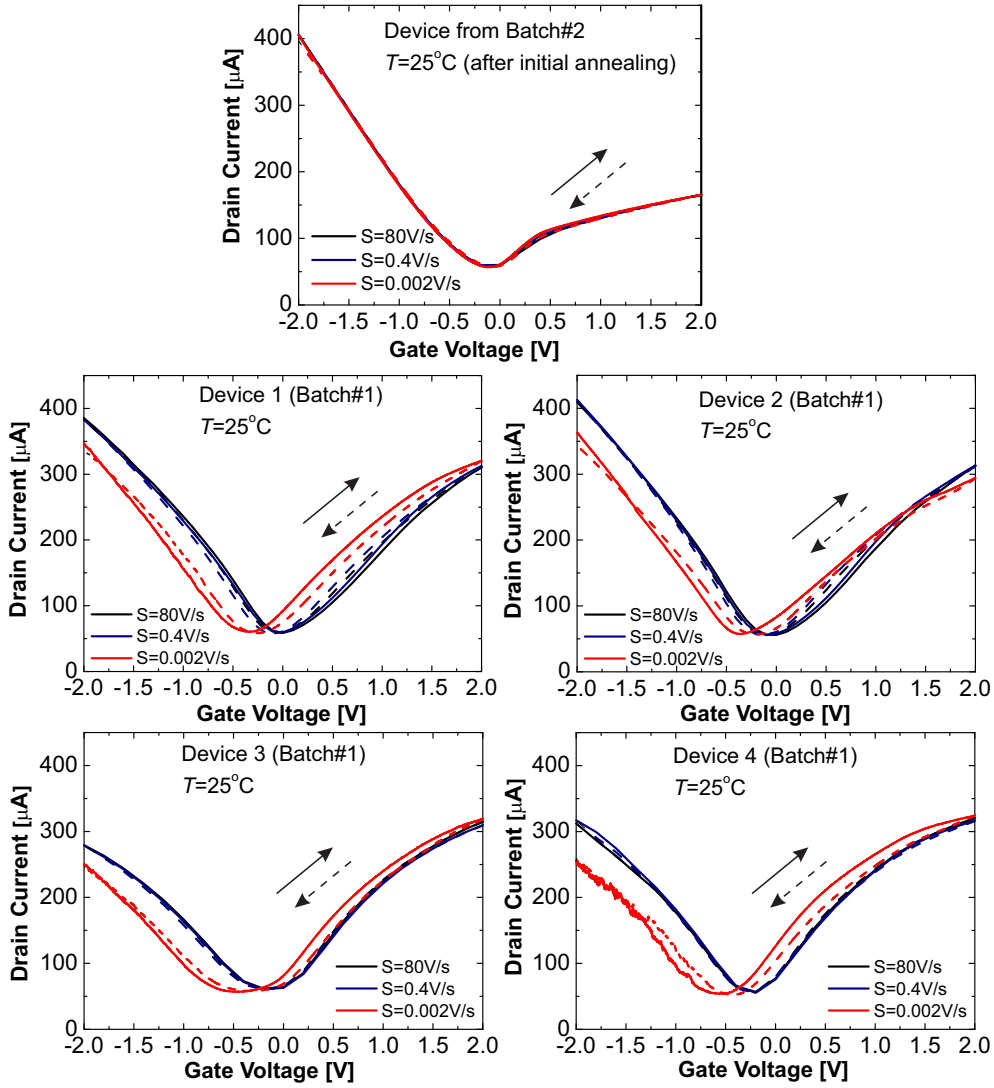

Figure S7: I_{D}-V_{G} characteristics of one GFET from Batch#2 and four typical GFETs from Batch#1 with 80 μm $\times$50 μm channel dimensions measured using different sweep rates.

Hysteresis dynamics

In Fig.S7 we show the I_{D}-V_{G} characteristics of one GFET from Batch#2 and four typical GFETs from Batch#1 with 80 μm $\times$50 μm channel dimensions which are studied in Fig.4 in the manuscript. While the measurements have been performed using different sweep rates, it is common that for our GFETs from Batch#1 at slow sweeps clockwise hysteresis appears together with a negative drift of V_{Dirac}. The clockwise hysteresis is likely caused by relatively

fast insulator defects in CaF_2 which are close to the interface with graphene. At the same time, negative drifts of V_{Dirac} at slow sweeps are due to slower defects in CaF_2. Remarkably, the device from Batch#2 has the smallest hysteresis and the less pronounced negative drift of V_{Dirac} as compared to all typical devices.

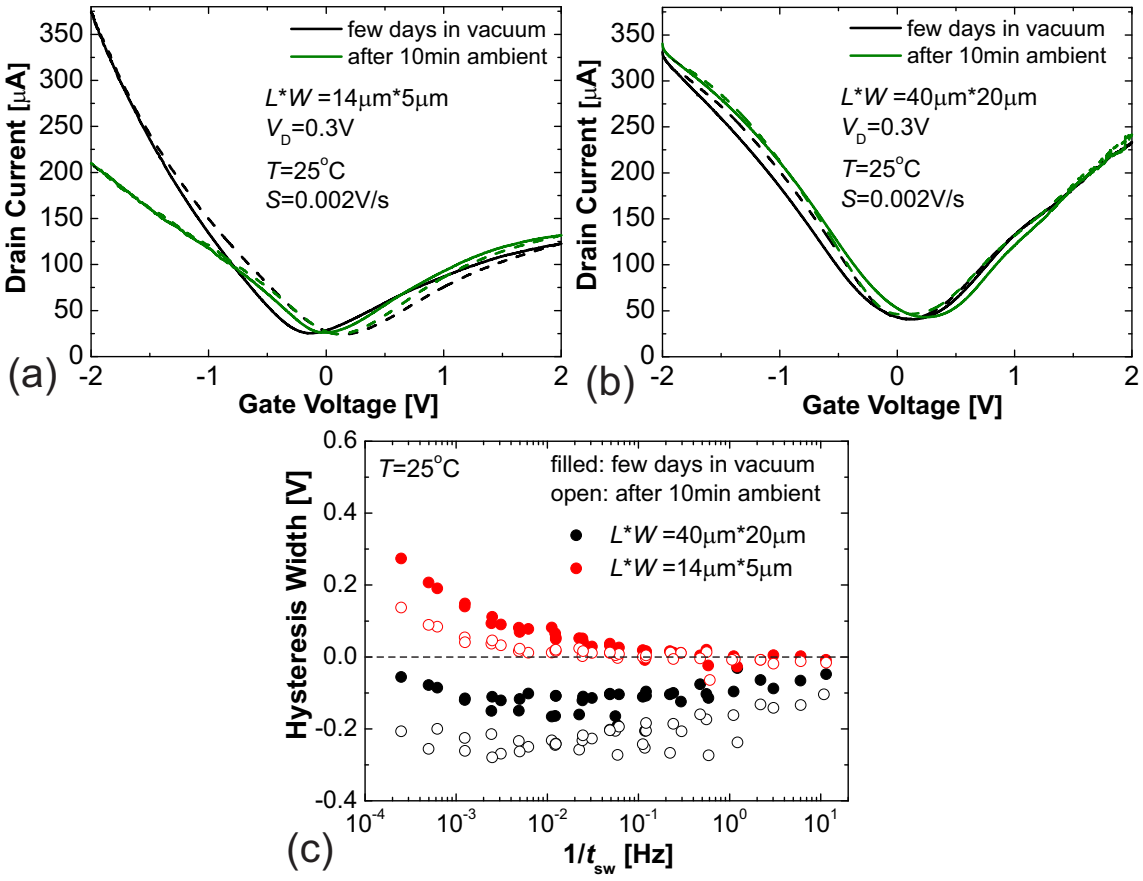

Figure S8: Slow sweep I_{D}-V_{G} characteristics of GFETs with clockwise (a) and counterclockwise (b) hysteresis measured in a vacuum before and after 10 minutes ambient exposure. (c) The corresponding ΔV_{H} vs. $1/t_{\mathrm{sw}}$ dependences.

In Fig.S8a,b we show the I_{D}-V_{G} characteristics of two GFETs measured at slow sweeps, one of which exhibits a clockwise and another one a counterclockwise hysteresis. The measurements have been performed in a vacuum first after few days of vacuum treatment at room temperature and then following 10 minutes of ambient exposure. As shown in Fig.S8c, the corresponding ΔV_{H} vs. $1/t_{\mathrm{sw}}$ dependences exhibit some trends towards more counterclockwise hysteresis following the ambient exposure. This suggests that this type of hysteresis

can be attributed to various mechanisms associated with the impact of the ambient, such as adsorbates or penetration of oxygen through imperfections in CaF_2.

Hysteresis in reference GFETs with 3D oxides

In Fig.S9a we compare slow sweep I_D-V_G characteristics measured for our reference back-gated GFETs with 90 nm SiO_2 and 36 nm Al_2O_3 insulators and observe a standard clockwise hysteresis in both cases. This means that due to a large density of oxide traps in SiO_2 and Al_2O_3, charge trapping by these defects is the dominant reason for the hysteresis. In contrast to CaF_2 GFETs, a counterclockwise hysteresis cannot be observed due to the much larger equivalent oxide thickness (EOT) of the layers of 90 nm and 13 nm, respectively. This is because charge trapping from the gate side only has a significant impact on the threshold voltage if the EOT becomes smaller than 5 nm. In Fig.S9b we show the corresponding ΔV_H vs. $1/t_{sw}$ dependences which look very similar. The increase of the hysteresis for slow sweep times suggests charge trapping by border oxide traps.

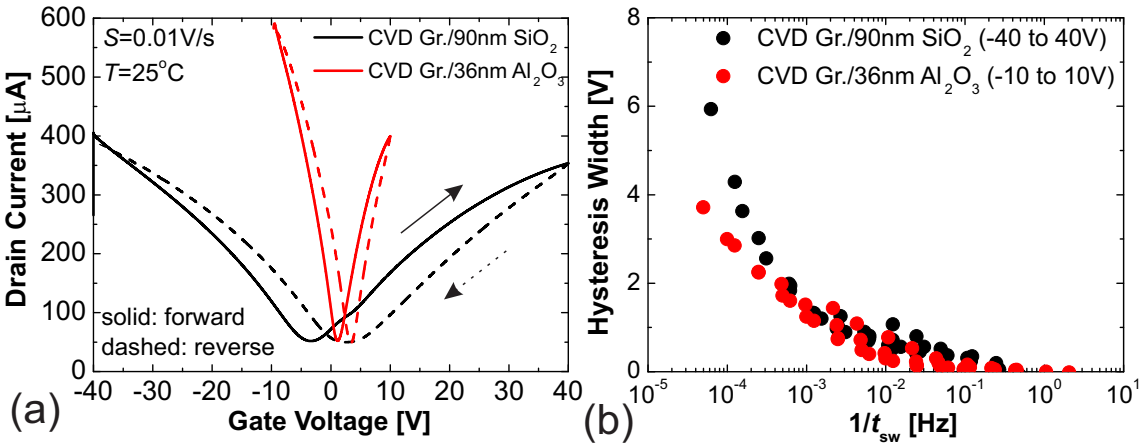

Figure S9: (a) Slow sweep I_D-V_G characteristics of back-gated GFETs with SiO_2 and Al_2O_3 insulators used as a reference. (b) The corresponding ΔV_H vs. $1/t_{sw}$ dependences.

Comparison of normalized hysteresis widths

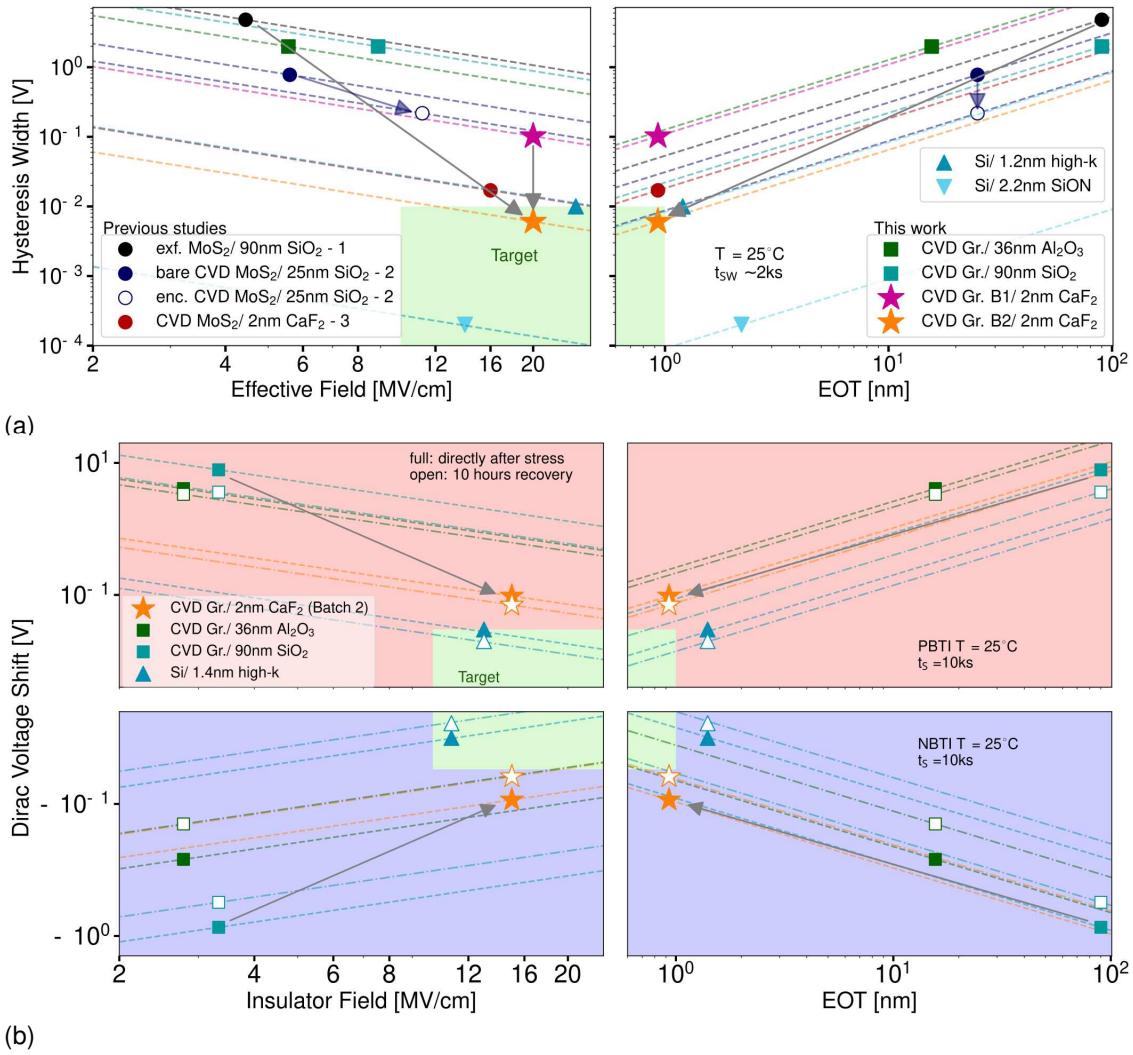

Figure S10: (a) Comparison of absolute hysteresis widths in different back-gated 2D FETs as well as Si FETs for a sweep time of about 2 ks plotted versus the effective gate field $(V_{\mathrm{G,max}} - V_{\mathrm{G,min}})/d_{\mathrm{ins}}$ (left) and versus EOT (right). Dashed lines indicate the trends for varying insulator thicknesses. (b) Comparison of absolute PBTI (top) and NBTI (bottom) drifts measured with a small time delay of about 0.5 s after the stress and after 10 hours of recovery versus the insulator field $V_{\mathrm{G,stress}}/d_{\mathrm{ins}}$ (left) and versus EOT (right). Dashed lines indicate the expected trends for varying insulator thicknesses.

In Fig.S10a we show that the hysteresis widths measured for our GFETs with CaF_2 are the smallest observed on any 2D FET also when the absolute values are compared. Fig. S10b shows the comparison of the absolute NBTI and PBTI drifts, demonstrating that the

results on the GFETs with CaF_2 come closest to the observed BTI on a commercial Si/high-k technology.

References

(1) Knobloch, T.; Uzlu, B.; Illarionov, Y.; Wang, Z.; Otto, M.; Filipovic, L.; Waltl, M.; Neumaier, D.; Lemme, M.; Grasser, T. Improving Stability in Two-Dimensional Transistors with Amorphous Gate Oxides by Fermi-Level Tuning. *Nature Electronics* **2022**, 1–11.