Supplementary

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Supplementary Note 1:

Electro-optical simulations and design

A 2-D electrical solver (SILVACO ATLAS [7]) was used to study the non-volatile electrical behavior of the III-V/Si memristor structure. This modeling software has been used successfully in other theoretical optical non-volatile structures[8,9]. The program numerically solves the Poisson, charge continuity equations, drift-diffusion transport, and quantum tunneling mechanisms. The models involved include Fermi-Dirac statistics, Shockley-Read-Hall recombination, quantum tunneling that includes direct and Fowler-Nordheim [7]. The semiconductor material parameters used for optical and electronic TCAD simulations are listed in Table *1*.

Table 1: Material parameters used in electro-optical simulations

Material	E_g (eV)	χ (eV)	VBO (eV)	CBO (eV)	n	N_{TC} (cm^{-3})	φ_d (eV)
Al_2O_3	7.0 [10]	1.5 [11–13]	3.2 [10]	2.7 [10]	1.75	-	-
HfO_2	5.7 [10]	2.5 [10]	2.7 [10]	1.9 [10]	1.9	10^{19} - 10^{20} [9,14,15]	2.0 [16–19]
SiO_2	8.9 [10]	1.3 [10]	4.5 [10]	3.3 [10]	1.44	-	-
Si	1.1 [10]	4.1 [10]	-	-	3.507 [20]	-	-
GaAs	1.43 [7]	4.07 [7]	-	-	3.406 [20]	-	-

E_g: Energy gap, χ: electron affinity, n: refractive index (at λ = 1310 nm), VBO: valance band offset, CBO: conduction band offset, N_{TC}: trap density, φ_d: electron trap level

Once the structure is built with the appropriately assigned models and trapped charge density, the band diagrams, C-V curves, and electron/hole concentrations are simulated for various biases. The spatial profiles of the change in electron/hole concentrations ($\Delta P(x,y)$ and $\Delta N(x,y)$) are then exported and used to calculate a spatial refractive index change $\Delta n(x,y)$ by the following equation [21,22]:

$$\Delta n(x,y) = -6.2\times10^{-22}\,\Delta N(x,y) - 6.0\times10^{-18}\,\Delta P(x,y) \qquad (1)$$

This equation is valid for a wavelength λ = 1310 nm and is used throughout the manuscript. Next, this spatial refractive index change $\Delta n(x,y)$ is exported into a 2D-FDE optical mode solver (Lumerical) and the non-volatile change in effective index ($\Delta_{neff,non\text{-}volatile}$) is calculated. This change can then be used to calculate non-volatile phase shifts on photonic devices such as ring resonators, Mach-Zehnder interferometers, filters, etc. The figure below illustrates the simulation procedure:

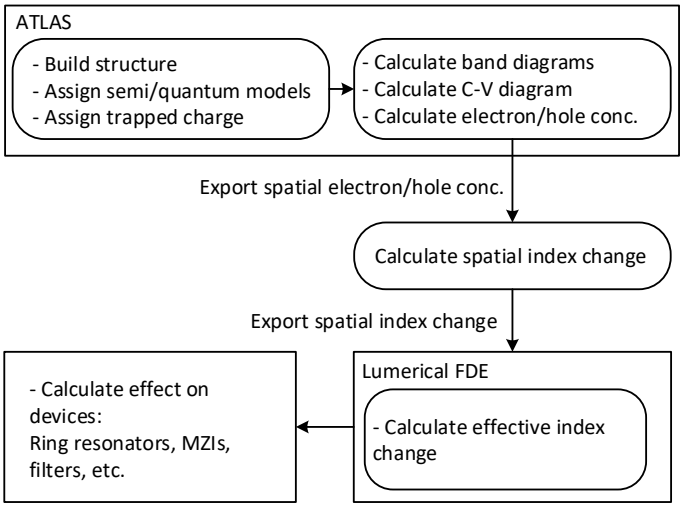

Fig. 1. Flowchart of electro-optical simulation procedure for III-V/Si memristor structure

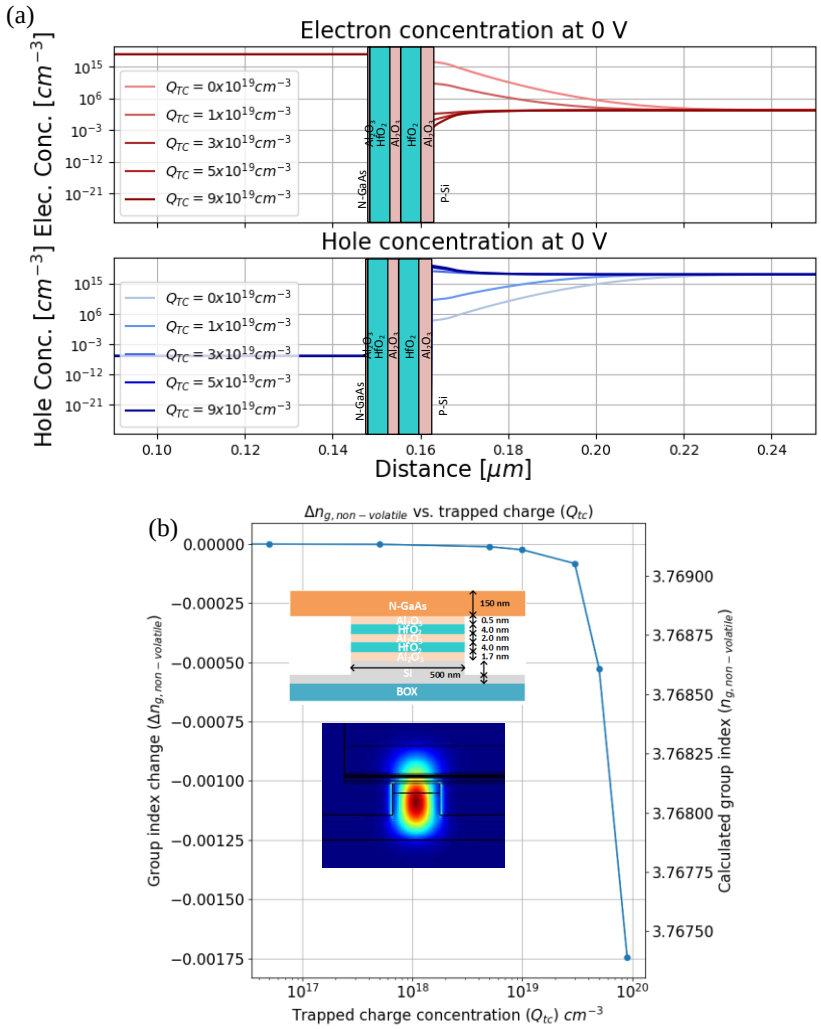

Fig. 2. Electron and hole concentrations for various QTC after set process (0 → -15 → 0 V) and (b) non-volatile group index change $\Delta n_{g,,non\text{-}volatile}$ vs. Q_{TC}.

Post-fabrication phase error correction

An alternative use of the non-volatile III-V/Si memristor cell is the role it can play in post-fabrication trimming or permanent phase error correction without consuming static electrical power. Inherent to the high index contrast of the silicon photonic material system, phase sensitive devices such as arrayed waveguide gratings (AWGs), lattice filters, and (de-)interleavers are sensitive to phase errors and are dependent on waveguide width, thickness, and refractive index non-homogeneity. In this case, the ability to use non-volatile phase tuning to correct the aforementioned errors is essential to minimizing power consumption. Changes in resonant the resonant wavelength can be described by the following equation [4]:

$$\Delta\lambda_0 = \left(\lambda_0 / n_g\right)\sqrt{\left(dn_{eff} / dw \cdot \Delta w\right)^2 + \left(dn_{eff} / dt \cdot \Delta t\right)^2} \tag{12}$$

$\lambda_0, n_{eff}, n_g, \Delta w,$ and Δt are the free-space wavelength, effective index, group index, width variation, and thickness variation respectively. Along with the group index $n_g = n_{eff} - \lambda_0 \cdot dn_{eff} / d\lambda$, the resonant wavelength variation for each dimension can be calculated as: $\Delta\lambda_0 / \Delta w = (\lambda_0 / n_g)(dn_{eff} / dw)$ and $\Delta\lambda_0 / \Delta t = (\lambda_0 / n_g)(dn_{eff} / dt)$. The effective index and group index as a function of width and thickness are plotted in Fig. *3*a – b. It can be seen that both values increase as waveguide dimensions increase because of increased modal confinement. Fig. *3*c – d illustrates width sensitivity (dn_{eff}/dw) and thickness sensitivity (dn_{eff}/dt). Throughout the paper, single-mode III-V/Si memristor waveguides are used and have design dimensions of height = 300 nm, width = 500nm, etch depth = 170nm, and GaAs thickness of 150 nm, thus resulting in effective index variations of $dn_{eff}/dw = 5.80 \times 10^{-4}$ /nm and $dn_{eff}/dt = -4.44 \times 10^{-5}$ /nm. Typically, the most critical parameter in controlling phase errors is the starting SOI wafer thickness uniformity.

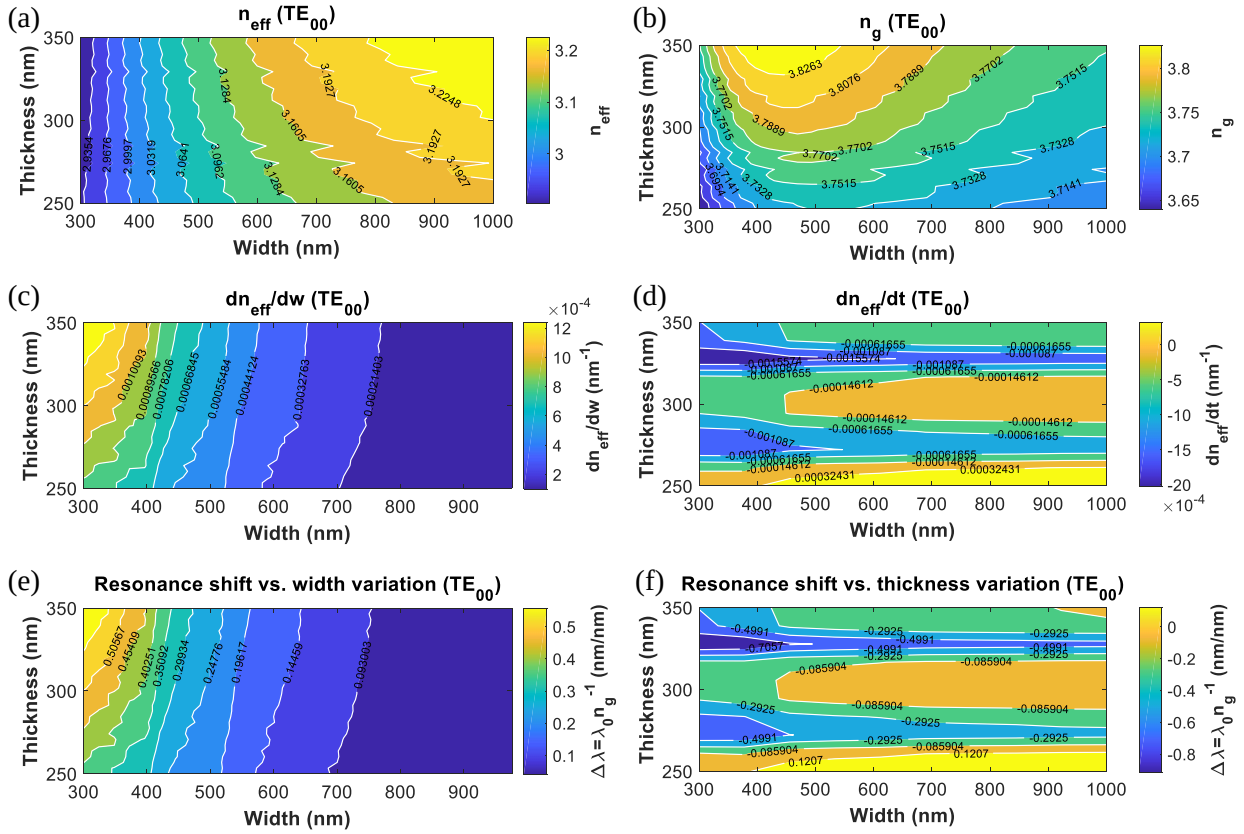

Fig. 3 III-V/Si memristor optical mode calculations for (a) effective index (n_{eff}), (b) group index (n_g), (c) effective index change vs. waveguide width (dn_{eff}/dw), (d) effective index change vs. waveguide thickness (dn_{eff}/dt), (e) wavelength shift ($\Delta\lambda_0/dw$) vs. waveguide width, (f) wavelength shift vs. waveguide thickness ($\Delta\lambda_0/dt$).

However, for the III-V/Si case, the GaAs thickness reduces this SOI thickness sensitivity significantly, and as a result, width variations play a larger role in phase errors by an order of magnitude. The wavelength shift variation are $\Delta\lambda_0/dw = 0.2457$ nm/nm and $\Delta\lambda_0/dt = -0.0187$ nm/nm as shown in Fig. *3*e – f. The use of wider waveguides can significantly reduce $\Delta\lambda_0/dw$ by another order of magnitude, however, the TE01 mode starts to appear at a width of 600 nm as seen in Fig. *3*b. We believe, the III-V/Si CTM waveguide dimensions used throughout this paper offers the best design trade-off in terms of low dn_{eff}/dw and dn_{eff}/dt while maintaining single-mode operation. If we assume a charge trap concentration of $Q_{TC} > 9\times 10^{19}$ cm^{-3}, which corresponds to a $\Delta n_{eff}^{III\text{-}V/Si} = 1.60 \times 10^{-3}$, the III-V/Si optical memristor may be capable of correcting a couple nm of variation in waveguide width and height.

Supplementary Note 2: Fabrication

In-house device fabrications starts with a 100 mm SOI wafer which consists of a 350 nm thick top silicon layer and a 2 μm buried oxide (BOX) layer. The top silicon is thinned down to 300 nm by thermal oxidation and buffered hydrofluoric (HF) acid etching, thus leaving a clean silicon surface. Silicon waveguides are defined by a deep-UV (248 nm) lithography stepper and boron is implanted to create p ++ silicon contacts. Grating couplers, silicon rib waveguides, and vertical out-gassing channels (VOCs) are respectively patterned using the same deep-UV stepper and then subsequently etched 170 nm with Cl_2-based gas chemistry. Next, the silicon wafer goes through a Piranha clean followed by buffered hydrofluoric (HF)

acid etching to remove any hard masks. Next, an oxygen plasma clean is performed followed by a SC1 and SC2 clean. The III-V wafer goes through a solvent clean consisting of acetone, methanol, and IPA, followed by oxygen plasma cleaning and a $NH_4OH:H_2O$ (1:10) dip for 1 minute. Next a dielectric of Al_2O_3 is deposited onto both GaAs and Si wafers via atomic layer deposition (ALD) by using 5 cycles of trimethylaluminum (TMA) + H_2O with a target thickness of 0.5 nm on each side. All ALD deposition temperatures are performed at 300 °C. Next, a thickness target of 3 nm HfO_2 is deposited on each sample via 30 cycles of tetrakis (ethylmethylamino) hafnium (TEMAH) + H_2O. Finally, a thickness target of 1 nm Al_2O_3 is deposited on each sample via 10 cycles of TMA + H_2O. The two samples are then mated manually at room temperature and then wafer-bonded under pressure for 250 °C (2 hour ramp) for a total of 15 hours. After wafer-bonding, the backside of the III-V is mechanically lapped until ~ 100 μm of III-V is left. An $Al_{0.20}Ga_{0.80}As$ etch stop layer allows selective removal of the remaining GaAs substrate via wet etching ($H_2O_2:NH_4OH$ (30:1)). The $Al_{0.20}Ga_{0.80}As$ is finally removed in buffered hydrofluoric acid (BHF), thus leaving a 150 nm-thick n-GaAs thin film on top of the SOI substrate. A combination of Ge/Au/Ni/Au/Pd/Ti (400/400/240/4000/200/200 Å) is deposited onto the n-GaAs as an n-contact layer. Next, the III-V film is defined and dry etched for device regions that require the use of phase tuning. Metal contact with the p-Si consists of Ni/Ge/Au/Ni/Au/Ti (50/300/300/200/5000/200 Å). Next, a plasma enhanced chemical vapor deposition (PECVD) SiO_2 cladding is deposited and the vias are defined and etched. Finally, Ti/Au metal probe pads are defined to make contact with n-GaAs and p-Si layers. The relevant fabricated devices can be seen in Fig. 5a-b.

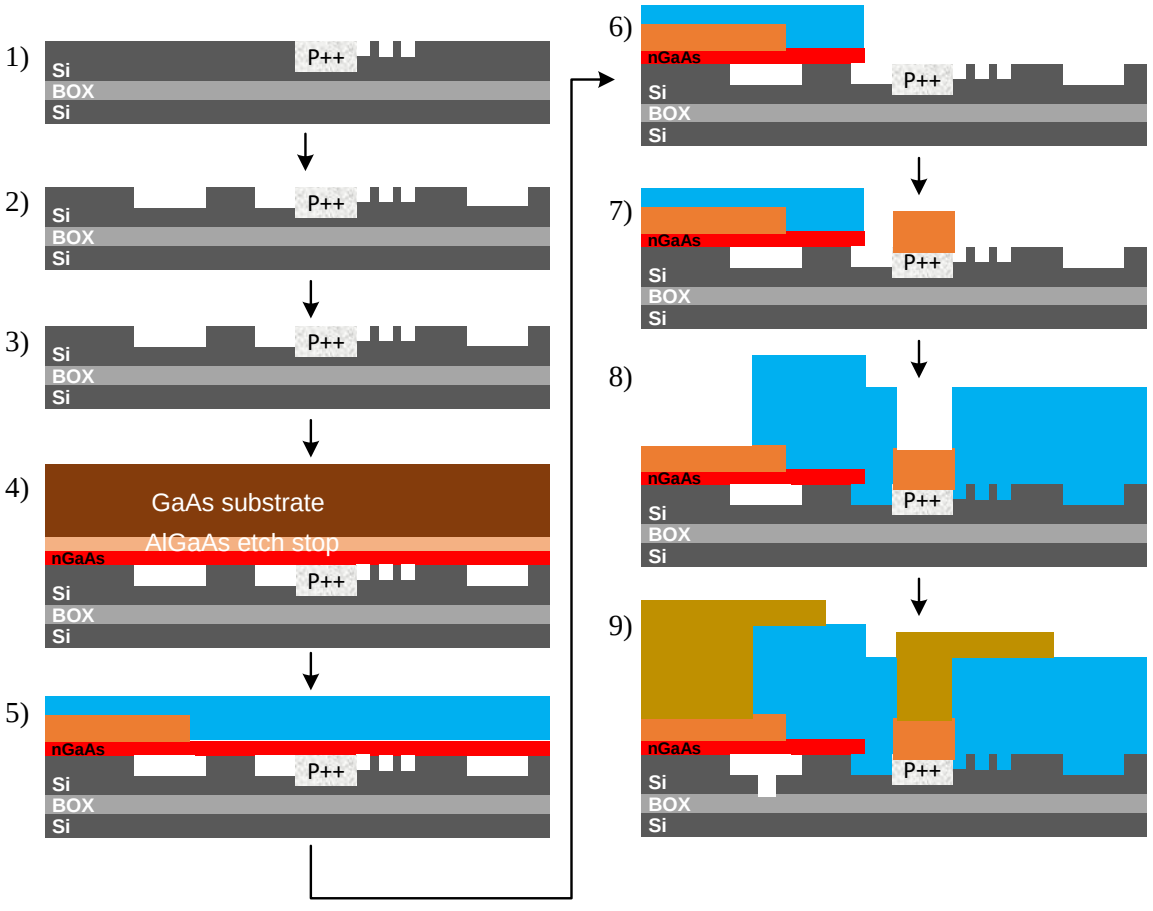

Fig. 4 Fabrication flow of heterogeneous III-V/Si photonic memristor devices.

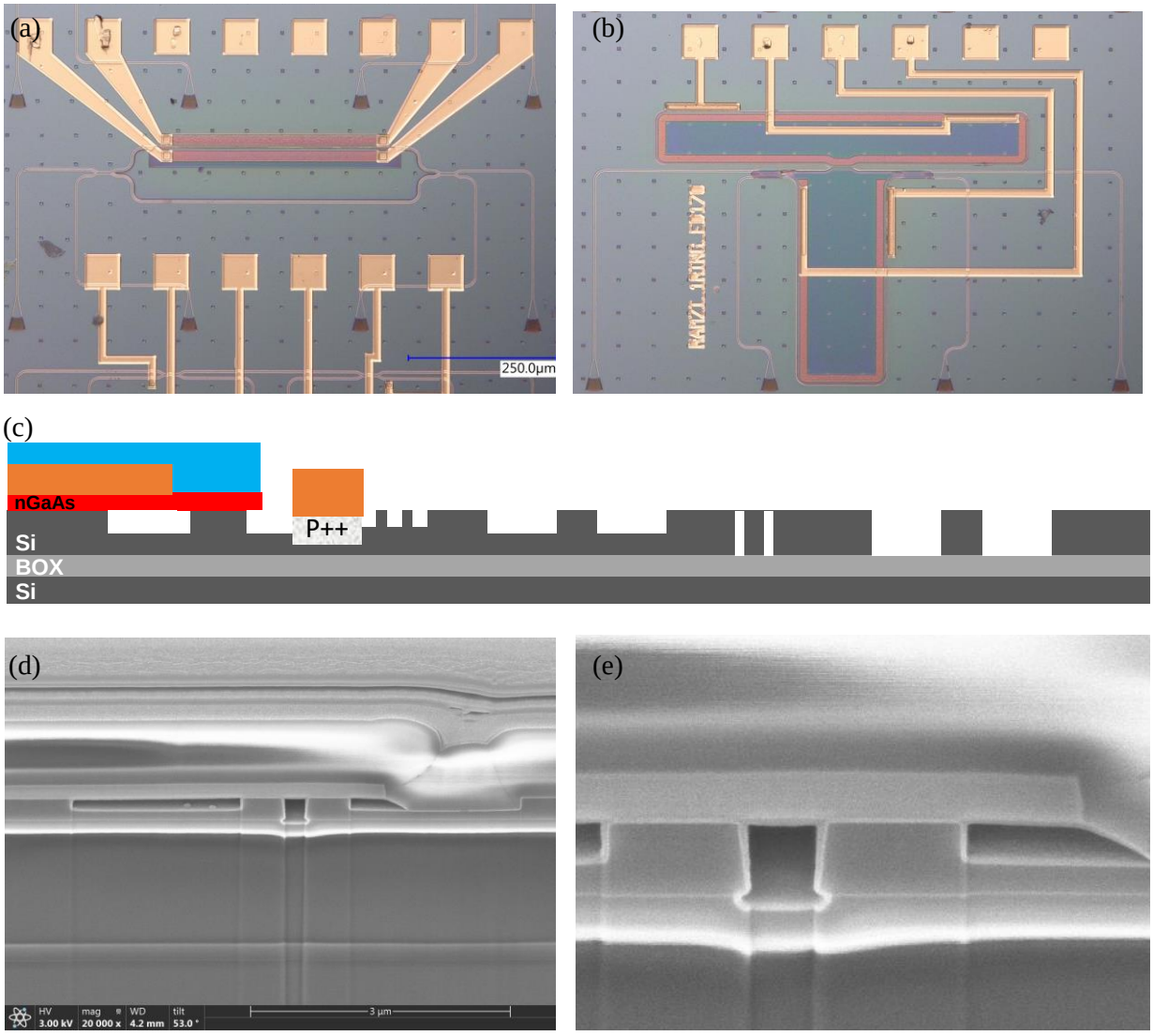

Fig. 5. Microscope images of fabricated III-V/Si photonic memristor devices (a) MZI, and (b) 1-RAMZI filter. (c) Schematic of 2-D cross-section. (d) - (e) SEM image of cross-section.

Supplementary Note 3: Transmission electron microscope (TEM) measurements of initial, set, and reset states.

We performed high resolution transmission electron microscope (HRTEM) imaging of initial, set, and reset states as shown in *Fig. 6*a-c respectively. Each image is a separate sample that was biased and subsequently imaged. There does not appear to be any visual evidence of dielectric breakdown in the n-GaAs/Al_2O_3/HfO_2/Al_2O_3/HfO_2/ Al_2O_3/Si memristor structure. There are contrast differences and may indicate variability in sample preparation as well as imaging settings. The electron dispersive spectroscopy (EDS) line scans below the TEM images also indicate minimal atomic/interfacial changes. Fig. *7*a-c shows the 2D atomic composition mapping for each respective state. Fig. *8*a-c shows the quantitative 2D strain mapping of the oxide/Si interface for each respective state. It is observed that the set state has more stain locations compared to the initial and reset states.

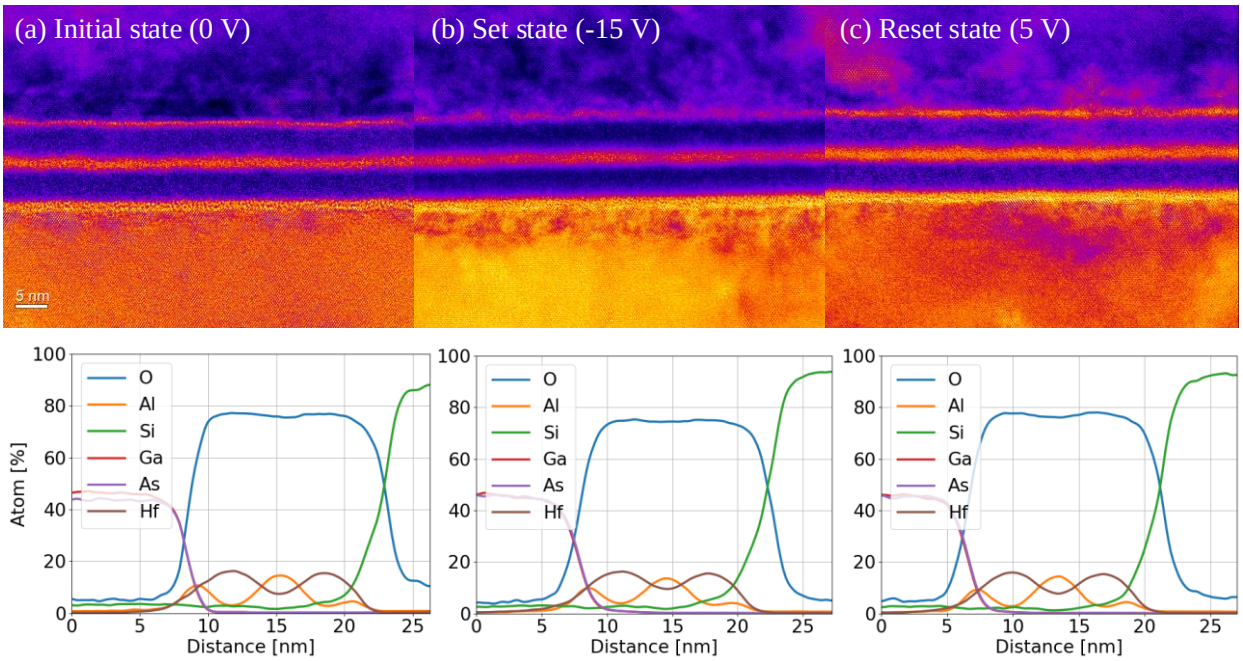

Fig. 6 TEM imaging and EDS line scan of n-GaAs/Al_2O_3/HfO_2/Al_2O_3/HfO_2/ Al_2O_3/Si memristor structure in (a) initial state (0 V), (b) set state (-15 V), and (c) reset state (+ 5 V).

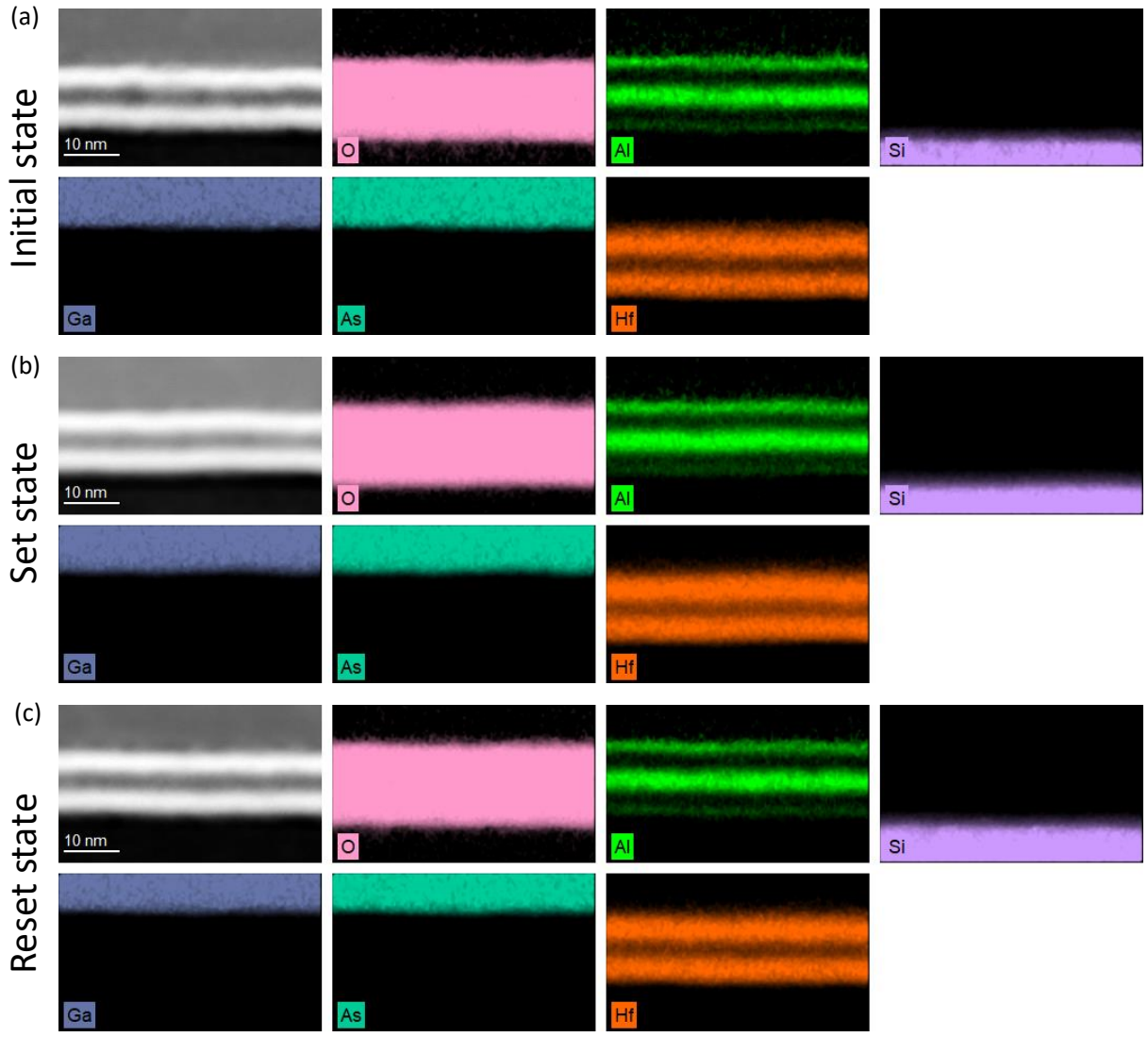

Fig. 7. 2D atomic composition mapping for (a) initial state (0 V), (b) set state (-15 V), and (c) reset state (+ 5 V).

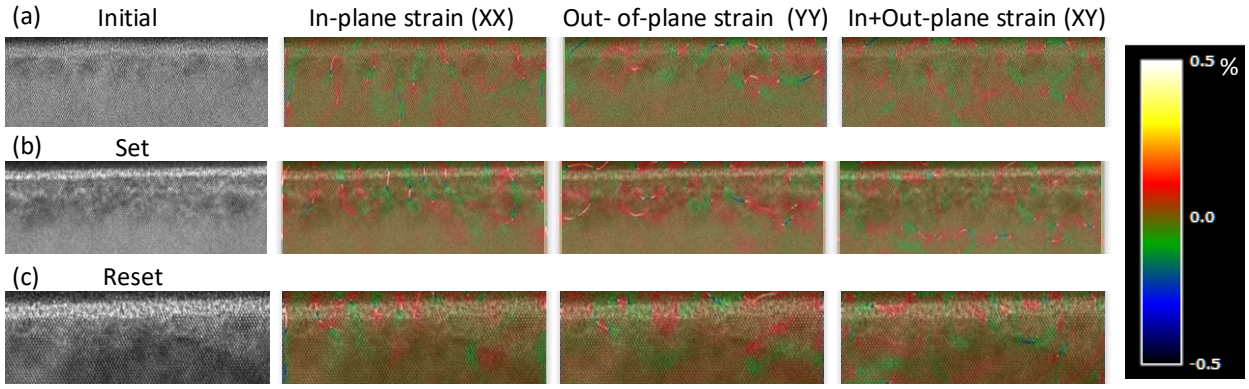

Fig. 8. 2D strain mapping via geometrical phase analysis (GPA) for (a) initial state (0 V), (b) set state (-15 V), and (c) reset state (+ 5 V).

Supplementary Note 4: High speed S_{21} measurements for multiple non-volatile states.

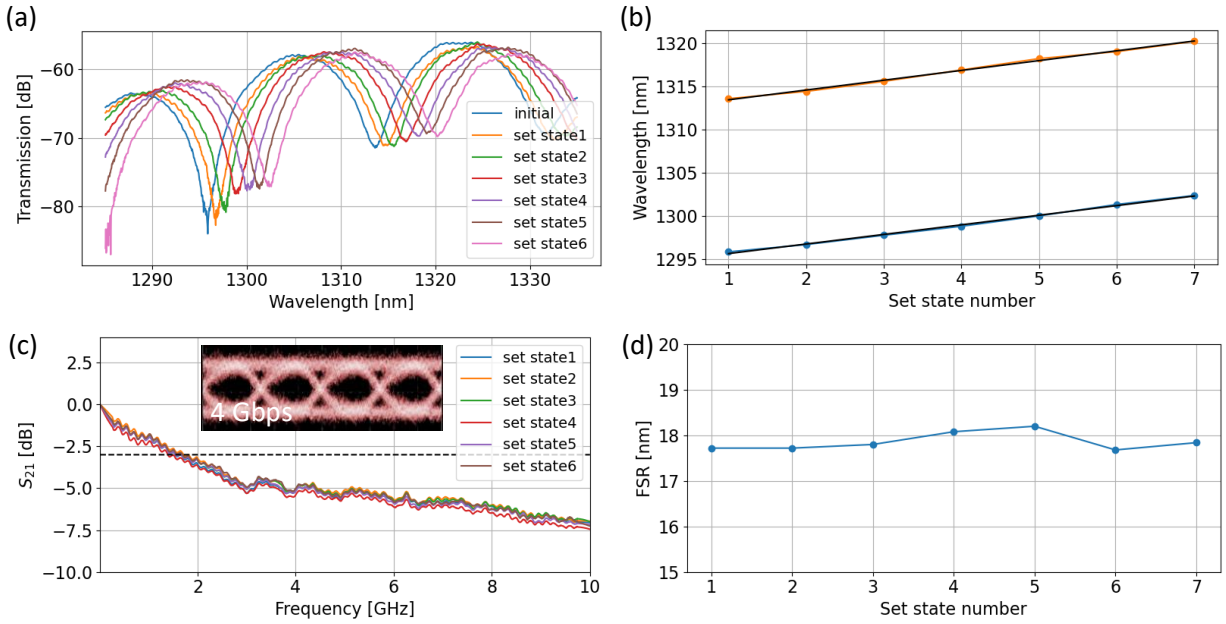

Fig. 9. (a) Optical spectrum of 6 non-volatile set-states, (b) corresponding wavelength shifts, (c) small-signal S_{21} measurement for each set state (f_{3dB} ~ 1.9 GHz) and an eye-diagram at 4 Gbps, and (d) extracted FSR for each state.

Supplementary Note 5: An extreme case of phase shift tuning > 4π

Here is one particular device that exhibited a phase shift $\Delta\varphi > 4\pi$. This corresponds to a III-V/Si group index change of $\Delta n_g^{III\text{-}V/Si} = 13.7 \times 10^{-3}$ determined by the method mentioned in the main text. The same voltage cycling is performed (0 → - 21 → 0 → 15 →0 V) and an electrical and resistive hysteresis is observed in Fig. *10*a – b respectively. Applying a bias from 0 to -21 V results in a non-volatile wavelength shift of $\Delta\lambda_{non\text{-}volatile}$ ~ 40 nm wavelength shift with near negligible optical losses (Fig. *10*c). Ramping back down from -21 to 0 V does not shift the optical response back to the original state (Fig. *10*d) and has a non-volatile wavelength stability of ~ +/- 0.2 nm (35 GHz). This indicates a non-volatile phase shift of $\Delta\varphi > 4\pi$, at essentially 0 power consumption (recorded current = 10.4 pA at 0 V).

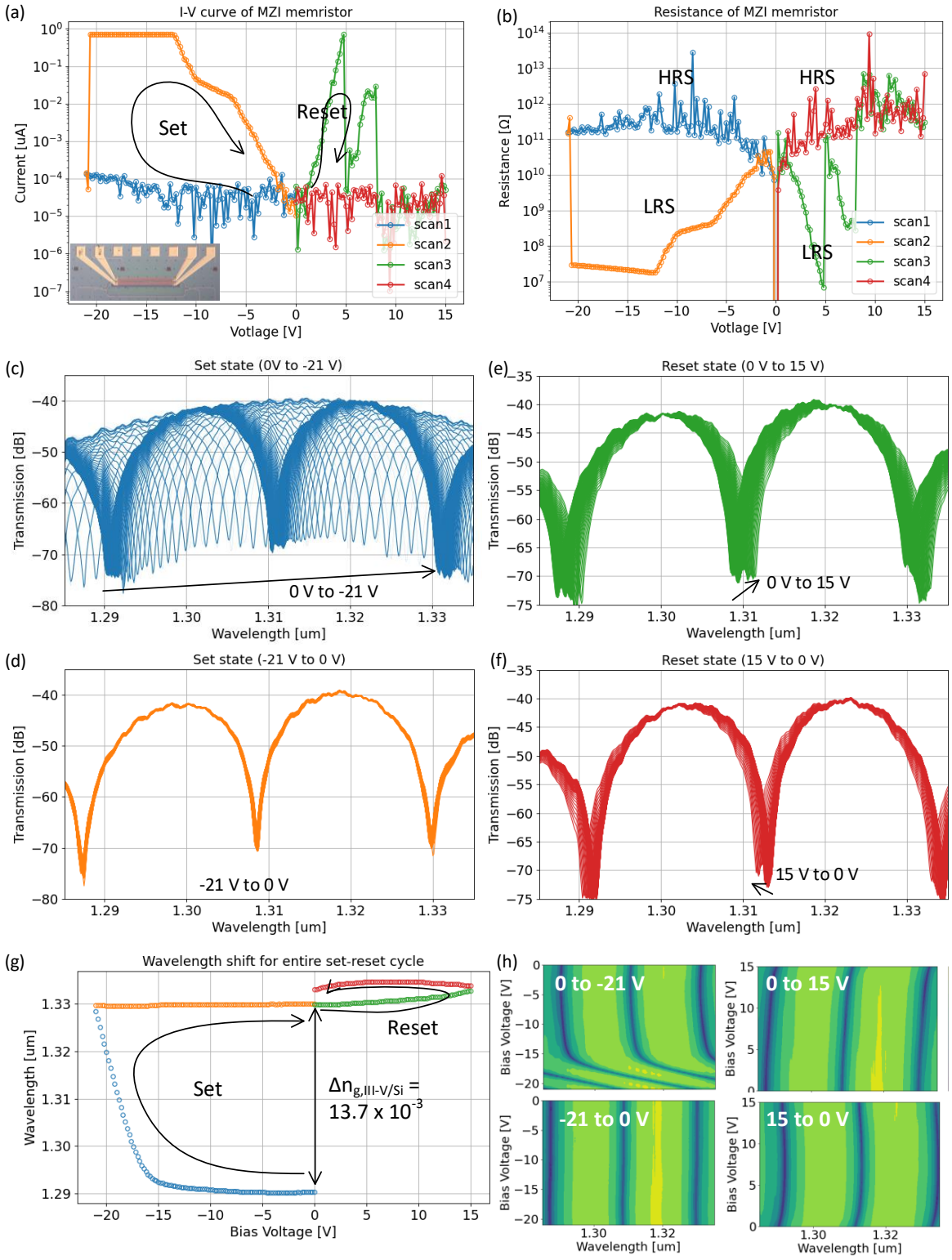

Fig. 10. (a) Measured I-V hysteresis indicating non-volatile memristive set/reset states. (b) Corresponding resistance indicating regions of high-resistance-states (HRS) and low-resistance-states (LRS). Measured optical spectrum for (c) "set" (0 to -21 V), (d) turning off "set" (-21 to 0V), (e) "reset" (0 to 15 V), and (f) turning off "reset" (15 to 0 V). (g) Tracked resonance vs. voltage, (h) spectral evolution vs. voltage.

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