Supporting Information

Boosting the Electron Beam Transmittance of Field Emission Cathode Using a Self-Charging Gate

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Note S1: The fabrication process of CNTs array and gate. The fabrication process for the gate and the CNTs array is illustrated in Figure S1a and Fig. S1b, respectively. The SiN_x/Au/Si gate was fabricated using a lithographic patterning process and film deposition technique. Initially, the cleaned 300 μm Si wafer was patterned using the 13 μm AZ9260 photoresist layer, and the hexagonal gate array, with 228 μm side and 20 μm distance, was obtained after DRIE etching process and removing the photoresist layer in sequence. Subsequently, the Au/Ti (400/50 nm) was deposited on the Si-based gate substrate using the EBE process as the metal electrode, and 1 μm SiN_x layer was then deposited on the Au/Si gate substrate using the PECVD process. Finally, the SiN_x/Au/Si gate was obtained successfully.

For the fabrication process of the cathode emitters, CNTs array was first grown on 500 μm Si substrate after the deposition of Al_2O_3 and Fe as the buffer layer and catalyst, respectively, using an automated wafer-scale TCVD system. To enhance the adhesion between CNTs and substrate and reduce the shielding effect, a transfer process was used to bond the CNTs and target substrate. Second, the Au/Ni/Cr (500/20/50 nm) was deposited on the target Si wafer as a conducting layer using the EBE process, and the patterned buffer layer was then deposited on the Au/Si substrate using the PECVD process. Subsequently, the CNTs on Si wafer, with patterned Au/Ni/Cr (500/20/50 nm) on the surface, were aligned and placed onto the target substrate. Under the treatment of 30 kPa pressure and temperature (300°C) on both substrates simultaneously for 5 minutes, the patterned CNTs array on the target substrate was obtained after removing the original substrate.

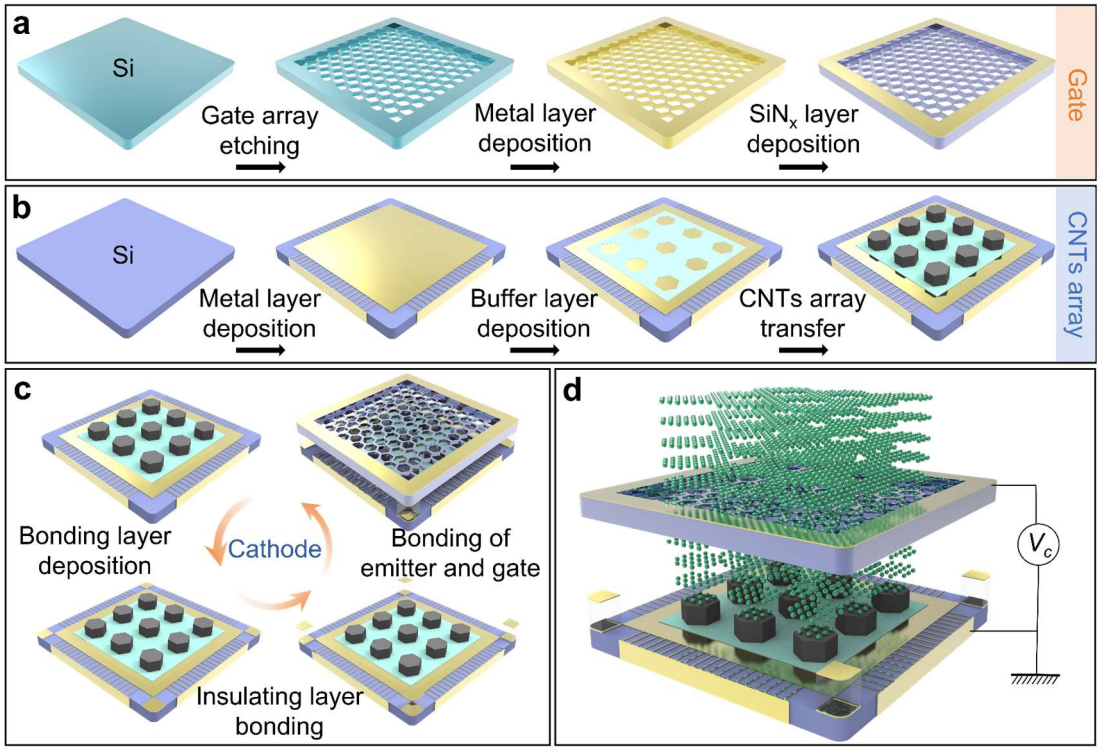

Figure S1. Schematic diagram of the cathode. The fabrication process of a) gate and b) CNTs array, respectively. c) The assembling process of the cathode. d) The schematic of the FE process of the cathode.

Following the fabrication of the gate and CNTs array, the cathode was assembled utilizing MEMS bonding technology, as depicted in Fig. S1c. Initially, a 400/50 nm thick layer of Au/Ti was deposited on both the top and bottom of the glass substrate to act as an insulating layer. Next, thermocompression technology was employed to successfully bond the gate and CNTs array emitter through the glass separator layer. When a voltage is supplied, the electrons are excited and pass through the gate under the focusing field, as demonstrated in Fig. S1d.

Note S2: The morphology and material characterizations of the cathode.

Figure S2a displays the optical images of the SiN_x/Au/Si gate with 228 μm side and 20 μm distance, magnified for better visualization. SEM images in Fig. S2b, c reveal the microscopic morphologies of the gate from different perspectives. To observe the section morphologies of the SiN_x/Au/Si gate, a high-precision DS-6 dicing saw was

used to carefully cut the gate. The resulting section view can be found in Fig. S2d, with a zoom-in view of the interfacial micro-morphologies between the Si substrate and the SiN_x/Au film shown in Fig. S2e, f, with each layer clearly labeled. And

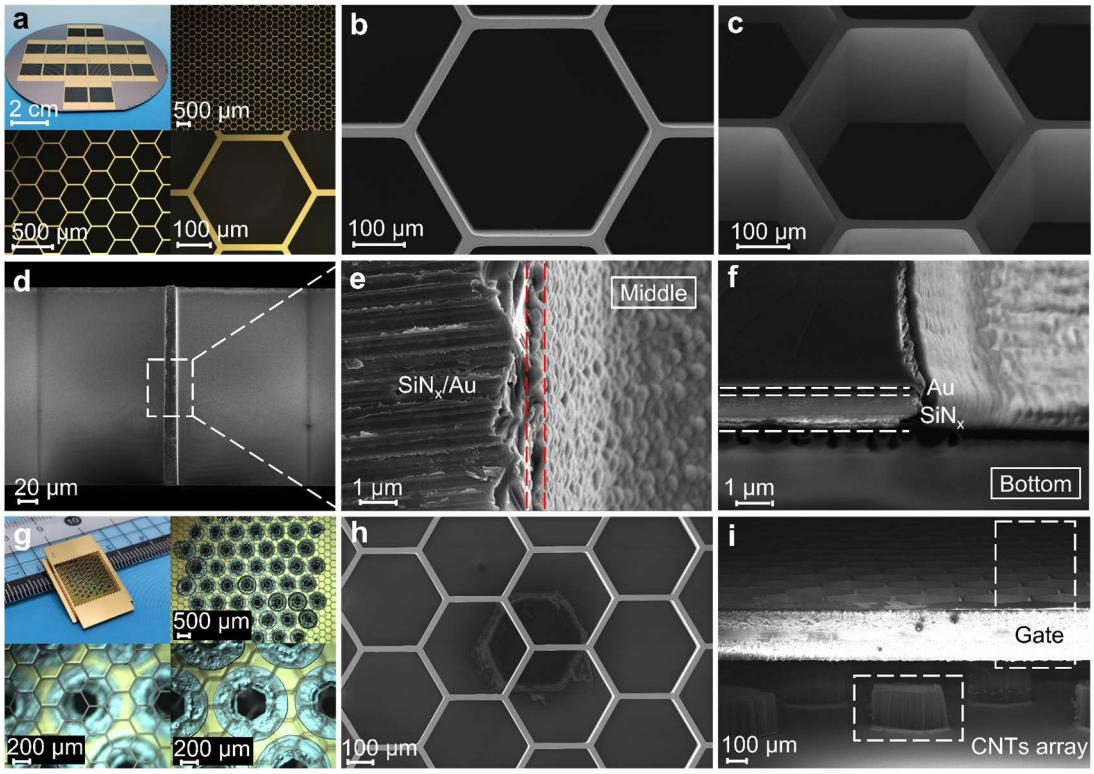

Figure S2. Morphology characterizations of the cathode. a) Optical image of the SiN_x/Au/Si gate. b, c) Top view of the SEM images of the SiN_x/Au/Si gate. d-f) Cross-sectional view of the SEM images of the SiN_x/Au/Si gate. g) Optical image of the cathode. h) The top view and i) side view of the cathode.

Fig. S2g displays the optical images of fabricated cathode, which consists of patterned CNTs array and SiN_x/Au/Si gate. SEM images in Fig. S2h, i show the top and side views of the cathode, respectively. The gate-to-CNTs distance was set to 500 μm.

As shown in the Fig. 2g, the gate potential (V_s) based on SiN_x electret is approximately -60 V after e-beam irradiation for 12 hours and decreases by around 40% within a week, which is attributed to the detrapping of electrons from the electret materials. As illustrated in Figure S3, the electrons emitted from the CNTs array can be trapped by the SiN_x/Au/Si gate due to the excellent charge storage performance, and the initial V_s of gate is V_0 after charge injecting. As the ambient humidity around the

gate rises, a conductive water layer forms on the gate surface due to chemical and physical adsorption. The increase in surface conductance and hydrone evaporation accelerate the charge decay on the SiN_x electret surface,[1] resulting in the a decrease in the V_s over time. After the conduction and hydrone evaporation process, the electrons trapped in deeper positions of SiN_x electret is retained instead of being released, resulting in a nearly 60% retention (V_s') of the initial potential (V_s) level after discharge for a week.[2]

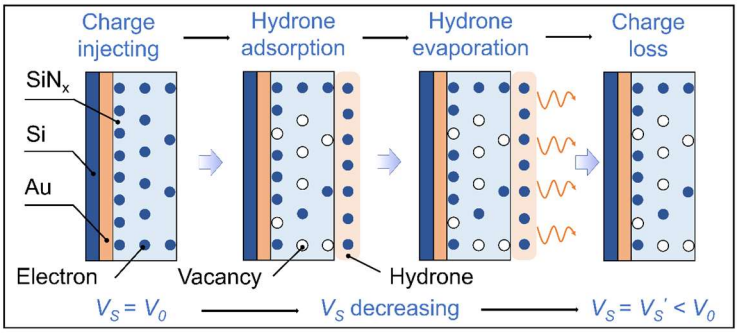

Figure S3. The mechanism analysis of the V_s dependence on the time.

Note S3: The numerical simulations of the cathode.

The cross-sectional of the simulation model is presented in Figure S4a. Here, T (300 μm), D (228 μm), and d (20 μm) represent the thickness, distance and side length of the gate, respectively. Similarly, T_1 (300 μm), D_1 (228 μm), and d_1 (20 μm) indicate the thickness, distance and side length of the CNTs array, respectively. The distance between the gate and the CNTs array is set to 500 μm, and the electric potentials of V_1, V_c, V_g, and V_a denote the potentials of the SiN_x electret, cathode substrate, Au electrode and anode, respectively. Fig. S4b shows the average electric field strength of the CNTs array surface when V_1, V_c, V_g, and V_a are set to 0 V, -500 V, 0 V, and 0 V, respectively, which is approximately 2.35×10^6 V/m. When V_1 is set to -60 V and other electric potentials of the cathode are set to the same value as mentioned above, the average electric field strength of the CNTs array surface is approximately 2.07×10^6 V/m. The slight reduction in field strength can be attributed to the negative potential applied on the SiN_x electret.

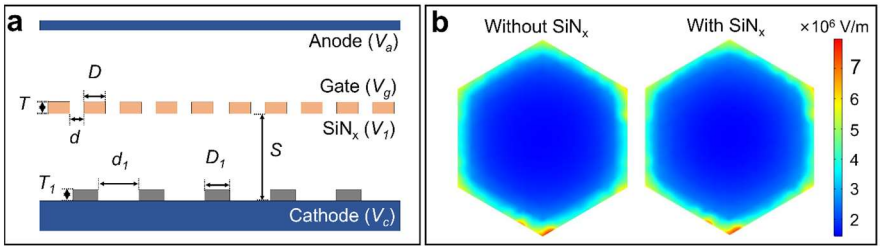

Figure S4. Simulation of the cathode with and without SiN_x electret. a) Schematic of the simulation model of the cathode. b) The electric field distribution of the surface of the CNTs array.

Note S4: Long-time measurement of the cathode.

The time dependence of the applied voltage at a constant emission current of 27 μA is shown in Figure S5, illustrating the long-term stability of the system. The current was kept constant by applying a DC voltage feedback loop continually for 550 hours, with the initial value of V_c set at 517.2 V. After the aging process, the average applied V_c is 412.0 V with a fluctuation of 12%, and an average decrease in voltage of 56.4 mV/hr over time. This phenomenon is attributed to the vacuum pressure within the chamber; at the start of the stability measurement, the vacuum quality is expected to decrease somewhat due to outgassing during the aging process, resulting in a higher voltage supply. As the outgassing process continues, the vacuum condition improves, leading to improved emission performance.[3]

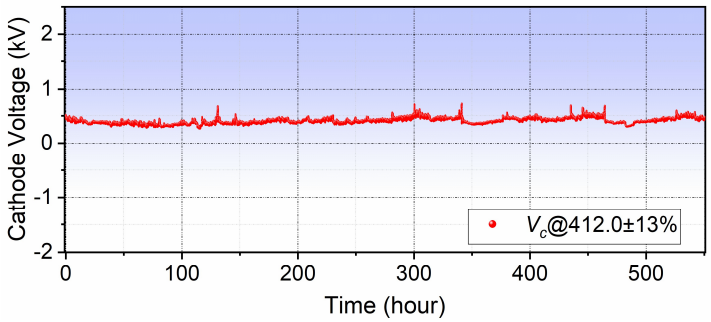

Figure S5. The applied V_c of the cathode as a function of time.

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micromachined devices. In: *IEEE Trans. Dielectr. Electr. Insul.* IEEE (1996).

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