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Graphene-Fullerene Heterostructures as Robust and Flexible Nanomechanical Bits

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Abstract

Electrical computers have revolutionized society over the past several decades, but questions have remained about their ability to perform in extreme environments. This has motivated the recent surge of interest in developing mechanical computing platforms at all length scales, including the nanoscale, in which traditional electrical computers are augmented with mechanical ones. However, most proposed nanomechanical bits are volatile memory bits based on the dynamic response of nanomechanical resonators, and as such there is a need to develop robust and reprogrammable entirely non-volatile nanomechanical bits. Here, we exploit the multiple quasi-stable configurations of the graphene/fullerene/graphene (GFG) van der Waals heterostructure to work as a novel non-volatile nanomechanical bit. The GFG heterostructure is unique and robust in that it can return to its initial state without further mechanical input, it can be used for logic functions at relevant operating temperatures through simple application of uniaxial strain, it can exhibit reprogrammability between five basic logic gates (NOT, AND, NAND, OR, NOR) by varying the magnitude or direction of applied strain, and it can be used to represent combinatorial logic through full and half adders. These findings provide a new opportunity to develop mechanical computers based on the large class of nanomaterials.

Keywords: Nanomechanical bit, van der Waals heterostructure, Strain engineering
I. INTRODUCTION

The traditional silicon-based electronic computer has brought about a significant revolution for human society since its development in the last century. Despite its enormous impact, electronic computers are not able to function properly in extreme environments like high or low temperature,\(^1\) which has motivated the development of alternative computing platforms, such as the optical logic gate,\(^2,3\) the quantum computer,\(^4\) the DNA-based parallel computer,\(^5,6\) the thin film mechanical-strain-gated switches,\(^7,8\) and the mechanical computer.\(^9-13\) In particular, mechanical computers are a promising candidate to supplement the traditional electronic computer at extreme environments, as their functionality depends on mechanical motion, which can be sustained in extreme environments such as high temperatures or under nuclear radiation.\(^9,10\) Furthermore, mechanical computers are able to interact mechanically with their environments, for example with other robots, which enables them to serve as a local processor and sensor for environmental information.\(^11-13\)

As the fundamental building block of the mechanical computer, bit storage and bit processing have been realized by utilizing various structures or mechanisms on the macro or microscale. Typically, structures that possess multiple quasi-stable configurations have been proposed to be used as the bit storage device.\(^14-19\) Mechanical computers that function by switching between multiple stable states act as nonvolatile systems. For example, a 3D-printed metamaterial was designed to propagate a mechanical signal using an embedded bistable spring.\(^14,18\) Merkle et al. designed a mechanical logic gate using the links and the rotary joint, which can be used to construct AND and OR logic gates.\(^17\) As a flexible system, the origami structure can be designed to have several multi-stable configurations that can be used to store bit information,\(^15\) and the origami system can interact with the surrounding environment.\(^16\)

Besides the macro and mesoscale mechanical computers, nanoscale mechanical computers have also been investigated in recent years. One of the most intriguing features of nanoscale mechanical computers are their nanoscale dimensions, which are on the same order as the traditional electronic transistor. While nanomechanical computers are not expected to replace existing CMOS technology, there may be opportunities to combine the advantages of both mechanical and electronic computing platforms.\(^19,20\) For example, nanomechanical computers have lower switching energy while maintaining satisfactory operation speed,\(^20-22\)
which may reduce energy consumption during operation. In recent years, the emergence of nanomaterials has opened a new development path for nanomechanical computers, such as nanomechanical gates based on silicon micro/nano beams or graphene.\textsuperscript{23,24} However, most nanomechanical computing systems at present are either of the volatile nature or CMOS-based nanoelectromechanical non-volatile systems. In volatile systems, nanomechanical resonators have been shown to be a useful building block for bit storage and logic gates, based on their high-frequency mechanical oscillations\textsuperscript{25} and nonlinear, large-amplitude oscillations.\textsuperscript{26,27} These nanomechanical bits and logic gates exploit the (oscillating) dynamic states of the resonator, which requires additional energy input to maintain the dynamic stability.\textsuperscript{20} However, the energy consumption of highly integrated volatile nanomechanical logic gates is a critical concern that must be addressed in modern computing. In contrast, non-volatile mechanical computers that experience quasi-static deformation between equilibrium states offer the advantage of low energy consumption in highly integrated designs, and they can store discrete state information without additional external energy. Most nanoelectromechanical non-volatile systems still require electrostatic actuation, which may restrict their practical applications and impede integration.\textsuperscript{28-30}

Mechanical computers, whether they are developed on volatile or non-volatile technologies, and regardless of whether they are nano or macro-scale, should satisfy several basic requirements for practical usage. First, the mechanical logic system should be able to return to its initial state, and thus original logical function, without external intervention. Second, the mechanical logic system should be reprogrammable, to reduce the complexity of integration. Finally, mechanical computers should be able to realize sequential logic in order to build devices with more complex and flexible functions.

In this work, we demonstrate that a graphene/fullerene/graphene (GFG) van der Waals heterostructure,\textsuperscript{31} which has multiple quasi-stable states, can be used as the basis to construct two key components for non-volatile nanoscale mechanical computers, i.e. the mechanical memory and logic gates. Specifically, the flexibility of graphene and the unique spherical structure of the fullerenes\textsuperscript{32} enables multiple multiple quasi-stable states through a competition between the bending energy of graphene and the van der Waals cohesive energy between layers. The resulting GFG based functional components can be accurately and robustly driven by the mechanical strain engineering. We use molecular dynamics (MD) simulations to show the functionality and specific advantages of the GFG heterostructure.
FIG. 1: Strain engineering for the GFG nanomechanical bit. (a) ‘State 0’: the GFG heterostructure is in the adhered configuration. (b) ‘State 1’: the GFG heterostructure is in the separated configuration. The in-plane strain drives the GFG heterostructure to transit from ‘State 0’ to ‘State 1’.

system, and particularly that it is one of the first non-volatile nanomechanical computing systems that can return to its initial state without further mechanical input, be used for logic functions at relevant operating temperatures through simple application of uniaxial strain, exhibit reprogrammability between five basic logic gates (NOT, AND, NAND, OR, NOR) by varying the magnitude or direction of applied strain, and be used to represent combinatorial logic through full and half adders.

II. GFG MECHANICAL MEMORY

A. One-bit memory

The GFG heterostructure contains three atomic layers, in which a fullerene layer is sandwiched by two graphene layers as shown in Fig. 1. The top and bottom graphene layers in the center region can be separated or adhered, depending on the width of the free space in the middle fullerene layer shown in Fig. 1(b). The configuration for the GFG heterostructure is governed by the competition between the bending energy and the cohesive energy. The bending energy drives the system to be in the separated state, while the cohesive energy tries to keep the system in the adhered configuration. The competition between the bending energy and the cohesive energy leads to a critical value of 3.4 nm for the width of the free space in the fullerene layer, as shown in Fig. 1 (b). The GFG heterostructure is in the sepa-
rated (adhered) configuration for free space narrower (wider) than 3.4 nm. For convenience, the GFG heterostructure is characterized by the width of the free space within the middle fullerene layers, \( W_S = L_x \times (1 - \alpha) \), where \( \alpha \) is the area ratio between the fullerene and the graphene layers, and \( L_x \) is the length of graphene layers in the x direction. A narrower free space in the fullerene layer corresponds to smaller free space width with more fullerenes.

The adhered configuration of the GFG heterostructure can be regarded as ‘State 0’ for the bit state, which can be driven to ‘State 1’ by applying tensile strain as illustrated in Fig. 1. The lateral size of the GFG heterostructure in Fig. 1 is 9.7 \( \times \) 9.9 nm\(^2\), while the free space width is \( W_S = 3.9 \) nm. Periodic boundary conditions are applied along the x and y directions, while free boundary conditions are applied in the z-direction. The logic gate operation is insensitive to temperature as shown in Fig. 2 (a), where the system in ‘State 0’ is heated from 10 K to 500 K during 1 ns. The system is further thermalized for another 1 ns at high temperature 500 K. From the potential energy of the system, we find that the system stays in ‘State 0’ during the entire heating process due to the large energy barrier (about 149.4 ev at 10 K) that needs to be overcome in order to transition between ‘State 0’ and ‘State 1’. To demonstrate the robustness of the GFG logic gate, we used tensile strain to drive transitions between ‘State 0’ and ‘State 1’ for 200 cycles at different temperatures. Figs. 2 (b)-(d) show that the transition between states ‘0’ and ‘1’ by tensile strain is still robust after 200 cycles for 40 ns at 10 K, showing that the GFG heterostructure can function well in extremely low temperature environments. Similar robustness can also be observed for higher temperatures 300 K and 500 K, where the 500 K temperature exceeds the current maximum allowed operating temperature of well-known CPUs (Intel\(^{33}\), AMD\(^{34}\), Citrix\(^{35}\)) and GPUs (Nvidia\(^{36}\)) of about 380 K. Thus, the GFG logic gates have the potential to improve the performance of traditional computers at high temperatures.

We now examine the accuracy in differentiating these two logic states ‘0’ and ‘1’. We simulate the tensile stress-strain relationship for five GFG heterostructures with the free space width \( W_S = 3.9, 4.8, 5.8, 6.8, \) and 7.8 nm, as shown in Fig. 2 (e). The ultimate tensile strain (\( \varepsilon_{\text{Max}} \)) of GFG heterostructures is 15.6%. These five structures are in the ‘State 0’ prior to the application of tensile strain at 300 K. With the increase of the strain, there is a sudden jump in the stress-strain curve, corresponding to the transition from the ‘State 0’ to ‘State 1’. The jumping regime is the inaccurate regime, as the GFG heterostructure in this regime is neither ‘State 0’ nor ‘State 1’. We can estimate possible error rates for the
FIG. 2: Stability and robustness of the GFG nanomechanical bit. (a) The potential energy variation during the heating process for the GFG heterostructure in ‘State 0’. (b-d) The potential energy variation during 200 cycles for the transition of the GFG nanomechanical bit between ‘State 0’ and ‘State 1’ at 10 K, 300 K, and 500 K. (e) The stress-strain relation for the tensile strain process of the GFG heterostructure with different free space width $W_S$. (f) The relation between the critical strain to drive the transition from ‘State 0’ to ‘State 1’ and the free space width $W_S$ in the graphene layers.

logic gate by comparing the inaccurate strain regime to the full strain regime,

$$E = \frac{\Delta \varepsilon}{\varepsilon_m},$$

where the $\Delta \varepsilon$ is the strain range for the transition regime, while $\varepsilon_m$ is the full strain range. The estimated error rate is only about 0.97%, which is within the acceptable range compared with other mechanical logic gates. The error rate of reversible molecular mechanical logic gates can reach the order of $10^{-5}$ to $10^{-3}$. Furthermore, it is obvious that the critical strain ($\varepsilon_C$) for structural transition from state ‘0’ to ‘1’ increases linearly with the increase of the free space width $W_S$ in the fullerene layer of the GFG heterostructure, as shown in Fig. 2 (f). The linear fitting is $\varepsilon_C = W_S \times 1.5 - 4.2$. Based on the ultimate tensile strain, the range for
the free space width of the GFG heterostructures used to construct logic elements is from 3.4 nm \((W_{\text{Min}})\) to 13.2 nm \((W_{\text{Max}})\), while the state of the GFG heterostructure cannot be changed via tensile strain if the free space width is outside this range. This demonstrates the flexibility in choosing the size of the GFG heterostructures as logic elements, as for GFG heterostructures with free space width in the range \([W_{\text{Min}}, W_{\text{Max}}]\), their states can be changed through application tensile strain in the range of \([\varepsilon_C, \varepsilon_{\text{Max}}]\). In order to demonstrate the design of logic devices more clearly, we have used GFG heterostructures of specific sizes in the following sections.

B. Two-bit memory structure

The GFG heterostructure can also be used as the basic building block to construct more complex mechanical logic systems with storage and computing capabilities. Several methods have been proposed to integrate logic elements for mechanical computers, including the dual rail logic\(^{38}\) and the rigid rod.\(^{39}\) The dual rail logic duplicates the signal path to provide a distinct 0-signal, which is more complex and requires more physical space. In contrast, the rigid rod method is flexible and is applicable to both micro and nano scales, so this method has been widely applied to connect basic logic elements or transmit signals.\(^{14,15,17,18}\)

We adopt diamond nanowires as the rigid rod to construct the GFG logic system, where the diamond nanowires are used to apply in-plane strain to the GFG heterostructures. Importantly, diamond nanowires are able to connect with GFG heterostructures through covalent bonding, as diamond has experimentally been grown on graphene or fullerene substrates.\(^{40-44}\) The \((111)\) crystal surface of diamond bonded with graphene has been found to be stable,\(^ {43}\) and a clean interface is formed between graphene and diamond as shown in Fig. 3 (a). The clean interface between GFG and diamond enables the strain applied to the diamond to transform the GFG heterostructure between different stable mechanical states. The dimension of the GFG heterostructure is \(11.1 \times 10.1 \text{ nm}^2\) and the free space width is \(W_S = 5.8 \text{ nm}\). Periodic boundary conditions are applied along the \(y\) direction, while free boundary conditions are applied in the \(x\) and \(z\) directions, respectively. These boundary conditions are applied to the two-bit memory structures (Fig. 3) in this section, while the same boundary conditions are also applied to the simulation of all logic gates in the following section (Fig. 4).
FIG. 3: GFG nanomechanical bit memory. (a) Top and side views of the graphene-diamond hybrid structure. (b) The two-bit nanomechanical memory is driven from ‘00’ to ‘11’ by the tensile strain. (c) The transition from ‘01’ to ‘10’.

We construct two mechanical logic gates in Fig. 3. To save computational cost, we reduce the dimension of the diamond nanowire and treat the diamond nanowire as a rigid body, as we have found that the diamond nanowires remain rigid during the entire tensile straining process. In Fig. 3 (b), these two GFG logic gates are both at ‘State 0’, so the whole system is initially at the ‘00’ state. We define the ‘In = 1’ when 4.5% tensile strain is applied, while ‘In = 0’ means no strain is applied. By applying the mechanical strain, these two GFG logic gates transform simultaneously from ‘State 0’ to ‘State 1’, so the whole system changes from the ‘00’ to the ‘11’ state. The full dynamic transformation process can be found in Movie S1, which also clearly shows that the diamond nanowire remains rigid during the whole tensile strain process.

Fig. 3 (c) illustrates the transition from the ‘01’ to the ‘10’ state. This is accomplished using two GFG logic gates. The left logic gate is in ‘State 0’, while the right GFG logic gate is in ‘State 1’ by pre-stretching it with a tensile strain of 4.5%. Applying tensile strain to the left GFG logic gate causes it to stretch and transit from ‘State 0’ to ‘State 1’, while the right GFG logic gate is compressed and transits from ‘State 1’ to ‘State 0’. As a result, the
FIG. 4: The GFG nanomechanical logic gates. (a) The NOT gate. (b) The AND gate. (c) The OR gate. (d) The XOR gate. (e) Truth tables of NOT, AND, OR, and XOR logic gates.

full GFG system transits from the ‘01’ to the ‘10’ state. The simulation movie for Fig. 3 (c) can be found in Movie S2.

III. GFG MECHANICAL LOGIC GATES

A. Logic gates

We now construct several basic logic gates based on the GFG heterostructure as shown in Fig. 4. To do so, we introduce additional nanowire conductors (blue lines in Fig. 4), which are a different material to the rigid diamond rods, in order to transport electrical signals when contact is established with the GFG heterostructure, to act as a state indicator. Specifically, core-shell heterostructure nanowires have been shown to have potential for future nanoelectronic applications. Realistic choices for the nanowire conductors are Co$_2$SiAl$_2$O$_3$ core-shell or Ge/Si core-shell nanowires, where such nanodevices can be created using transfer printing techniques. The electrical signal can be transported in ‘State 1’ when contact is established between the conductive nanowire and the GFG heterostructure, while the electrical signal is blocked by the GFG heterostructure in ‘State 0’ due to the lack of contact between the conductive nanowire and the GFG heterostructure. One advantage of using electrical signals as a state indicator is that it is easier to observe as compared to observing
structural changes, which is one approach to integrating mechanical computers within existing electronic computing platforms. However, we note that conductive nanowires are not necessary in GFG logic gates, which can function without the electrical state indicator.

The NOT gate is demonstrated in Fig. 4 (a). The dimension of the GFG heterostructure is $10.5 \times 10.8 \text{ nm}^2$. The free space width is $W_S = 5.3 \text{ nm}$, for which the critical strain is 3.75% to drive the free space into the separated configuration according to Fig. 2 (f). The GFG heterostructure is initially prestretched for the strain of 4.5% and is in ‘State 1’, where the graphene layer and the nanowire conductor are in contact. When 4.5% compressive strain is input, i.e., the rigid rod is driven along the direction of the two red arrows, the GFG heterostructure will transit to ‘State 0’, where the nanowire conductor and the graphene layer are not in contact, and thus no electrical signal is transmitted. The simulation movie for the NOT gate can be found in Movie S3, where an additional GFG heterostructure (initially in ‘State 0’) is included at the input signal. We find that these two GFG heterostructures are always in the opposite states, which illustrates the function of the NOT gate in a clear manner.

The AND gate is realized in Fig. 4 (b). The dimension of the GFG structure is $12.6 \times 10.8 \text{ nm}^2$. The free space width is $W_S = 6.8 \text{ nm}$, for which the free space is large in the fullerene layer of the GFG heterostructure. According to Fig. 2 (f), the critical strain is 6.0%, above which the free space will be driven into the separated configuration. As a result, the GFG will be driven into the separated ‘State 1’ only if 4.5% tensile strain is applied to both In1 and In2, resulting in a total strain of 9%. Otherwise, the GFG will be always in ‘State 0’ if only one or no input is applied. The movie for the AND gate can be found in Movie S4.

Fig. 4 (c) is the OR gate. The dimension of the GFG structure is $10.5 \times 10.8 \text{ nm}^2$. The free space width is $W_S = 5.3 \text{ nm}$, which is slightly smaller than that for the AND gate in Fig. 4 (b). Because the critical strain for structural transition from state ‘0’ to ‘1’ increases linearly with the increase of the dimension of the free space in the fullerene layer of the GFG heterostructure, as shown in Fig. 2 (f), a smaller strain is required for to drive the GFG heterostructure from ‘State 0’ to ‘State 1’. Keeping the same tensile strain as that for the AND logic gate the electrical signal can be output if the mechanical strain is applied to either In1 or In2. The movie for the OR gate can be found in the Movie S5. The functional-complete NAND gate and NOR gate are constructed using the above AND, OR and NOT
gates, which can be found in Fig. S1 (a-b) in the supplemental material.

The complex XOR gate shown in Fig. 4 (d) is also important in the construction of logic devices, as the XOR gate can judge whether the input signals are consistent. The dimension of the GFG heterostructure is $10.5 \times 10.8 \text{ nm}^2$, and the free space width is $W_S = 5.3 \text{ nm}$. In the top layer, the GFG heterostructure on the left is in ‘State 1’ by pre-stretching it with a tensile strain 4.5%, while the right GFG heterostructure is in ‘State 0’. The GFG heterostructures in the bottom layer have the opposite setting, i.e. the left GFG heterostructure is in ‘State 0’, while the right GFG heterostructure is in ‘State 1’ by pre-stretching it with a tensile strain 4.5%. Applying tensile strain to the top layer and the bottom layer, the states of the GFG logic gates in the top layer transit from ‘State 1 (left) and State 0 (right)’ to ‘State 0 (left) and State 1 (right)’, while the states of GFG logic gates in the bottom layer transit from ‘State 0 (left) and State 1 (right)’ to ‘State 1 (left) and State 0 (right)’. Thus no electrical signal is transmitted as the initial states. The XNOR gate is the opposite operation of XOR. When the input signals are consistent, the electrical signal is transmitted. The structure for the XNOR is illustrated in Fig. S1 (c).

B. Reprogrammability

An important consideration for the building blocks of mechanical computing is their versatility, or reprogrammability, in which a single mechanical building block can be used to exhibit different computing functionality. Here, we demonstrate how the GFG heterostructures can achieve reprogrammability, where multiple logic functions can be achieved using the same structure by varying the input strain. Specifically, for GFG heterostructures of the same dimension, five basic logic gates (NOT, AND, NAND, OR, NOR) can be realized by changing the magnitude or the direction of the applied strain. As shown in the Fig. 5 (a), the dimension of the GFG structure is $10.5 \times 10.8 \text{ nm}^2$ and the free space width is $W_S = 5.3 \text{ nm}$. Taking this as the base structure, we now demonstrate how the five basic logic gates can be obtained shown by varying the input strain.

The NOT logic gate is shown in Fig. 5 (b). If 6.0% tensile strain is applied to the right diamond rod, and the left diamond rod is fixed, the state of the GFG heterostructure is ‘State 1’ as shown in the top image of Fig. 5 (b). Starting from that configuration, we define the ‘In=1’ when 6.0% mechanical compressive strain is applied to the right diamond rod,
FIG. 5: The reprogrammability of GFG nanomechanical logic gates. (a) The GFG heterostructure. (b) The NOT gate. (c) The AND gate. (d) The OR gate. (e) The NAND gate. (f) The NOR gate.

While ‘In=0’ means no strain is applied. Then the Input and the Output are always in the opposite states. For example, the GFG heterostructure will transit to ‘State 0’ by applying the 6.0% compressive strain (‘In=1’) as shown in the bottom image of Fig. 5(b).

The AND logic gate is shown in Fig. 5 (c). The initial state of the GFG heterostructure is ‘State 0’, i.e. the same as shown in Fig. 5 (a). We define the ‘In=1’ when 3.0% mechanical tensile strain is applied, while the ‘In=0’ means no strain is applied. As a result, the GFG will be driven into the separated ‘State 1’ only if the 3.0% tensile mechanical strain is applied to both In1 and In2. Otherwise, the GFG will be always in ‘State 0’ if only one or no inputs are applied.

The OR logic gate is shown in Fig. 5 (d). Similar to the AND logic gate, the initial state of the GFG heterostructure is ‘State 0’, i.e. the same as shown in Fig. 5 (a). As long as the input strain is increased, the AND logic gate in Fig. 5 (c) can be transformed into the OR logic gate. We define the ‘In=1’ when 6.0% mechanical tensile strain is applied, while the ‘In=0’ means no strain is applied. Thus, the GFG will be driven into the separated ‘State 1’ if the mechanical strain is applied to either In1 or In2.
The NAND logic gate is shown in Fig. 5 (e). Based on the AND logic gate, the NAND logic gate can be obtained by setting pre-tensile strain and changing the direction of the input strain. 6.0% pre-tensile strain is applied to obtain the GFG heterostructure in the top image of Fig. 5 (e), for which the state of the GFG heterostructure is ‘State 1’. We define the ‘In=1’ when 3.0% mechanical compressive strain is applied for both In1 and In2, while ‘In=0’ means no strain is applied. Then the GFG will be driven into the separated ‘State 0’ only if the 3.0% tensile compressive strain is applied to both In1 and In2.

Finally, the NOR logic gate is shown in Fig. 5 (e). Similar to the NAND gate, the NOR gate starts by setting the pre-tensile strain of 6.0% to obtain the GFG heterostructure in the top image of Fig. 5 (e). At this time, the state of the GFG heterostructure is ‘State 1’. We define the ‘In=1’ when 6% mechanical compressive strain is applied, while ‘In=0’ means no strain is applied. Then the GFG will be driven into the separated ‘State 0’ if the 6.0% tensile compressive strain is applied to either In1 or In2.

In summary, the input strain for the AND/NAND logic gates is twice that for the OR/NOR logic gates in programmable logic elements, and setting a tensile pre-strain on the GFG structure can transform AND/OR logic gates into NAND/NOR logic gates. We also note that there are dimensional restrictions on all of the logic gates. Specifically, for the OR and NOR logic gates, the maximum strain input should be half of the ultimate tensile strain of the GFG heterostructure ($\varepsilon_C=7.8\%$ tensile strain), because each input must be greater than the critical value $\varepsilon_C$ for structural transformation, while the free space width $W_S$ should lie within the range of 3.4 - 8.0 nm. For the NOT, AND and NAND logic gates, the sum of input strains greater than the critical value $\varepsilon_C$ will cause structural transition, and the free space width $W_S$ should lie within the range of 3.4 - 13.2 nm. For the initial structure in Fig. 5(a), $W_S$ should be within 3.4 - 13.2 nm for NOT, AND and NAND gates, and between 3.4-8.0 nm for OR and NOR gates.

C. Logic function

The above basic logic gates can be used to construct complex logic functions such as the half-adder and the full-adder. The half-adder shown in Fig. 6 (a) is able to perform the addition of two single binary digits, which consists of AND and XOR gates. The 4.5% tensile strain is input through In1 and In2. The addition result is output by the carry bit ‘Out1’
FIG. 6: The GFG nanomechanical logic function. (a) The half-adder. The addition process of $1 + 1 = 10$ is illustrated. (b) The full-adder. The addition process of $1 + 1 + 1 = 11$ is displayed. (c) The binary counter, which also has the function of a half adder. (d) Truth tables of half-adder, full-adder, and binary counter.

and the sum bit ‘Out2’, which are controlled by the AND gate and XOR gate, respectively. To clearly display the logic diagram, we simplify the model diagram by using black lines as the diamond nanowire, and brown and red lines as the conductive nanowires. The different colored nanowires represent different circuits. The addition process for the half-adder is illustrated in Fig. 6 (a) for ‘$1+1=10$’. As the ‘In1=1’ and ‘In2=1’ are input, the AND gate change to ‘1’ and the brown circuit is connected. By contrast, the XOR gate accepts two identical input signals, resulting in the red circuit failure. All possible addition results from the half-adder are summarized in Fig. 6 (a).

The full-adder shown in Fig. 6 (b) can perform the addition of three single binary digits.
The black lines represent the diamond nanowire for the tensile strain, while other lines are for the nanowire conductors. The addition process for ‘1+1+1=11’ is displayed in Fig. 6 (b). All possible addition results from the full-adder are summarized in Fig. 6 (b). The above half-adder and full-adder show the combinatorial logic, whose output signal only depends on the current input signal. Even if the components with computing functions can be constructed through combinatorial logic, their spatial requirements and structural complexity must be considered. As one of the significant properties of logic circuits, sequential logic is as important as the reprogrammability of structures. It can reduce the complexity of structures and build powerful logic devices such as counters and latches. For example, Mei et al. can reduce the compact crossover from 176 signal elements to 25 signal elements through sequential logic.\textsuperscript{56}

The GFG logic gates can also be used to exhibit sequential logic, where the output depends on not only the current input but also the historical input. As shown in Fig. 6 (c), a binary counter based on GFG logic gates can be operated through the sequential logic, which can perform a binary count of the number of Input. It consists of a NAND logic gate, an AND logic gate with a longer adhesive length ($W_S = 8.8\ nm$), and the half-adder in Fig. 6 (a). The added AND logic gate, the NAND logic gate and the XOR logic gate control the state of Out2 together. During the operation of the counter, the left diamond rod is fixed and the right diamond rod is pulled to the right for counting. Note that the Input is not released after each stretch (4% tensile strain) until it is counted three times. The initial state is shown in Fig. 6 (c), both the Out1 and Out2 states are ‘0’ and the counter has a count of ‘0’. When the mechanical tensile strains is first applied, the red circuit is turned on and the Out2 state changes to ‘1’ as shown in Fig. 6 (c-i). At this time, the Out1 is ‘0’ and the Out2 is ‘1’, which indicates that the number of Input is ‘1’. Based on the first Input, the second Input continues to apply a 4% tensile strain to the counter. The Fig. 6 (c-ii) shows that the brown circuit is turned on and the red circuit is turned off. The states of Out1 and Out2 are ‘1’ and ‘0’, respectively. Then the counter has a count of ‘2’, which indicates that the number of Input is ‘2’. When the tensile strains is third applied based on the second Input, the red and brown circuits remain the same as the previous step, and the green circuit is turned on as shown in Fig. 6 (c-iii). Both the Out1 and Out2 states are ‘1’ of the counter, which indicates that the number of Input is ‘3’. Finally, the Out1 and Out2 can return to the initial states by releasing the tensile strain.
During the operation of this counter, the state of the logic gate depends on the current input and the historical input, such as the changes of the added AND logic gates. Furthermore, the structure in Fig. 6 (c) is reprogrammable, which also has the function of a half adder. When using the structure as a half-adder, the tensile strain applied to the left and right diamond rods ranges from 3.75% to 4.5%. At this time, the added AND and NAND logic gates do not change, and there is no difference between the structure in Fig. 6 (a) and the structure in Fig. 6 (c). Therefore, GFG logic gates have the potential to build more powerful computing components through reprogrammable and sequential logic.

IV. DISCUSSION

In the above examples, the fundamental mechanism for the operation of the GFG based mechanical memory and logic gates is to drive the transition of the GFG heterostructure between two quasi-stable configurations (adhered and separated). Specifically, we have demonstrated that the structural transition of the GFG heterostructure can be realized by applying in-plane tensile strain. We note that we could alternatively use out-of-plane compressive strain to drive the GFG structure to transit from the separated ‘State 1’ to the adhered ‘State 0’. The GFG mechanical memory driven by the out-of-plane strain is shown in Fig. S2. Both in-plane and out-of-plane strains can be used together to provide a rather flexible manner to realize the nanomechanical bit as shown in Fig. S2.

We have also demonstrated that the GFG-based mechanical computing system exhibits several important advantages compared to previously proposed mechanical computers, as summarize in Table I. First, GFG logic gates can be returned to their initial states by releasing the applied tensile stress. Second, GFG heterostructures have excellent stability and robustness under a wide range of ambient temperatures (10 K-500 K), which have the potential to improve the performance of traditional computers at high/low temperatures. Third, the structural transformation of GFG heterostructures is based on the competition between the bending energy of graphene and the van der Waals cohesive energy. It has a relatively simple structure and can directly be produced experimentally. Fourth, the GFG heterostructures are reprogrammable, in which five basic logic gates (NOT, AND, NAND, OR, NOR) can be achieved using the same structure by varying the direction and magnitude of applied strain. Using the same structure to achieve different logical functions can effec-
TABLE I: Performances of various mechanical computers across different length scales.

<table>
<thead>
<tr>
<th>Structure</th>
<th>Size</th>
<th>System</th>
<th>Reset</th>
<th>Temperature</th>
<th>Cycle</th>
<th>Memory</th>
<th>Reprogrammability</th>
<th>Sequential Logic</th>
</tr>
</thead>
<tbody>
<tr>
<td>GFG heterostructures</td>
<td>≥ 5 nm</td>
<td>Non-volatile</td>
<td>Automatic</td>
<td>10-500 K</td>
<td>≥ 200</td>
<td>One-bit</td>
<td>Multi-bit</td>
<td>Yes</td>
</tr>
<tr>
<td>(This work)</td>
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<tr>
<td>Triangulated cylindrical origami</td>
<td>9-15 cm</td>
<td>Non-volatile</td>
<td>Room temperature</td>
<td>One-bit, Multi-bit</td>
<td>Yes</td>
<td></td>
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<tr>
<td>tunable truss structures</td>
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<tr>
<td>Origami waterbomb</td>
<td>4 cm</td>
<td>Non-volatile</td>
<td>Automatic</td>
<td>Room temperature</td>
<td>≥ 5</td>
<td>One-bit</td>
<td>Multi-bit</td>
<td>Yes</td>
</tr>
<tr>
<td>mechanomemory</td>
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<tr>
<td>Bi-stable flexure</td>
<td>38 µm-20 cm</td>
<td>Non-volatile</td>
<td>Continuous logic operations without resetting</td>
<td>Room temperature</td>
<td>One-bit</td>
<td></td>
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<tr>
<td>mechanisms</td>
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<tr>
<td>Nanoelectromechanical relay</td>
<td>100 nm-5.92 µm</td>
<td>Non-volatile</td>
<td>Automatic</td>
<td>300-473 K</td>
<td>≥ 40</td>
<td>One-bit</td>
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<td>without pull-in instability</td>
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<tr>
<td>Soft conductive</td>
<td>0.5-1.6 cm</td>
<td>Non-volatile</td>
<td>Automatic</td>
<td>Room temperature</td>
<td>≥ 6</td>
<td>One-bit</td>
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<td>mechanical metamaterials</td>
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<tr>
<td>Reprogrammable mechanomaterials</td>
<td>0.96 cm</td>
<td>Non-volatile</td>
<td>Room temperature</td>
<td>One-bit</td>
<td>Yes</td>
<td>Yes</td>
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<tr>
<td>Reprogrammable mechanical</td>
<td>3 cm</td>
<td>Non-volatile</td>
<td>Room temperature</td>
<td>≥ 3000</td>
<td>One-bit</td>
<td>m-bit</td>
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<tr>
<td>Soft modules</td>
<td>0.2-2 cm</td>
<td>Non-volatile</td>
<td>Room temperature</td>
<td>≥ 500</td>
<td>One-bit</td>
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<td>rigid Frames</td>
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<tr>
<td>CMOS compatible</td>
<td>30-2200 nm</td>
<td>Non-volatile</td>
<td>Automatic</td>
<td>233-400 K</td>
<td>≥ 20</td>
<td>One-bit</td>
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<td>Nanomechanical</td>
<td>2 nm-1 µm</td>
<td>Volatile</td>
<td>Automatic</td>
<td>Room temperature</td>
<td>One-bit</td>
<td>Multi-bit</td>
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<td>Fredkin gate</td>
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<td>Driven chain of spherical particles</td>
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<td>One-bit</td>
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<tr>
<td>Single</td>
<td>3-500 µm</td>
<td>Volatile</td>
<td>Automatic</td>
<td>288-358 K</td>
<td>One-bit</td>
<td>Multi-bit</td>
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<td>micromechanical resonator</td>
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<tr>
<td>Phenom-based mechanical calculator</td>
<td>0.2-12.5 cm</td>
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<td>Room temperature</td>
<td>≥ 12</td>
<td>One-bit</td>
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<td>Microelectromechanical</td>
<td>2.3-500 µm</td>
<td>Volatile</td>
<td>Automatic</td>
<td>262-384 K</td>
<td>≥ 1000</td>
<td>Multi-bit</td>
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<td>resonators partial electrodes</td>
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<td>Cascadable reconfigurable</td>
<td>3-850 µm</td>
<td>Volatile</td>
<td>Automatic</td>
<td>Room temperature</td>
<td>Multi-bit</td>
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<tr>
<td>Cantilever-based resonator</td>
<td>200 nm-10 µm</td>
<td>Volatile</td>
<td>Automatic</td>
<td>Room temperature</td>
<td>One-bit</td>
<td>Yes</td>
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</tbody>
</table>

Fifth, the GFG heterostructures can realize the sequential logic. Based on the sequential logic, more functional logical devices can be designed, such as counters and latches. Overall, the GFG logic gates highlight the benefit of reversibility, excellent stability and robustness, simple structure, reprogrammable and sequential logic, which can be combined with traditional
electronic computers at nanometer scale to improve their performance.

V. CONCLUSION

In summary, we have demonstrated that, as a novel van der Waals heterostructure, the GFG heterostructure has multiple quasi-stable configurations, which enables it to be utilized as the fundamental bit unit for non-volatile nanomechanical computing. In-plane tensile strain can be used to drive the GFG-based mechanical memory to work efficiently and robustly, with low computation error and high stability in extreme environments. MD simulations have been performed to illustrated the function of basic logic gates including AND, OR, NOT, NAND, NOR, XOR and XNOR. We believe this is one of the first non-volatile nanomechanical computing systems that is reprogrammable, can be used to exhibit sequential logic, can return to its initial state without requiring additional external energy input, and that can further go beyond binary computation systems by including more van der Waals layers. Our findings provide a new idea for the design of mechanical computers at the nanoscale, which has the potential to be widely used in various extreme environments in supplement to traditional computers.

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Data availability Data supporting the findings of this study are available from the corresponding author on request.

Author contributions Yixuan Xue conducted the research and interpreted the results, and Harold S. Park and Jin-Wu Jiang provided guidance throughout the research. Yixuan Xue, Harold S. Park, and Jin-Wu Jiang prepared the manuscript.

Competing interests The authors declare no competing financial interests.

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