Supplementary Material

Graphene-Fullerene Heterostructures as Robust and Flexible Nanomechanical Bits

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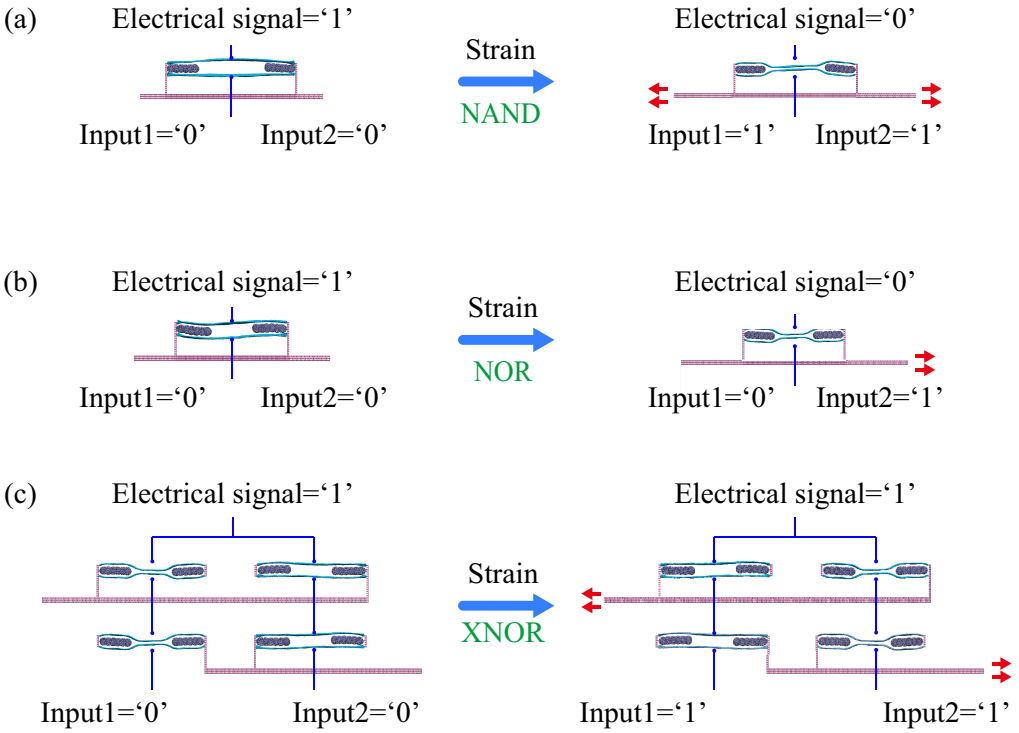
The logic gates

The NAND gate is realized in Fig. S1 (a). The dimension of the GFG structure is 12.6×10.8 nm^2. The free space width is $W_S = 6.8$ nm, for which the critical strain is 6.0%. The GFG heterostructure is initially prestretched for the strain of 9.0% and is in 'State 1', where the graphene layer and the nanowire conductor are in contact. As a result, the GFG will be driven into the separated 'State 0' only if 4.5% compressive strain is applied to both Input1 and Input2, resulting in a total strain of 9%. Otherwise, the GFG will be always in 'State 1' if only one or no input is applied. The movie for the NAND gate can be found in Movie S6.

Fig. S1 (b) is the NOR gate. The dimension of the GFG structure without strain is 10.5×10.8 nm^2. The free space width is $W_S = 5.3$ nm, for which the critical strain is



Input1	Input2	Output
1	1	0
1	0	1
0	1	1
0	0	1

Input1	Input2	Output
1	1	0
1	0	0
0	1	0
0	0	1

Input1	Input2	Output
1	1	1
1	0	0
0	1	0
0	0	1

Fig. S1: The GFG nanomechanical logic gates. (a) The NAND gate. (b) The NOR gate. (c) The XNOR gate.

3.75%. The GFG heterostructure is initially prestretched for the strain of 4.5% and is in 'State 1', where the graphene layer and the nanowire conductor are in contact. Thus, keeping the same compressive strain as that for the NAND logic gate, the electrical signal can be output if the mechanical strain is applied to either Input1 or Input2. The movie for the NOR gate can be found in the Movie S7.

The complex NXOR gate shown in Fig. S1 (c) is also important in the construction of logic devices, as the NXOR gate can judge whether the input signals are consistent. The dimension of the GFG heterostructure is 10.5×10.8 nm^2, and the free space width is $W_S = 5.3$ nm. In the top layer, the GFG heterostructure on the right is in 'State 1' by pre-stretching it with a tensile strain 4.5%, while the left GFG heterostructure is in 'State 0'. The GFG heterostructures in the bottom layer have the same setting. Applying compressive strain to the top layer and the bottom layer, the states of the GFG logic gates transit from 'State 1 (right) and State 0 (left)' to 'State 0 (right) and State 1 (left)'. Thus the electrical signal is transmitted as the initial states.

Flexible construction of logic gates

In addition to the in-plane tensile strain, there are many ways to adjust the cohesive energy to construct logic devices, such as the out-of-plane compressive strain. As shown in Fig. S2 (a), the free space width W_S of GFG heterostructure is smaller than the critical value 3.4 nm, and the graphene layers are separated by fullerene. After

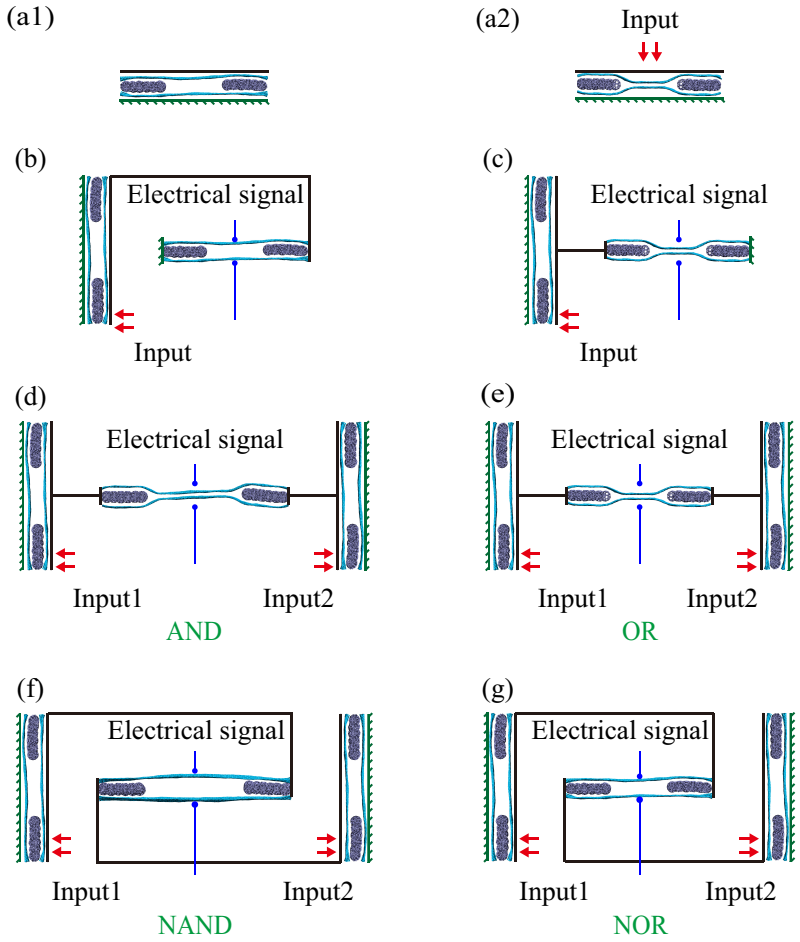


Fig. S2: The GFG nanomechanical logic gates. (a1) 'State 1': the GFG heterostructure is in the separated configuration. (a2) 'State 0': the GFG heterostructure is in the adhered configuration. (b) The two-bit nanomechanical memory is driven from '00' to '11'. (c) The two-bit nanomechanical memory is driven from '01' to '10'. (d) The AND gate. (e) The OR gate. (f) The NAND gate. (g) The NOR gate.

the out-of-plane compressive strain is applied, the GFG heterostructure changed from 'State 1' to 'State 0'. Therefore, the GFG logic gates can be flexibly constructed by combining the in-plane and out-of-plane strain. Examples of logic devices are shown in the Fig. S2 (b-g). The black lines, blue lines and green lines are the diamond rigid rods, nanowires and fixed walls, respectively. Thus, the position of GFG heterostructures and diamond rods can not be strictly limited, and the logic gates can be flexibly built according to the requirements of actual space.