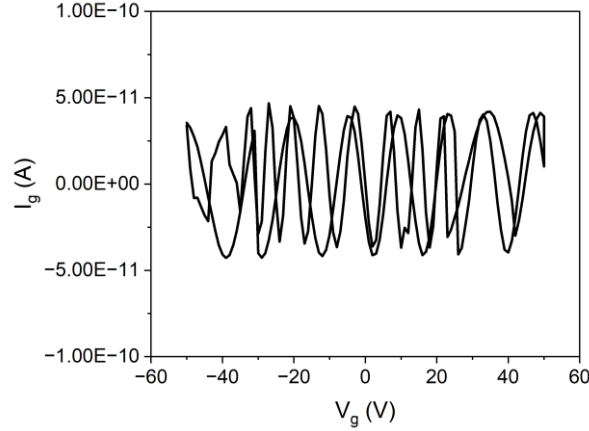


# Asymmetric two-dimensional ferroelectric transistor with anti-ambipolar transport characteristics

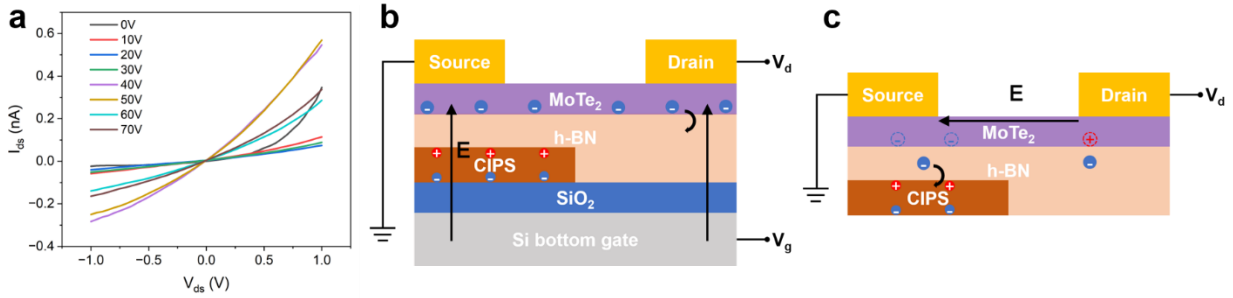
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**Figure S1** Leaking current curve against  $V_g$



**Figure S2** Retention test results of the device. **a** Output curves of the device after applying 10 s of  $V_g$  at different strength and withdrawing. **b** Schematic of the charge generation and transfer behaviors in the device with  $V_g$  applied. **c** Schematic of the charge behaviors in the device as a source-gated transistor.

Fig S2 presents the results of the retention test, which involves the application and subsequent withdrawal of different values of  $V_g$  for a duration of 10 s. Upon withdrawal of  $V_g$ , the ferroelectric  $\text{CuInP}_2\text{S}_6$  acts as a gate controlling the barrier on the source side, enabling the device to function as a source-gated transistor. Output curves are presented in Fig S2a, revealing a noticeable rise (from 0 V to 50 V) and fall (above 60 V) in the current level as  $V_g$  increases. In the low  $V_g$  range, higher values result in stronger polarization retention, whereas depolarization occurs at higher  $V_g$ . This change is attributed to the charge-storage properties of h-BN. Under high gating electric field, electrons produced in the channel can migrate to h-BN, as illustrated in Fig S2b. After withdrawal, the remaining electrons combine with the ferroelectric layer and causes depolarization. Additionally, a production of sporadic holes may be induced in the channel. The charge behaviors are described in Fig S2c. As a consequence, lower current levels are observed after high  $V_g$  polarization.