Yttrium-induced phase-transition technology for forming perfect ohmic contact in two-dimensional MoS_2 transistors

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Abstract

The van der Waals (vdW) strategy is promising for overcoming the Fermi pinning challenge in two-dimensional (2D) transistors. However, the lack of advanced-node lithography-compatible methods hinders wafer-scale integrated manufacturing of vdW contacts. We report a yttrium-doping-induced phase-transition technology for converting semiconducting trigonal prismatic (2H) into heavily doped metallic octahedral (1T) MoS2 to achieve suitable vdW band alignment and ideal ohmic contacts. This Y-doped 1T-MoS2 is a vdW metallic buffer, and it improves carrier transfer efficiency from the metal electrode to 2H MoS2. We developed a solid-state-source three-step doping method (plasma-deposition-annealing) and achieved Å-thickness surface doping with yttrium atoms replacing sulfur atoms in the top surface of MoS2, thus forming self-aligned Y-doped 1T-MoS2 vdW ohmic contacts lithographically patterned in the source and drain regions. We fabricated 10-nm MoS2 FETs with Y-doped 1T-MoS2 vdW contacts in 2-inch wafers exhibiting nearly ideal ohmic contact with an ignorable Schottky barrier, achieved the smallest contact-resistance Rc in all 2D TMD FETs (less than 117-ohm micrometers) and a total-resistance (235-ohm micrometers) more than three times smaller than those of the best-reported 2D n-type FETs (greater than 800-ohm micrometers), showing high performance with an excellent on-current density of 1.22 milliamperes per micrometer at a small drain voltage of 0.7 V, a high ballistic ratio of 80%, and a record transconductance of 3.2 millisiemens per micrometer.

One-sentence Summary

Solid-state-source yttrium-doping-induced phase-transition technology enables wafer-scale 10-nm ballistic MoS_2 FETs to approach the ideal ohmic contact and performance limits.

Main Text

Silicon technology is quickly approaching its fundamental limits at the sub-10 nanometer node predicted by the International Roadmap for Devices and Systems (IRDS)[1]. Further scaling of field-effect transistors (FETs) requires new channel materials[2-12]. Two-dimensional (2D) semiconductors have two intrinsic electronic advantages, ultrathin bodies, and high carrier mobilities[13-18], which allow better electrostatic control and on-state performance in short-channel FETs[19-24]. However, the high contact resistance resulting from the Fermi-pinning effect introduced by nonideal interfaces through conventional metal physical vapor deposition, is one of the main obstacks limiting the on-state performance of 2D transistors[25-30]. Van der Waals contact can in principle effectively avoid Fermi pinning, and many attempts have been made to improve the contact, such as using mechanical transfer of metal films[31,32], low-thermal deposition (indium, semimetal bismuth, etc.)[33-35], and contact phase transition through laser-induced or chemical treatments [36,37]. But, the total-resistances of all 2D transistors are still greater than 800 ohms per micrometer, and this does not meet the standard for commercial advanced-node silicon transistors (250-ohm micrometers by IRDS)[1], and wafer-scale advanced-nodes lithography-patterned van der Waals contacts is desired.

We first examine the mature structure of commercial silicon transistors, aiming to find a method with which to realize wafer-scale ohmic contact engineering in 2D electronics. In a commercial silicon transistor, the contact structure is sophistically designed to decrease the contact resistance, which includes the metal electrode, heavily doped source and drain extension regions, and a crucial metal silicide thin layer, such as TiSi or CoSi, which acts as a buffer between the metal electrode and heavily doped silicon, as shown in Fig. 1a[1,38], thus improving the carrier transfer efficiency and decreasing the series contact resistance. The silicides are formed by alloying a surface silicon layer through the deposition of an ultrathin metal layer and annealing. This classical structure and the corresponding standard silicide process have always accompanied the scaling of silicon transistors, which have followed Moore's law from the micrometer nodes in the 1970s to the state-of-the-art sub-10 nm nodes today. In this work, we explore a suitable metallic 2D buffer layer sandwiched between the metal electrode and the 2D semiconductor, which plays a role similar to that of the "silicide" structure in silicon transistors to improve the carrier transfer efficiency, as illustrated in Fig. 1b. This metallic 2D buffer is formed with a mechanism that we named "yttrium-doping-induced phase-transition technology" and is fabricated through a phase transition in homogenous 2D materials in locally lithography-patterned source and drain regions. The van der Waals interface between this metallic 2D buffer and 2D semiconductor avoids lattice degradation and does not introduce additional Fermi pinning. During the preparation of this contact, we developed a wafer-scale three-step Y-doping integrated process named "plasma-deposition-annealing" as a potential way to achieve Å-thickness ultrathin doping and Y-doping-induced 1T phase transition in the local source and drain regions defined through lithography patterning (note: conventional ion implantation gives doping depths of not less than 5 nm, which is inapplicable to surface doping in low-dimensional semiconductors)[39,40]. Then, we adopted this Y-doping-induced phase-transition van der Waals ohmic contact engineering to fabricate 10-nm gate length MoS_2 transistors in 2-inch CVD wafers. The scaled MoS_2 FETs exhibit the smallest contact-resistance R_C of less than 117-ohm micrometers in all 2D TMD FETs, a total-resistance of 235-ohm micrometers, which is more than three times smaller than the best-reported 2D n-type FETs (over 800-ohm micrometers), a large on-current density of 1.22 milliamperes per micrometer at a small drain voltage of 0.7 V, and more importantly, a record transconductance of 3.2 millisiemens per micrometer.

In some previous reports, the 2H-to-1T phase transitions of transition metal dichalcogenides (TMDs) in source and drain regions seemed to be the closest 2D metallic buffer strategy, including laser-induced, plasma-induced or chemical lithium ion-induced[36,37,41]; unfortunately, however, the Fermi levels of all the 1T metallic phase TMDs (MX_2, M=Mo, W; X= S, Se, Te) lie in the middle of the bandgaps of their corresponding homologous 2H semiconducting phase TMDs, which inherently causes a large Schottky barrier between the 2H phase and 1T phase TMDs (Fig. 1c) [42-47]. This occurs because the total number of conduction and valence electrons is conserved during the phase-transition process, so the Fermi level shifts only slightly before or after the phase transition. Therefore, introducing suitable dopants into 1T phase 2D semimetals is required to provide adequate excess electrons or holes and thus move the Fermi level of the 1T phase 2D semimetals to become higher than the conduction band minimum (CBM) or lower than the valence band maximum (VBM) of 2H phase 2D semiconductors to form the appropriate

band alignment and thus the ideal ohmic contact. Here, we choose the rare-earth element yttrium (Y) as the dopant for 2D MoS_2, and density functional theory (DFT) results show that the configuration of Y atoms replacing S atoms requires less formation energy (1.42 eV) and was more stable than that of Y atoms replacing Mo atoms (1.67 eV). Fig. 1d shows the band structure of the Y-doped 1T-MoS_2 obtained by DFT, which confirms the zero-bandgap semimetal characteristic with the CBM and VBM coinciding in the Brillouin zone. The band structures of intrinsic 2H-MoS_2 and 1T-MoS_2 are shown in Extended Data Fig. 1. Our DFT calculations show that when increasing the Y atom doping density to nearly 8%, adequate excess electrons are added to elevate the Fermi level of 1T phase 2D MoS_2, causing the work function of Y-doped 1T-MoS_2 (4.0 eV) to be smaller than the electron affinity of intrinsic 2H-MoS_2 (4.3 eV); thus, an ideal ohmic contact at the junction of Y-doped 1T-MoS_2 and 2H-MoS_2 is predicted theoretically. In comparison, the work function of the intrinsic metallic 1T-MoS_2 is 5.1 eV, and the Fermi level is located in the middle of the band gap of semiconducting 2H-MoS_2, causing a larger Schottky barrier (Fig. 1c). In addition, compared to conventional metal contacts (such as Ti, etc.), which induce significant metal-induced gap states (MIGS), semimetallic Y-doped 1T-MoS_2 in contact with 2H-MoS_2 has negligible MIGS and thus almost no additional Fermi pinning; it benefits from the native ideal van der Waals interface and much smaller density of states (DOS) for the semimetal at the Fermi energy level (Fig. 1e). Furthermore, to understand how Y-doping affects the dynamic mechanism of the phase transition, the nudged elastic band (NEB) method was adopted to calculate the energy barrier for the phase transition from the 2H to the 1T structure of MoS_2, as shown in Figs. 1f and 1g. The result shows that the barrier from 2H-MoS_2 to 1T-MoS_2 is 1.57 eV. By comparison, the barrier from 2H-MoS_2 to Y-doping-induced 1T-MoS_2 (Y-T-MoS_2) is reduced to 0.34 eV when some S atoms are substituted by Yatoms. This indicates that Y atom doping favorably induces the phase-transition process since the smaller energy barrier in the Y-doped system means that the 2H-to-1T phase transition would occur more easily. On the other hand, there is a large energy difference between intrinsic 1T-MoS_2 and Y-T-MoS_2. Note that 1T-MoS_2 is a metastable metallic phase, and its structural energy is 0.83 eV higher than that of the original stable-phase 2H-MoS_2, meaning possible reversion into 2H when undergoing the following device fabrication process. After Y-doping, the structural energy of Y-T-MoS_2 decreases to approximately 0.8 eV lower than that of intrinsic 1T-MoS_2 and thus forms stable-metallic-phase Y-T-MoS_2. Therefore, Y-doping is an effective strategy for achieving reliable ohmic contact, not only inducing the phase transition and stabilizing the 1T-metallic-phase but also elevating the Fermi level of 1T-MoS_2.

Next, we consider to find a fabrication process to achieve Y-doping into the MoS_2 structure. Note that local doping in 2D materials in the source and drain regions through lithography patterning is extremely difficult and has not been reported thus far. This is because the atomic 2D materials are too thin to use the normal ion-implantation and dopant-activation process, and sub-5 nm-thick ion-implantation engineering is not yet achieved in Foundries[39,40]. Here, we have developed a three-step process called plasma-deposition-annealing (PDA) method to achieve yttrium doping in the surface layer of MoS_2 (Fig. 2a). First, the patterned local contact areas were treated with low-power (9 watts, 15 seconds) argon soft plasma to modify the contact interface and generate active sites. This low-power soft plasma filtering of

energetic particles induces trace amounts of sulfur vacancies on the surface of the top-layer MoS_2 without damaging the overall lattice of the 2D MoS_2. Next, a 1/5/7 nm-thick Y/Ti/Au stacked metal was deposited by electron beam evaporation in high vacuum (<1×10^{-8} Torr), and the 1 nm-thick active metal Y was used as a solid-state doping source. Finally, Y atoms diffused toward active sites of the plasma-induced sulfur vacancies and were activated in the top layer of MoS_2 using high-temperature annealing (250 ℃ for 30 min) in an inert gas environment. Due to the utilization of hyperfine patterned structures, great thermal stability after annealing, and all-solid-state nature, this PDA doping process is compatible with advanced-node wafer-scale integration.

Fig. 2b shows optical images of wafer-scale 2D MoS_2 films used to fabricate our transistors grown by layer-by-layer epitaxy on sapphire substrates[48]. High-angle annular dark field (HAADF) scanning transmission electron microscopy (STEM) imaging show a clear lattice structure and atomically clean and sharp interfaces, confirming the high quality of the MoS_2 films (Fig. 2 and Extended Data Fig. 2). Compared to monolayer MoS_2, trilayer MoS_2 has a smaller bandgap, a smaller effective mass, and higher thermal velocity and mobility, making it more suitable for use as a channel material in high-performance electronics[20,48]. Therefore, the devices focused on in this work are mainly based on high-quality trilayer MoS_2 channels. We conducted yttrium doping into MoS_2, and the STEM image and electron energy-loss spectroscopy (EELS) maps in Figs. 2c-e demonstrates the cross-sectional atomic structure and elemental composition of Y-doped 1T-MoS_2. Each layer of intrinsic MoS_2 is composed of a layer of Mo atoms and two layers of S atoms above and below, and the Mo atoms appear brighter than the S atoms in the STEM image due to the different atomic numbers (Z-contrast). After the yttrium-PDA process, the uppermost S atoms of MoS_2 were partially replaced by bright Y atoms (Fig. 2c, right), and this was further confirmed by elemental analysis, which showed a significant Y element signal in the top layer of MoS_2 (Fig. 2d, e), which provides strong evidence for Y-doping and partial replacement of top surface S atoms. After the selective removal of excess Y metal by a wet process, Raman spectroscopy and X-ray photoelectron spectroscopy (XPS) were used to exhibit the following significant differences between the Y-doped 1T-MoS_2 and intrinsic 2H-MoS_2: i) The Y-doped MoS_2 showed a significant Y XPS signal (different from the pure Y metal binding energy) after removal of the excess Y metal from the surface (Fig. 2f, left), which further proved that yttrium atoms were doped and activated in MoS_2; ii) The XPS peaks for both Mo and S were shifted in the direction of lower energies after Y doping, which again provided strong evidence for the Y-doping-induced metallic 1T phase transition (Fig. 2f, middle)[37,41,49-52]. In addition, the XPS spectra obtained for the surface of the Y, MoS_2, and Y-doped MoS_2 samples all had C 1s peaks corrected to 284.8 eV (Fig. 2f, right); iii) The Y-doped MoS_2 had three more new peaks, J_1 (167 cm^{-1}), J_2 (227 cm^{-1}), and J_3 (334 cm^{-1}), in the Raman spectrum, demonstrating the characteristics of the 1T semimetal phase (Fig. 2g)[37,41,49-52]. Fig. 2h shows four typical output characteristics of ballistic MoS_2 FETs after annealing activation at different temperatures, which corresponds to no activation (at room temperature, RT), partial activation (at 150 °C and 200 °C), and full activation (at 250 °C) of the yttrium dopants. The unannealed MoS_2 FET exhibited an extremely high Schottky barrier (total resistance of

~1×10^5 Ω·μm, bottom blue curve), while the MoS_2 FET with full dopant activation achieved the desired ohmic contact (total-resistance of ~235 Ω·μm, top red curve) for ballistic transistors. The electrical transport measurement provides the most direct evidence, and it also showed that the device containing Y-doped 1T-MoS_2 as the channel exhibited semimetallic modulation with an on/off current ratio of less than 10, while the device with an intrinsic semiconducting 2H MoS_2 channel exhibited an on/off current ratio of greater than 10^8 (Fig. 2i).

Fig. 3a shows a schematic drawing of the 2D MoS_2 FET structure used in this work. A cross-sectional STEM image and the corresponding EELS map of our ballistic MoS_2 transistor are shown in Figs. 3b and 3c, and these results confirm the location of the 2-nm-thick trilayer MoS_2 channel, the 10-nm channel length (10-nm back-gate length and 5 nm top-gate length), 2.6-nm-thick HfO_2 dielectrics for both the top and bottom gates formed by atomic layer deposition (ALD), the source/drain/gate electrodes, and a thin layer of yttrium in the contact area. The dual-gate leakage currents are shown in Extended Data Fig. 3.

Our ohmic-contact ballistic 10-nm MoS_2 FET exhibited a constant on-state current over a wide temperature range from 300 K to 100 K (Fig. 3d) in the transfer characteristics, which is the first time that this has been observed in short-channel MoS_2 transistors, providing strong evidence of the near-zero Schottky barrier in our devices[53]. Moreover, the Schottky barrier height (SBH) was extracted via Arrhenius plots from the temperature-variable transfer characteristics of our ballistic FET and showed to approach the theoretical limit (Extended Data Fig. 4). In a typical ballistic unoptimized Schottky-barrier MoS_2 FET using a conventional Ti/Au metal contact, there exist two slopes below the threshold in the FET transfer characteristics determined at a low temperature of 100 K (Fig. 3e and Extended Data Fig. 5). The lower part consists only of thermal emission (TE) current determined by the channel potential, and it exhibits a smaller subthreshold swing (SS)[54]. The upper part consists of the thermal field emission (TFE) current and shows poor SS due to gate-modulated Schottky barrier tunneling[26]. Furthermore, the case of the intrinsically undoped 1T-MoS_2 contact using only the argon plasma-induced phase transition, as reported in the literature (after 40 s treatment), also exhibits a large Schottky barrier as shown for comparison in Fig. 3e (gray hollow dot) and Extended Data Fig. 5 [41,55]. Although the ideal van der Waals interface without Fermi pinning makes the undoped 1T-MoS_2 contact better than the conventional Ti/Au contact in MoS_2 FETs (purple hollow dot, Fig. 3e), the large Schottky barrier between undoped 1T-MoS_2 and 2H-MoS_2 still reduces the current to a much lower level than that in the case of the Y-doped 1T-MoS_2 (blue solid dot, Fig. 3e).

Typical saturation output characteristics (with maximum V_{GS}) of our ballistic MoS_2 transistors, compared with those of other reported sub-50 nm short-channel 2D TMD transistors, are shown in Fig. 3f[19,20,34,35,56-61], and more details of our ballistic FETs are shown in Extended Data Figs. 6 and 7. The total resistance of our ballistic MoS_2 transistors is more than three times smaller than those of the reported optimum sub-50 nm 2D n-type FETs, which allows a standard high current density of 1 mA/μm at much lower drain voltages below 0.5 V. Previous reports have consistently proven that the

transmission line method (TLM) is not always accurate for extracting the contact resistance of a 2D transistor because of fluctuations in the large-channel resistances[4,62]. Since the total contact-resistance $2R_C$ is approximately equal to the total-resistance R_{total} in a ballistic transistor, extracting the total-resistance in ballistic 2D FETs is thus a more reliable method than TLM for evaluating the contact resistance, as we have shown here [28,31-34,56,63-65].

The process flow for wafer-scale 2D MoS_2 FETs is depicted in Fig. 4a, and SEM images of an array of FETs based on the CVD trilayer MoS_2 film and a typical 10-nm gate length dual-gate transistor are shown in Fig. 4b. Our ballistic MoS_2 transistors exhibit advances in main electronic merits and are superior to the best-performance 2D TMD transistors previously reported (Fig. 4c)[20,34,56]. Fig. 4d shows the total resistances of fifty representative ballistic FETs, and the corresponding saturation output characteristics are shown in Extended Data Fig. 8; these demonstrate that our FETs have three times smaller total-resistance values than other 2D transistors, and the lowest total-resistance R_{total} can reach 235 Ω·μm (Fig. 4d), corresponding to a contact-resistance Rc less than 117 Ω·μm ($R_{total} = R_{CH} + 2R_C$). Fig. 4e shows typical transfer characteristics for our ballistic MoS_2 FETs (L_G=10 nm for the left, and L_G=20 nm for the right) exhibiting ideal switching characteristics, including a SS of 63 mV/decade near the Boltzmann limit, a negligible drain-induced barrier lowering (DIBL) of 14 mV/V, and a large on/off current ratio of $>10^8$, which satisfy the requirements for commercial standard-performance (SP) integrated circuits[1]. In addition, more typical electric data for ballistic transistors are shown in Extended Data Figs. 6 and 7, and the typical hysteresis of our ballistic FET is shown in Extended Data Fig. 9. To benchmark the overall switching behaviors of 2D FETs, we plotted the SS-I_{DS} of our ballistic MoS_2 FETs as well as those of other reported 2D sub-50 nm short-channel FETs[19,56-61]. Our 20 nm ballistic MoS_2 transistors show an ideal SS close to the Boltzmann limit of 60 mV/decade across over four orders of magnitude for I_{DS}, which is more than two orders of magnitude larger than that for other sub-50 nm short-channel 2D transistors. The transconductance determines the intrinsic gain and switching speed of a FET and is a more practical parameter for evaluating performance than the saturation current. In our MoS_2 FETs, a scattering-free ballistic channel is combined with an ideal ohmic contact and an ultrathin 2.6 nm-HfO_2 dual-gate structure to provide record transconductance (3.2 mS/μm) and transconductance rates (13 mS/μm·V), which are nearly an order of magnitude larger than those of other reported short-channel 2D TMD FETs (Figs. 4g and 4h)[19,20,34,56-61]. Fig. 4i shows the output characteristics of a typical 10 nm MoS_2 FET and its corresponding standard virtual source model fitting, and the extracted room-temperature ballistic rate of our typical 10-nm MoS_2 FET is close to 80%, which is significantly higher than those of all previously reported silicon-based and other 2D transistors (Fig. 4j)[66-68]. The excellent overall electrical characteristics of our ballistic FETs are attributed to the low contact resistance that results from the van der Waals Y-doped 1T-MoS_2 ohmic contact strategy.

In summary, we propose a solid-state-source doping-induced 2D phase-transition technology that is compatible with advanced Å-nodes; it achieves reliable vdW ohmic contact for wafer-scale n-type MoS_2

transistors, and this strategy can in principle be extended to other 2D material systems. There remain, however, important challenges hindering the transfer of 2D semiconductor transistors from the laboratory to industry, these include CVD growth of wafer-scale single-crystal 2D materials, higher-quality gate stack structures, and complementary transistors fabricated with monolithic integration. Nevertheless, this work provides the first step toward pushing the switching and on-performance of wafer-scale ballistic 2D semiconductor transistors to the theoretical limit under ohmic contact, which confirms the practical potential of 2D semiconductors in large-scale integrated circuits of future nodes.

Declarations

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Materials And Methods

1. Layer-by-layer epitaxy of wafer-scale MoS_2.

A multisource chemical vapor deposition (CVD) system with three temperature zones, referred to as zones I, II, and III, was used for all MoS_2 growths. A typical growth process involved loading one high-purity (99.9%) sulfur source (15 g) into zone I and carrying it with Ar (40 sccm), while loading six MoO_3 sources (99.999%, 30 mg) into zone II and carrying it with Ar/O_2 (40/1.7 sccm) and loading single side polished 2-inch sapphire substrates with c-plane (0001) into zone III. For heterogeneous epitaxy (first MoS_2 layer growth, sapphire-MoS_2) of MoS_2 on 2-inch sapphire, the temperatures in zones I, II, and III were maintained at 120, 540, and 910 ℃, respectively, while for homogeneous epitaxy (top two layers growth, sapphire-MoS_2-MoS_2-MoS_2) of MoS_2, the temperatures in zones II and III were increased to 570 and 940 ℃, respectively. More details of the growth can be found in our previous work[48].

2. Transfer of MoS_2 films on dielectric/Si substrates.

Transfer of MoS_2 films was performed by using polydimethylsiloxane (PDMS, Dow Corning), which was made by mixing a ten-to-one weight ratio of prepolymer and crosslinker in a mold and curing at 100 °C

for four hours. During the transfer process, a customized mechanical transfer platform was used to press the prepared PDMS onto the sapphire grown with MoS_2, and the PDMS was stripped using a deionized water-assisted approach, thus transferring the MoS_2 film from the sapphire to the PDMS. Furthermore, the PDMS with the MoS_2 film was pressed onto the plasma-modified substrate (HfO_2/Si) using a mechanical transfer platform and stripped off. After transfer, the MoS_2 films were placed in a vacuum drying system for 6 hours to avoid moisture adsorption.

3. Device fabrication.

To prepare dielectric/Si substrates, highly doped bare silicon wafers were cleaned using a standard buffered oxide etch (BOE) process to remove polymer and oxide layers on the surface, then rinsed with deionized water. The cleaned substrates were quickly placed in the vacuum chamber of the atomic layer deposition (ALD, BeneQ TFS 200) for HfO_2 dielectric growth. The 2.6 nm thickness of the back-gated HfO_2 dielectric was grown using a high temperature of 230 ℃. In addition, the standard electron-beam lithography (EBL)/electron-beam evaporation (EBE)/lift-off processes were used in this work. Spin coating of electron beam resists, such as polymethyl methacrylate (PMMA) and hydrogen silsesquioxane polymers (HSQ), was followed by pattern preparation through an EBL system (Raith Voyager), metal deposition by EBE after development, and finally metal lift-off. Then, the MoS_2 films were transferred to the premade metal-mark substrate (2.6 nm HfO_2 dielectric/Si), and the substrate was modified with a low-power oxygen plasma for 120 seconds before transfer. An inductively coupled plasma (ICP) system was then used to dry etch the MoS_2 film into a banded structure using a hard mask. The source/drain electrodes were prepared by using double overlay exposure (more details can be found in our previous work[8]), and 10 nm source/drain electrode gaps were generated to define the channel length (i.e., back-gated length) of the ballistic MoS_2 FETs. As contacts for ballistic MoS_2 FETs, a Y/Ti/Au metal film stack of 1/5/7 nm thickness was used. To make injecting the solid-dopant source of the reactive metal Y easier, the contact area defined by the EBL system was treated with a low-power argon soft plasma (for 15 s) before contact metal evaporation. After annealing at 250 °C for 30 minutes under an inert gas atmosphere, the solid-dopant source Y diffused toward the upper layer of the MoS_2, resulting in Y-doping at the active sites induced by the pre-plasma. Under all metal lines and pads (Ti/Au of 5/120 nm) except the contact area, 60 nm-thick SiO_2 from HSQ (2%) was used to define the pattern through electron beam lithography (EBL) and to reduce leakage from the back gate. A few layers of Al atoms oxidized into 0.3 nm Al_2O_3 were used as the seed layer for the growth of the top-gated 2.6 nm HfO_2 dielectric with a growth temperature of 150 ℃, followed by growth of Ti/Au as the top-gated electrode defined by EBL. Finally, the PMMA defined by EBL was used as a mask to etch the thin-layer HfO_2 on top of the pad through the ICP system.

4. Characterization and Measurements

Optical images were taken using an optical microscope from Nikon, and the thickness of the layer-by-layer epitaxy of MoS_2 was determined by atomic force microscopy (AFM, Veeco Instruments Inc.

Dimension Icon) using tapping mode (Extended Data Fig. 2). Raman spectroscopy was performed using a spectrometer (Renishaw) with a laser wavelength of 532 nm at a laser power of 2.5 mW, and XPS (Thermo Fisher) was used in the binding energy analyses of our samples. For cross-sectional analyses of materials and devices, the sample was cut out from our chip using a double-beam focused ion beam (FIB, Zeiss Auriga Compact) system and transferred into the TEM grid with OmniProbe 200 nanomanipulators. Then, a high-resolution spherical aberration correction TEM (JEM-ARM200F) was used to obtain the cross-section scanning transmission electron microscopy (STEM) images and EELS maps of our samples. A Zeiss Sigma 300 SEM with inLens probes was used to obtain SEM images of our FETs. Electrical characterizations of the FETs were performed using parameter analyzers (Keithley B4200A and Agilent B1500), and the low-temperature transport of our ballistic FETs was measured using a Lakershare vacuum low-temperature probe station under a vacuum of 1.3×10^{-3} mbar.

5. Schottky barrier height extraction.

A thermionic-emission model was used to extract the Schottky barrier heights (SBHs) of 2D transistors in near-threshold or subthreshold regions. In this case, carriers inject to the 2D semiconductors occurred mainly through thermal emission below the flat-band voltage (V_{FB}), as shown by the following equation[31,69-71]:

$$I_{DS} = AA^{*}T^{3/2}exp\left[-\frac{\Phi_{SB}}{kT}\right] \qquad (1)$$

where I_{DS} is the source-to-drain current in the FET, A is the junction area, A^{*} is the Richardson constant, Φ_{SB} is the Schottky barrier, k is the Boltzmann constant, and T is the temperature. As a result, the formula for extracting the Schottky barrier from an Arrhenius diagram was[31,69-71]:

$$\mathrm{In}\left[\frac{I_{DS}}{T^{3/2}}\right] = -\frac{\Phi_{SB}}{kT} + c \qquad (2)$$

where c is a constant and Φ_{SB} is the slope within the Arrhenius plots. Based on Equations (1) and (2), the SBHs of the 2D FETs were extracted under various gate voltages. For an n-type 2D transistor, when the gate voltage is below the flat-band voltage ($V_{GS}<V_{FB}$), the device is in the subthreshold region (thermionic emission current), where the 2D channel resistance dominates devices and produces a significantly larger Schottky barrier height. In contrast, when the gate voltage is higher than the flat-band voltage ($V_{GS}>V_{FB}$), the superimposed tunneling current greatly affects the height of the extracted Schottky barrier[26], which exhibits a smaller SBH. Therefore, the SBHs at gate voltages equal to the flatband voltage were extracted for accurate contact evaluation.

6. Density functional theory (DFT) calculations

DFT calculations were performed using the projector augmented wave approach implemented with the VASP package. The electron exchange-correlation energy was described by the generalized gradient approximation (GGA) in the scheme of the Perdew-Burke-Ernzerhof (PBE) functional. The cutoff energy of the plane-wave basis was 500 eV. Optimization of atomic positions was performed until the forces were smaller than 0.02 eV/A, and the electronic self-consistent interaction was converged until the energy difference was less than 10^{-5} eV between two interaction steps. A vacuum space larger than 15 Å was added to the z directions of all 2D materials to prevent interactions between periodic images. The phase transition occurring between the 2H and 1T phases was calculated using the Nudge Elastic Band method with a force convergence of 0.03 eV/A.

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Figures

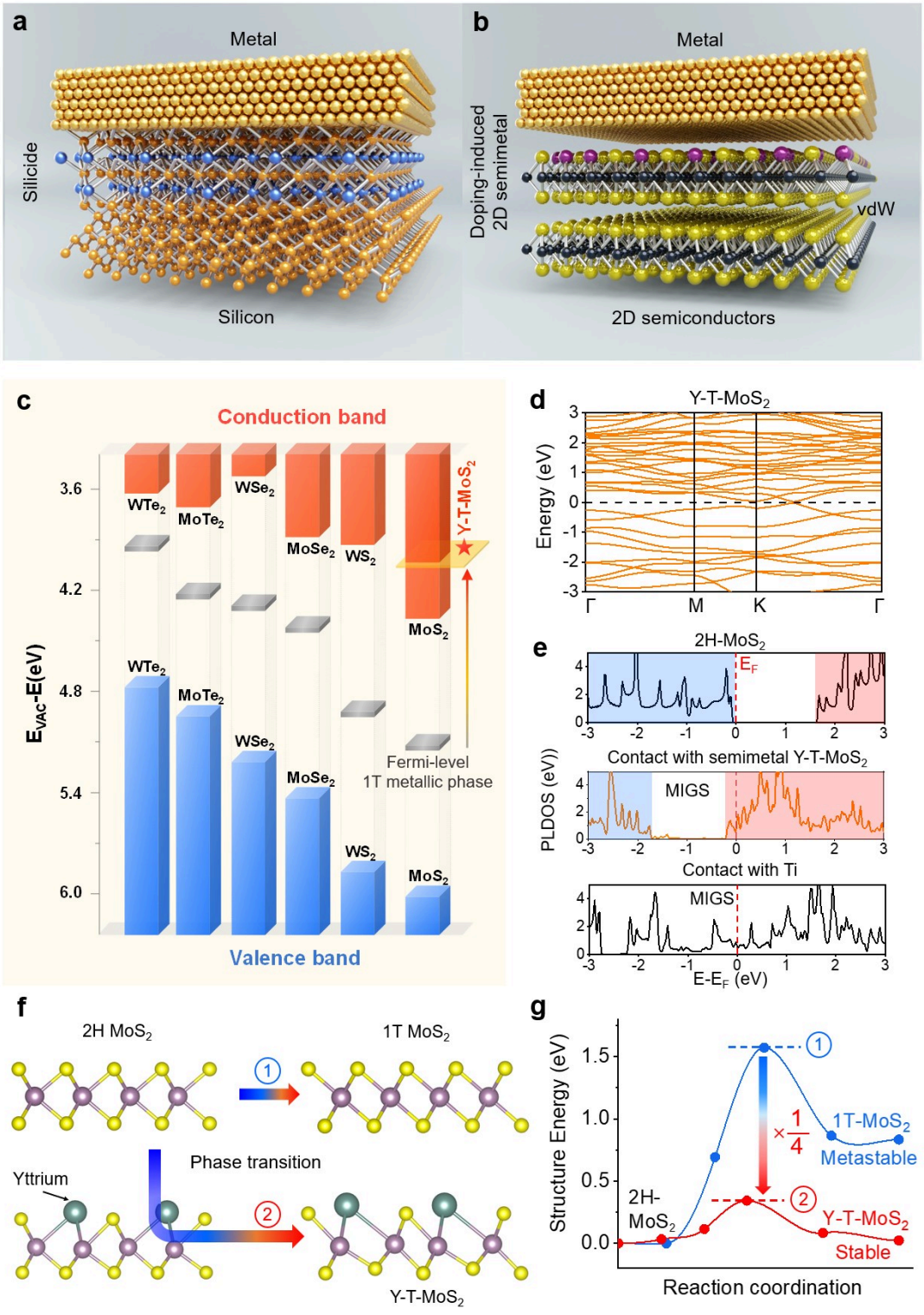

Figure 1

Illustration and theoretical calculations of phase transition and semimetal Y-T-MoS_2 ohmic contact. a, Schematic diagram showing an advanced-node commercial silicon-based transistor contact, with metal silicide introduced between the metal and silicon semiconductor to reduce the contact resistance. **b,** Ideal 2D transistor contact diagram, with a 2D semimetal inserted between the metal and the 2D semiconductor for Fermi-level depinning. **c,** Band alignment between 2D semimetals and 2D

semiconductors[42]. The red and blue squares represent the conduction and valence bands of the 2H-TMDs, respectively, and the gray planes represent the Fermi levels of the corresponding semimetal 1T-TMDs. **d,** Calculated band structure for Y-doping-induced phase-transition MoS_2 (Y atoms are substitutionally doped into the top layer of MoS_2). **e,** Projected local density of states (PLDOS) of MoS_2 before (upper panel) and after contact with metal Ti (lower panel) and semimetal Y-T-MoS_2 (middle panel). The light blue part represents the valence band, and the red part represents the conduction band. The Fermi level moves from inside the gap (before contact) to above the minimum value of the conduction band (after Y-T-MoS_2 contact). **f,** Illustration of the phase transition from the 2H to 1T structure of MoS_2, intrinsic (up) and Y-doping (low), and **g,** the corresponding required barrier energy calculated by the nudged elastic band (NEB) method.

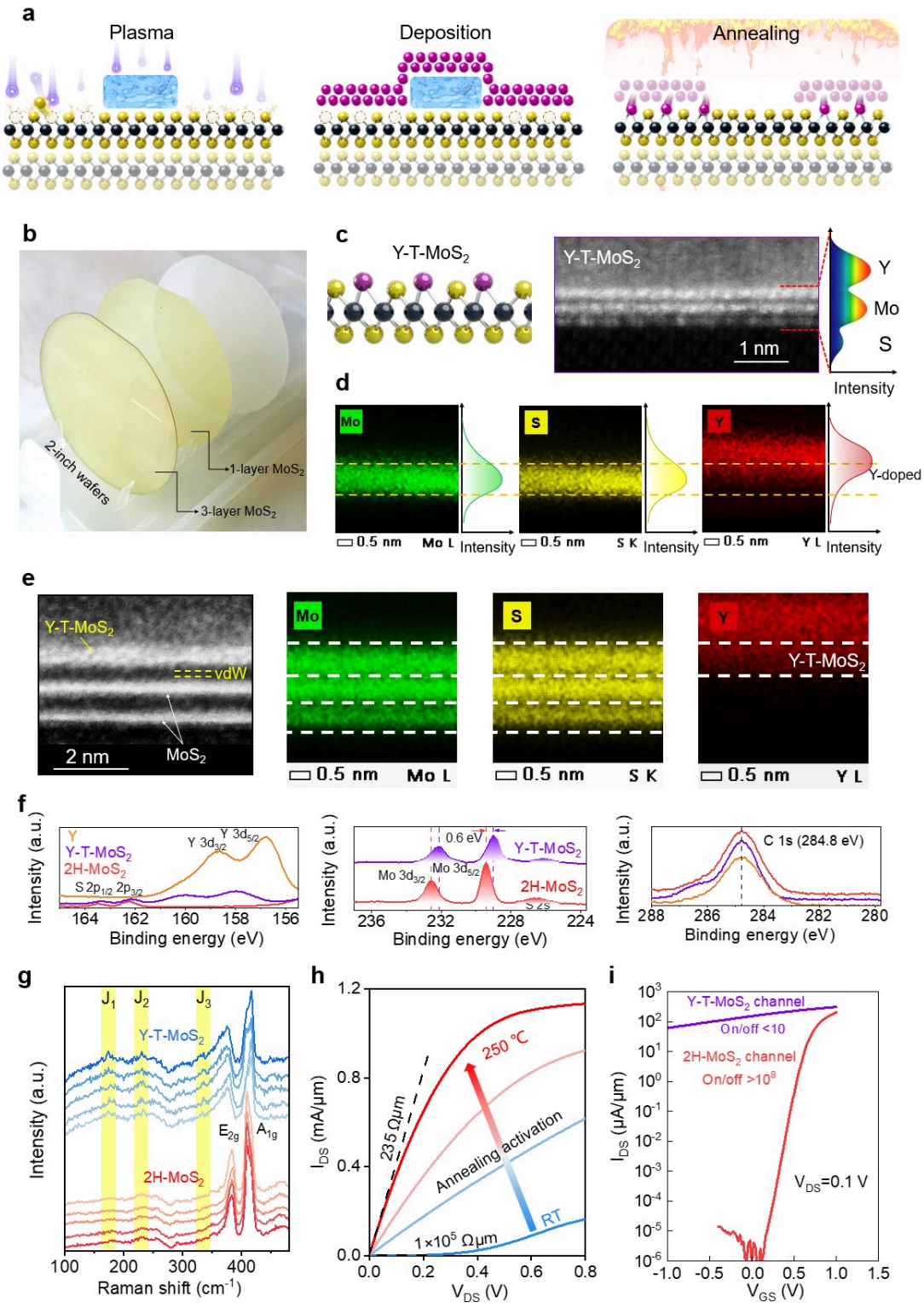

Figure 2

Characterization of doping-induced phase-transition technology. a, Schematic diagram of the plasma deposition-annealing (PDA) method for doping-induced phase transition. **b,** Photograph of 2-inch sapphire wafers covered with few layer MoS_2, including monolayer and trilayer MoS_2. **c,** Cross-sectional STEM image of the Y-doping-induced Y-T-MoS_2. The brighter atoms are Mo and Y, and the darker atoms are S (scale bar, 1 nm). Corresponding atomic structure is shown on the left. **d,** EELS maps showing the

presence and spatial distributions of Mo, S, and Y elements. The green, yellow, and red maps represent Mo, S, and Y elements. The spatial elemental maps show that Y atoms were clearly diffused into the MoS_2. Scale bar, 0.5 nm. **e,** Cross-sectional STEM images and EELS maps of Y-doping-induced phase-transition in trilayer MoS_2. EELS maps show the presence and spatial distribution of Mo, S, and Y elements in the trilayer structure. The green, yellow, and red maps represent Mo, S, and Y elements respectively. The spatial elemental maps show that Y was only doped into the uppermost layer of the trilayer MoS_2. Scale bar, 0.5 nm. **f,** XPS spectra showing the Mo, S, Y, and C (baseline) peaks and the shifts of the Y film (orange curves), intrinsic MoS_2 (red curves), and Y-doping-induced Y-T- MoS_2 (purple curves); a.u., arbitrary units. **g,** Comparison of Raman spectra of trilayer MoS_2 wafers before (red lines) and after (blue lines) Y doping. New peaks (J_1, J_2, and J_3) can be observed in the Y-doped trilayer MoS_2, confirming the occurrence of the phase transition. **h,** Typical output characteristics with the maximum gate voltage of ballistic MoS_2 FETs at different annealing activation temperatures, from bottom to top, room temperature (RT), 150 ℃, 200 ℃, and 250 ℃. This corresponds to states of no activation, partial activation, and full activation of the doped impurities. **i,** Transfer characteristics of ballistic FETs with the intrinsic MoS_2 channel (red curves) and the Y-doping-induced Y-T-MoS_2 (purple curves) channel. The weak gate modulation of the Y-T-MoS_2 channel FET is direct evidence of the semimetal mature of Y-T-MoS_2.

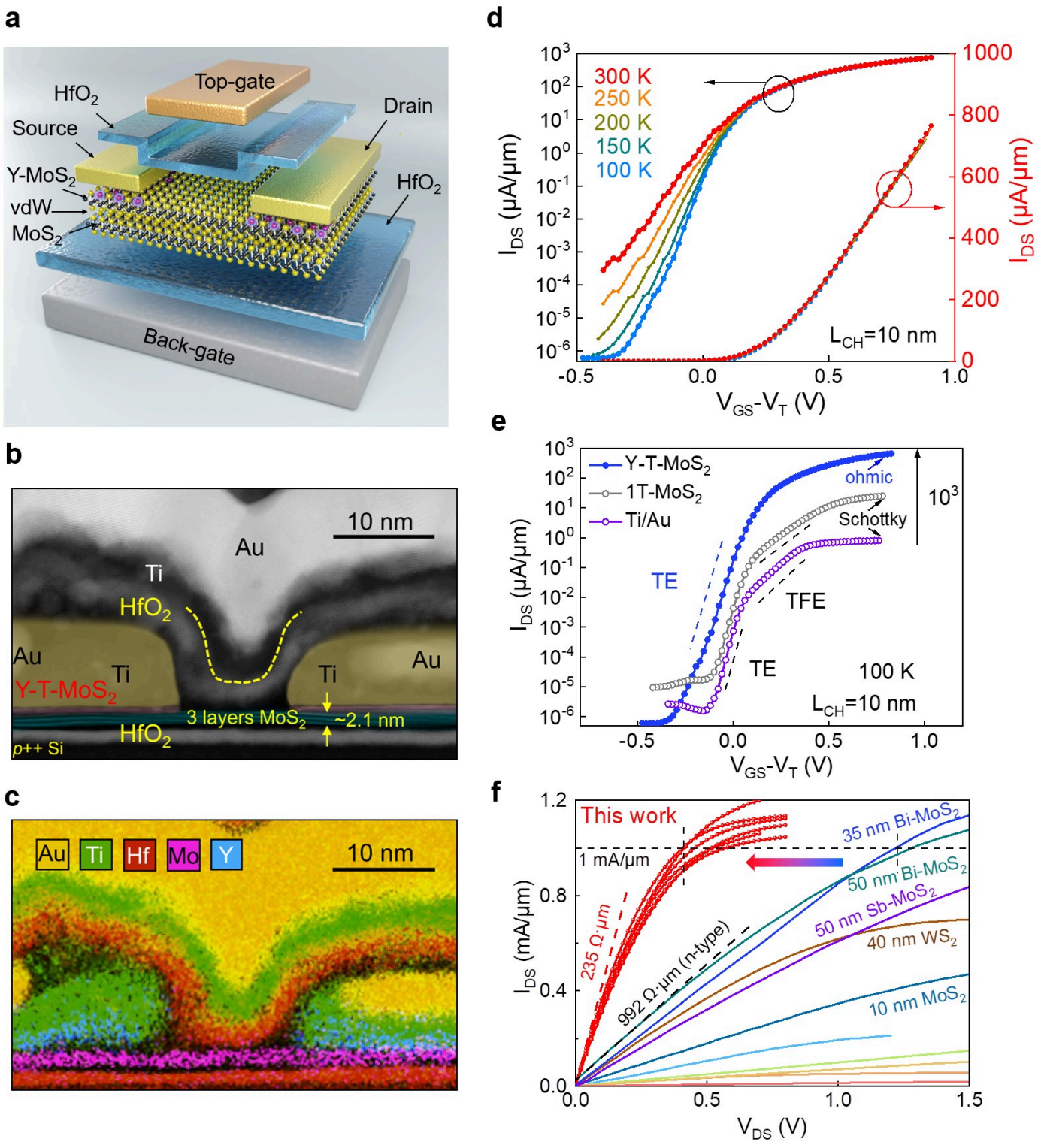

Figure 3

Structural and electric characteristics of ballistic MoS_2 FETs. a, Schematic diagram of a double-gate MoS_2 transistor with a semimetal Y-T-MoS_2 contact. The black, yellow, and purple balls represent Mo, S, and Y atoms, respectively. **b,** Cross-sectional STEM image of a ballistic 3-layer MoS_2 FET with a dual-gate and 2.6 nm HfO_2 dielectirc layers, showing a channel length of ~10 nm, top-gate length of 5 nm, and

back-gate length of 10 nm. **c,** EELS map showing the spatial distributions of yttrium, molybdenum, sulfur, titanium, gold, and hafnium elements, confirming the locations of the MoS_2 channel, Y-MoS_2 semimetal buffer, electrodes, and HfO_2 dielectric layers. **d,** Variable temperature transfer characteristics of a typical 10 nm gate length ballistic MoS_2 FET at temperatures from 300 K to 100 K. **e,** Transfer characteristics of ballistic MoS_2 FETs with three types of contacts measured at low temperatures of 100 K, including Y-T-MoS_2 vdW contact, argon plasma-induced undoped 1T-MoS_2 vdW contact, and conventional Ti/Au metal contact. **f,** Comparison of the saturation output characteristics and the total-resistances of our ballistic MoS_2 transistors and other reported n-type 2D sub-50 nm TMD transistors[19,20,34,35,56-61].

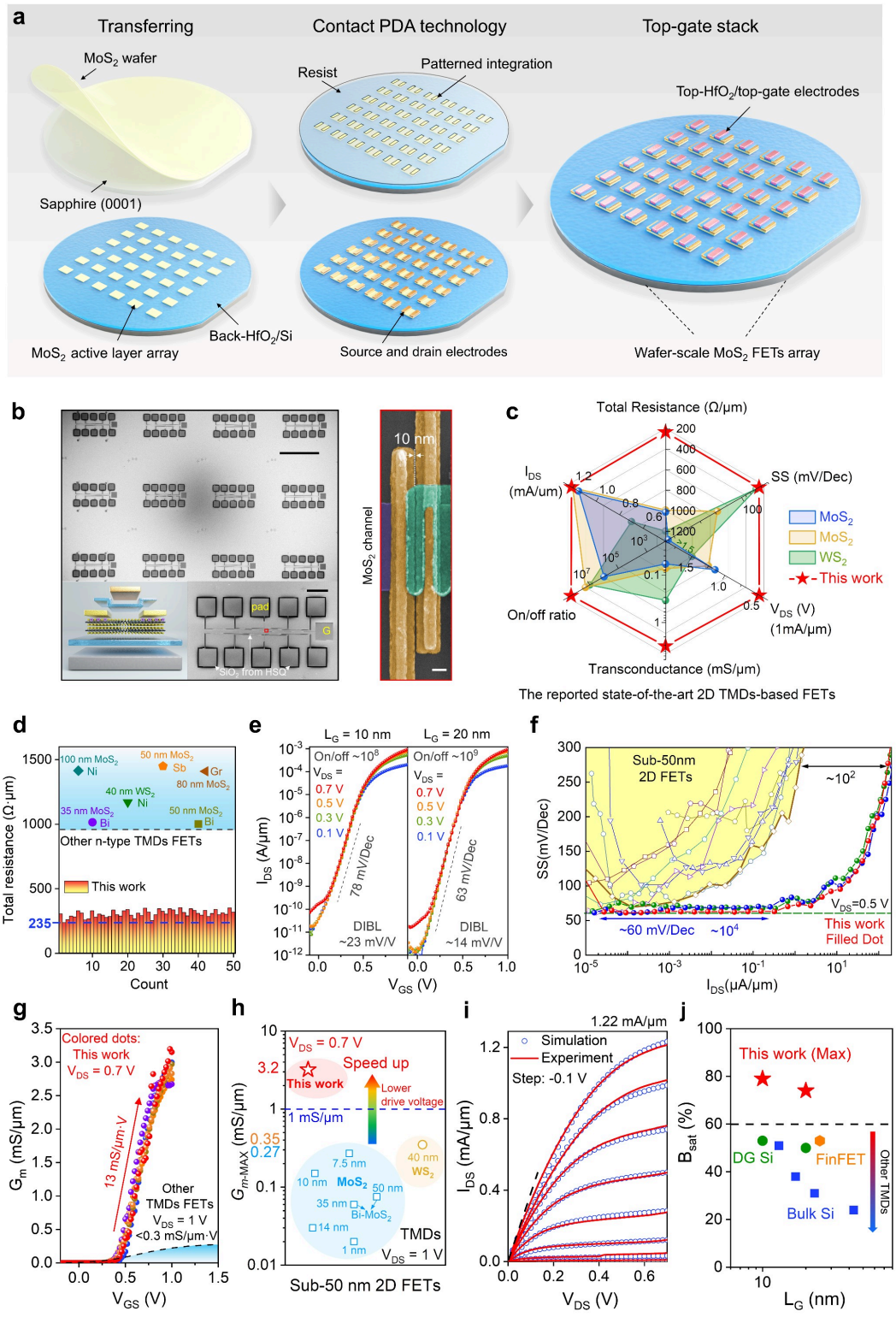

Figure 4

Wafer scale fabrication and comparison of MoS_2 FETs. a, Process flow diagram for preparing wafer-scale ballistic MoS_2 FETs with doping-induced Y-T-MoS_2 contacts. **b,** SEM images of a fabricated dual-gate ballistic MoS_2 FET array (scale bar, 250 nm) and a typical 10 nm gate length MoS_2 FET (scale bar, 100 nm). Among the false colors, gold is the contact electrode, cyan is the gate electrode, and purple is

the MoS_2 channel. The inset shows a schematic diagram and an SEM image of the MoS_2 FET (scale bar, 40 μm). **c,** Radar plot of the electric performance of our ballistic MoS_2 FETs versus other reported short-channel TMD FETs[20,34,56]. Red stars indicate our FETs, and light blue, light yellow, and light green areas indicate other reported advanced TMD FETs. **d,** The total-resistances extracted from output characteristics of 50 representative ballistic MoS_2 FETs. The colored solid dots in the upper area represent the total resistance of all other n-type sub-50 nm TMD FETs. **e,** Transfer characteristics of our typical ballistic MoS_2 FETs with 10 nm (left) and 20 nm (right) gate lengths at V_{DS}= 0.1, 0.3, 0.5, and 0.7 V. **f,** Comparison of I_{DS}-SS plots of our three typical ballistic MoS_2 FETs (solid dots) with other published sub-50 nm short-channel 2D FETs (hollow dots) [19,56-61]. **g,** Transconductances and transconductance rates of six typical ballistic MoS_2 FETs. The colored dots represent our FETs, and the blue area represents other 2D TMD FETs[19,20,34,56-61]. **h,** Peak transconductance comparison of our ballistic MoS_2 FETs at V_{DS}=0.7 V and other sub-50 nm 2D TMD FETs at V_{DS}= 1 V. The light red, light blue, and light yellow areas represent our ballistic MoS_2 FETs, other reported MoS_2 FETs, and reported WS_2 FETs[19,20,34,56-61]. **i,** Comparison of the virtual source model fitting (hollow circles) and measured data (lines) for output characteristics from a typical 10-nm gate-length MoS_2 FET. **j,** Benchmarking the room-temperature ballistic ratios of our MoS_2 FETs with those of short-channel FETs, including bulk silicon FETs, silicon FinFETs, dual-gated silicon FETs, and other 2D FETs[66-68].

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