An Optical Logic Gate Based On 2-Dimensional Photonic Crystals with High Operating Contrast Ratio And Fast Response Time

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Abstract

An optimized all-optical "NAND" logic gate is studied analytically. The particular characteristic of this logic gate is that it is based on photonic crystals, it consists of a resonator coupled with two waveguides on a silicon substrate. The operating wavelength is equal to 1.55μm which represents the telecommunication wavelength, the switching power of the optical logic gate studied is 1.693 kw /μm2 its response is independent of the response of the resonator when the power intensity of the optical waves is lower than the resonance wavelength, the light will be coupled in the waveguides, in the opposite case the light propagates in the waveguide of the bus.

1. Introduction

Nowadays, the most common application of optical technology in fiber-optic telecommunication networks is for high-speed connections such as server racks, terminal connections, WANs [1]

Photonic crystals are effective structures for making new artificial materials with controlled light characteristics for special functions [2]. It is necessary to mention that, before the development of photonic crystals, the control of light in dielectric environments was impossible, and the only way to use the properties of light was in a reflected state against different materials [3,4]. Studies of photonic crystal based logic gates are divided into broad categories of photonic crystal interference based logic gates, photonic crystal resonator based logic gates and photonic crystal self-collimating logic gates Salmanpour et al (2014) [5].

The realization of ultra-fast processing in all-optical information and computation, based on micro-nanometer scale integrated optical devices, is one goal of integrated optical technology development [6,7].

Manufacturing and implementation of nanoscale integrated optical devices are some of the main applications of photonic crystals. Logic devices are one of the essential components of optical computing systems and ultra-fast information processing. Logic gates can be built on the effects of the photonic band gap, waveguides, and severe light limitations in photonic crystal microcavities [8,9].

Lately, various designs have been proposed for the implementation of photonic crystal-based grids [10]. These structures have been proposed to improve the characteristics of photonic crystal logic gates, including reducing power consumption, increasing bandwidth, and increasing contrast ratio. They also use different materials and semiconductors to implement and improve the properties of crystal-based photonic logic gates. Some of these structures implement two gates simultaneously [11]. During this decade, other designs were introduced that used the multimode interference feature to make crystal-based photonic logic gates. These schemes include the one proposed by Ishizaka et al (2010) [12] to implement AND and XOR gates based on multimode interference.

2. Materials And Methods

The FDTD method is based essentially on the direct resolution of Maxwell's equations in their differential form [13]. Recall that in the case where the material is isotropic, non-dispersive, without source and transparent the Maxwell differential equations in a Cartesian reference frame (x, y, z), are written [14]:

$$\frac{\partial Ex}{\partial t} = \frac{1}{\epsilon}(\frac{\partial Hz}{\partial y} - \frac{\partial Hy}{\partial z})$$

1

…….

$$\frac{\partial Ey}{\partial t} = \frac{1}{\epsilon}(\frac{\partial Hx}{\partial z} - \frac{\partial Hz}{\partial x})$$

2

…….

$$\frac{\partial Ez}{\partial t} = \frac{1}{\epsilon}(\frac{\partial Hy}{\partial x} - \frac{\partial Hx}{\partial y})$$

3

…….

$$\frac{\partial Hx}{\partial t} = \frac{1}{\mu}(\frac{\partial Ey}{\partial z} - \frac{\partial Ez}{\partial y})$$

4

…….

$$\frac{\partial Hy}{\partial t} = \frac{1}{\mu}(\frac{\partial Ez}{\partial x} - \frac{\partial Ex}{\partial z})$$

5

…….

$$\frac{\partial Hz}{\partial t} = \frac{1}{\mu}(\frac{\partial Ex}{\partial y} - \frac{\partial Ey}{\partial x})$$

6

…….

Note that the spatial variations of the magnetic components "H" govern the temporal evolution of the eclectic field components "E" and vice versa (vice versa) [15]. In the case of two-dimensional periodic photonic crystals (along the two directions (x and y) and invariant along the third (z)), the reduction of this system in the plane (x,y) makes it possible to subdivide it into two independent subsystems [16]. One involves the electric field components of the plane (Ex, Ey) and the component normal to the plane (Hz), and the other involves the remaining field components (Hx, Hy, Ez), giving rise to the two polarizations: transverse magnetic "TM" and transverse electric "TE" respectively [17,18].

3. Design Of The Proposed Optical Logic Gate “nand”

The studied structure is a structure based on photonic crystals with a square array of glass rods, which has a refractive index equal to 3.1 in air. The radius of the rods is r = 0.19*a, where a = 640 nm is the dielectric constant of the array. Figure 01 represents the band diagram in TE polarization, it is clear that the structure has a photonic bandgap region between $0.32 < a/\lambda < 0.44$ in the normalized frequency domain, which gives a range of lengths of waves between $1489nm < \lambda < 2065$ nm. This means that optical waves in this wavelength region will not scatter inside the fundamental structure.

The composition of our structure is a resonant ring between two waveguides (bus and drop). The bus waveguide was created by removing a full row of dielectric rods in the X direction, also removing rods in the Z direction, to create the drop waveguide. For the resonant ring, a 7*7 dielectric rod array was removed, then a 12-fold quasicrystal was replaced in the center of the structure. The latter is composed of three ports; input port (A), direct transmit port (B) and direct bypass port (C). Optical waves enter the structure through port A and exit through port B, but at the desired wavelength (λ = 1.55μm), the optical wavelengths drop to drop the waveguide at through the resonant ring and head towards port C. Figure 02.

Figure 02: the proposed structure of NAND logic gate

incident light from the bias port will penetrate inside the structure, and the output state of the NAND gate will be controlled through ports A and B. The logical NAND gate is OFF when its two logic inputs A and B are enabled (A = B = 1), otherwise it will be ON.

4. Results

The proposed NAND optical logic gate has four 4 different input states, we fed the BIAS, A and B ports with a continuous wave λ = 1.55μm with a power of 0.5 $kw/\mu m^2$. In all 4 states, the activation wave should be on. When both input ports are OFF (A = B = 0), the optical power near the resonant ring is 0.5 $kW/\mu m^2$, which is below the resonator switching threshold (1.5 kW μm^2) so that the bias wave propagating in the B3 waveguide will fall into the output waveguide due to the resonance effect of the resonant ring and move into the output port and will activate the NAND gate. In this case, the gate will be in the ON state (OUT = 1) (Fig. 3 (a)).

In the case where "A" equals 1 (is activated) and "B" equals 0 (is deactivated) (A = 1, B = 0), the light coming from "A" moves towards the resonant ring, the power density is lower than the switching threshold, it at 1 $kW/\mu m^2$ which facilitates light propagation in the output port and it will be ON (OUT = 1) (Fig. 3 (b)).

If port "A" is OFF and port "B" is ON (A = 0, B = 1), the optical waves coming from port B will go to the resonant ring, the power density always remains below the threshold of switching (about 1 kW/μm^2), the resonant ring will drop the optical waves into the output port and the gate will be in the ON state (OUT = 1) (Fig. 3(c)).

In the last case where both input ports are ON (A = B = 1), the light will flow towards the resonant ring with an overall optical power intensity reaching the switching threshold (1.5 kW/μm^2) and will shift the resonant wavelength so that optical waves in the bus waveguide cannot reach the output port, which rounds the output equal to 1 (active) (Fig. 3(d)).

Figure 3.**d**: Output state of the NAND optical logic gate when A = B = 1

Table 1 summarizes all the preceding cases whose "ON" state is represented by "1" and the "OFF" state is represented by "0", it is clear that the output will be deactivated (Out = 0) when the two input ports will be activated (A = B = 1) otherwise the output will be activated (Out = 1). All these states are valid when the BIAS port is enabled always equal to “1”. Comparison of the results in Table 1 with the truth table of the NAND gate proves that the proposed structure works as a logical NAND gate optical.

Table 1
the output obtained from the NAND optical logic gate for different states of the input ports

BIAS	A	B	Logic Out	Out
1	0	0	**1**	**1**
1	0	1	**1**	**1**
1	1	0	**1**	**1**
1	1	1	**0**	**0**

5. Conclusions

In this study, we proposed an optical non-AND gate based on photonic crystals composed of guides in coupled with a ring resonator. When both logic ports are on, the bias light does not propagate to the output waveguide and will not go to the output port and the gate will be turned off (equal to 0), but when one or both logic ports turn off, the bias light propagates to the output waveguide, and the gate will become active (equal to 1).

Bold to its compact size the proposed NAND gate is easy to integration with other integrated circuits applied in all-optical communication systems.

Abbreviations

CP: crystal photonic;

FDTD: Finite Difference Time Domain;

WAN: wide area network;

2D: Two dimensional;

NAND: Not-And;

TE: transverse electric;

TM: transverse magnetic;

Declarations

Ethical approval and consent to participate:

Not applicable.

Consent for publication:

Not applicable.

Availability of data and materials

All data needed to evaluate the conclusions in the manuscript are presented herein and/or the Supplementary Materials. Additional data related to this study may be requested from the authors.

Competing interests

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R.D. proposed the idea and designed and performed the numerical simulations and wrote the manuscript, **MR.L.** performed the measurements, **S.M**. Supervised the overall projects. All the authors analyzed the data and discussed the results. All authors read and approved the final manuscript.

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Figures

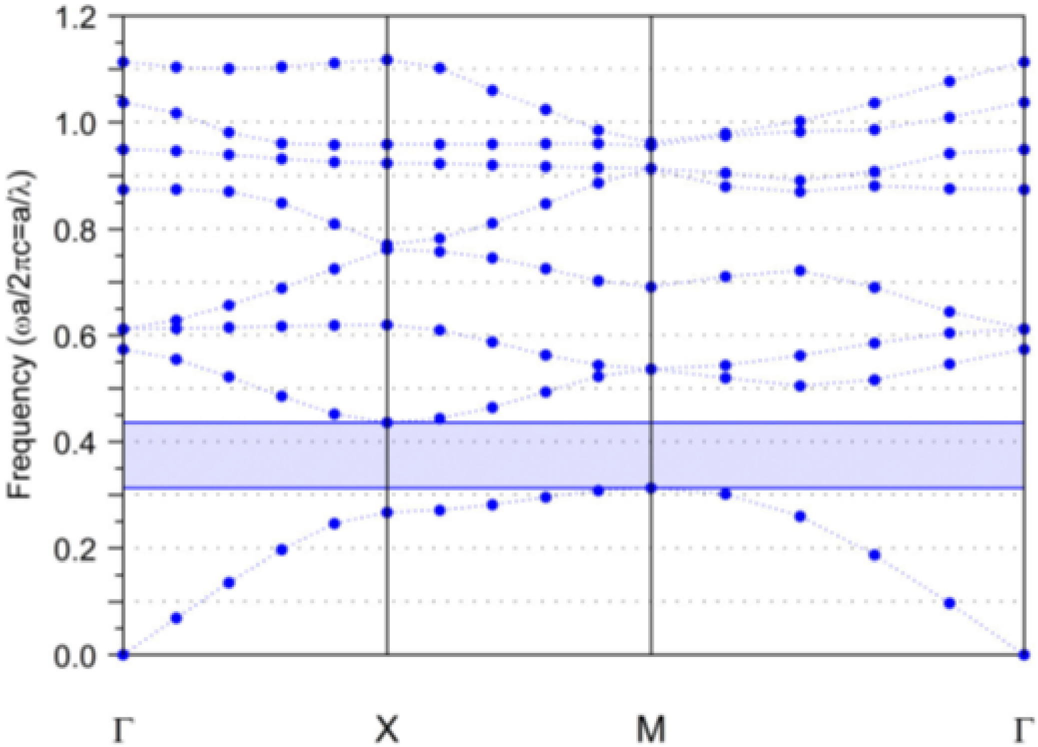


Figure 1

the bandgap of the proposed structure

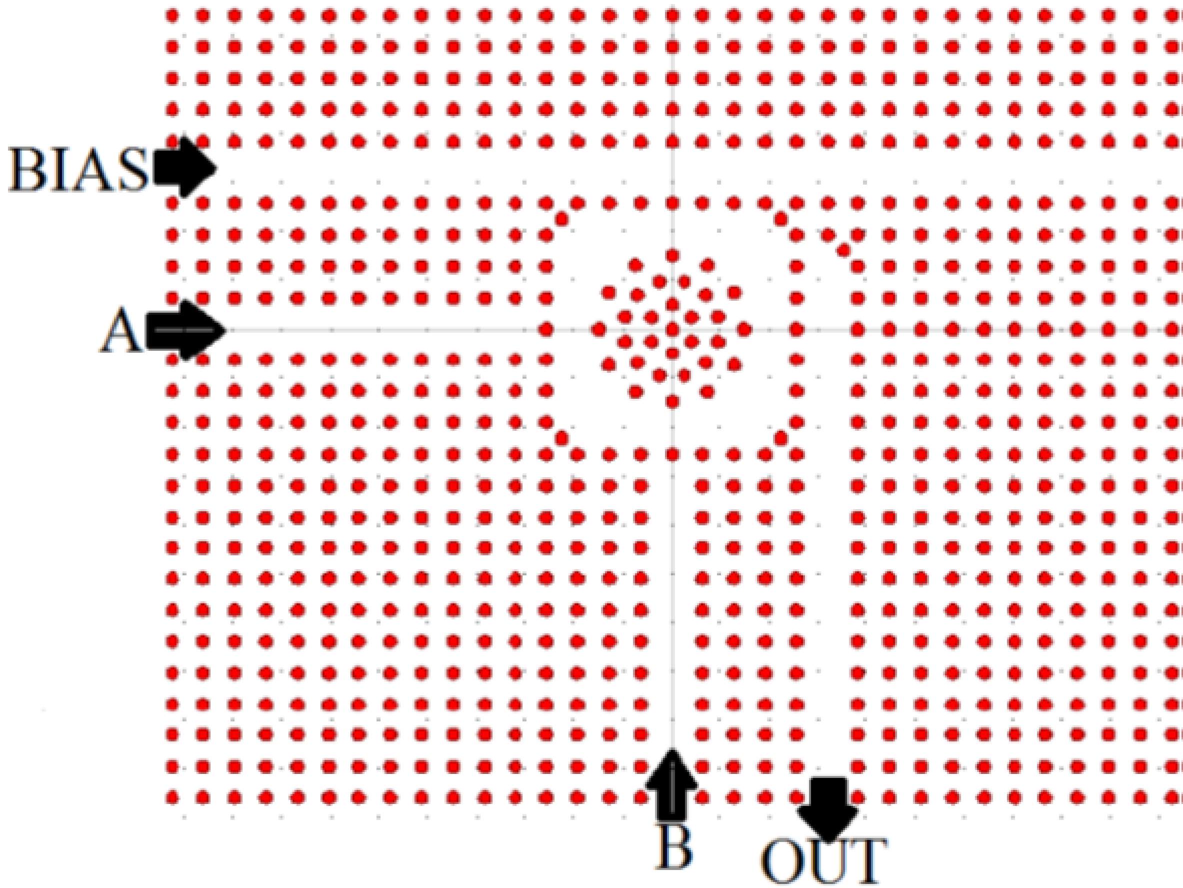
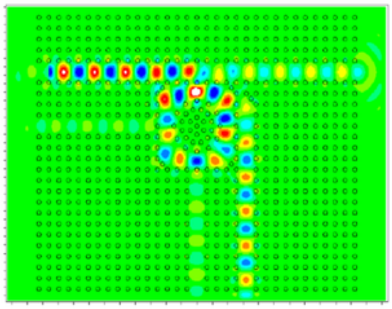


Figure 2

the proposed structure of NAND logic gate



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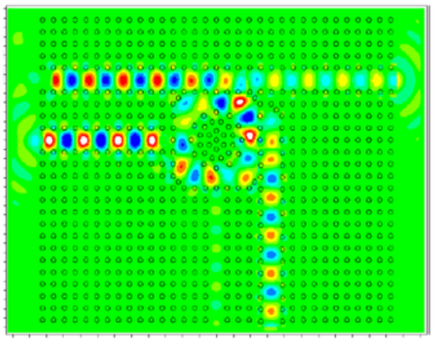

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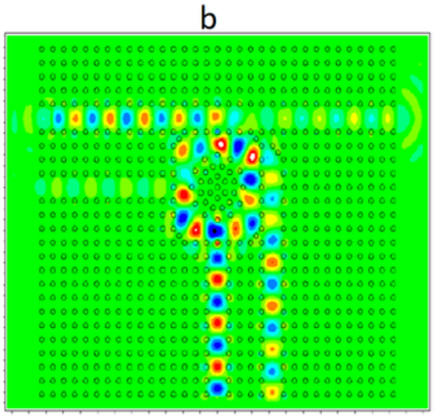
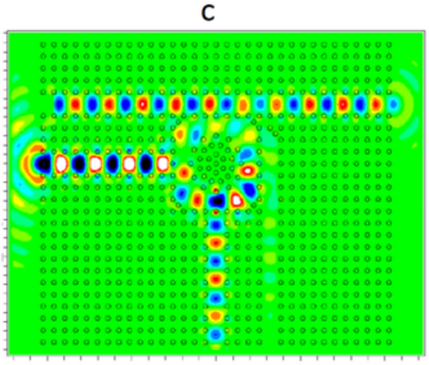


c



d

Figure 3

a: Output state of the NAND optical logic gate when A=B=0

b: Output state of the NAND optical logic gate when A=1.B=0

c: Output state of the NAND optical logic gate when A=0.B=1 d: Output state of the NAND optical logic gate when A=B=1