Wafer-Scale Functional Circuits Based on Two Dimensional Semiconductors with Fabrication Optimized by Machine Learning

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Table of Contents

1. Materials and Methods

a. Synthesis of wafer-scale MoS_2

A crucible with MoO_3 power (Alfa Aesar 99.95%) is placed in Zone 2, and an appropriate amount of sulfur powder (Alfa Aesar 99.999%) is placed in Zone 1, which is upstream of the flow in the tube. The distance between the two zones is 30 cm. A carefully rinsed sapphire substrate is placed face-down on the MoO_3 power. During the synthesis process, 300 sccm argon gas serves as a carrier gas. The synthesis temperature for Zone 1 and Zone 2 is controlled at 180 and 650 ^oC, respectively. Continuous monolayer MoS_2 film is synthesized at atmospheric pressure with a 10 min sulfuration time.

b. Fabrication process of MoS_2 FETs and circuits

The MoS_2 FETs and circuits are fabricated on the wafer-scale MoS_2 film on the sapphire substrate. The contact electrodes, source and drain contacts, are patterned by laser direct writing technology (Micro-Writer ML3) and subsequently deposited using Electronic Beam (E-beam) evaporation. CF_4 plasma etching is performed to define the MoS_2 channel region. A SiO_2 seeding layer is deposited by E-beam evaporation and subsequently annealed in an oxygen atmosphere at 100 ℃. Then HfO_2 is then grown by Atom Layer Deposition (ALD) as the FET dielectric layer. Another lithography/lift-off/deposition process is repeated to form the top metal layer. For electrical probing or further fabrication of more complex circuits, SF_6 plasma etching is used to remove the HfO_2 layer on top of the source/drain electrodes to form via holes defined by the lithography.

c. Electrical measurement

The electrical properties of MoS_2 FETs and circuits are carried out in a probe station connecting to an Agilent B1500A semiconductor analyzer with eight source measure units (SMUs). To investigate the circuit's dynamic response, an *Agilent 33622A* arbitrary waveform generator is used to input signals while a *RIGOL DS1054Z* digital oscilloscope captures the output voltage.

2. Raman spectra and mapping of wafer-scale MoS_2 films

Raman spectra from 1800 locations were measured in 3 regions (a, b, and c in Fig. S1d) of the as-synthesized films (insets in Fig. S1a-c). The Raman spectra have nearly identical shapes and intensities, revealing large-area uniformity in the synthesized monolayer MoS_2 film. Raman mapping at the E^1_{2g} peak (384.4 cm^{-1}) was also performed to build a 2D color plot in a square region (120×120 μm^2) at various positions (a, b, and c in Fig. S1d) on the wafer. These results show that the synthesis method used in this paper can effectively grow wafer-level, crystal-like, uniform MoS_2 monolayers with a variety of potential applications.

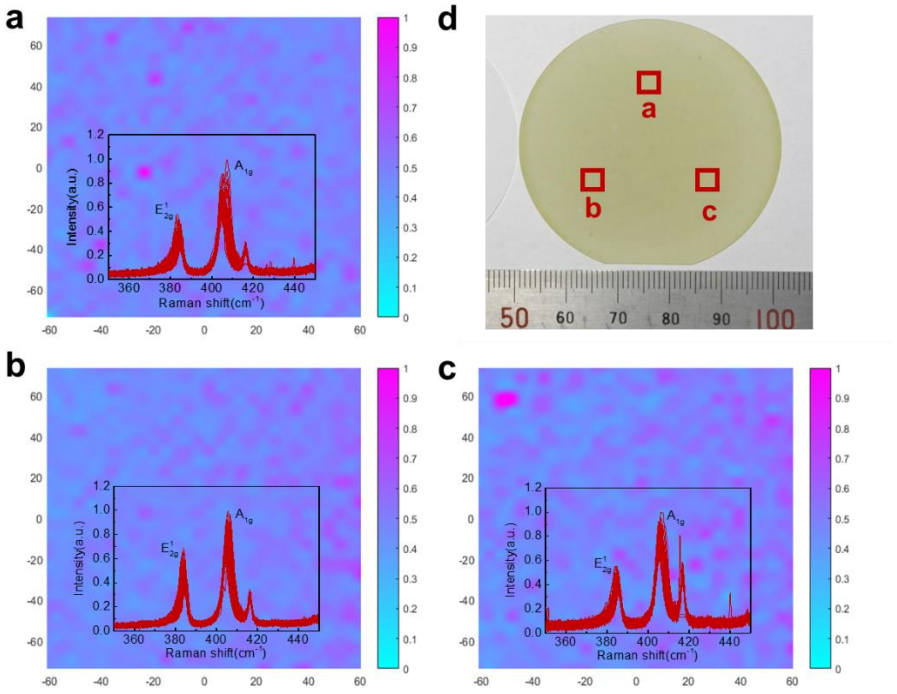

Fig. S1. Raman intensity maps normalized by the highest intensity at the E^1_{2g} peak (384.4 cm^{-1}) in wafer-scale monolayer MoS_2 grown on a sapphire substrate, where the scanning area is 120×120 μm^2. The wavelength of the Raman laser is 514 nm. The insets in Fig. S1 **a-c** show normalized Raman spectra from 1800 different locations in the scan area. **d,** Optical images of wafer-scale monolayer MoS_2, in which the three red squares (a, b, and c) indicate the scanning areas in Fig. S1 **a-c**, respectively.

3. The supervised ML method used in this work

a. Description of ensemble learning:

Because the semiconductor manufacturing process cannot guarantee similar data types in each step, we choose the Random-Under-Sampling (RUSBoost) algorithm and the decision tree as the weak classifier because they can efficiently handle discrete data, and RUSBoost is especially effective at classifying imbalanced data.

The RUS algorithm takes N, the number of members in the class with the fewest members in the training data, as the basic unit for sampling. Classes with more members are sampled by taking only N observations of every class. After training the RUSBoost classifier, we can find the best semiconductor manufacturing recipe combination through a grid search method. Grid search is extensively used in the field of discrete parameters.

B .Description of Radom forest algorithm

Random forest is an integrated learning algorithm based on decision tree learners, which is widely used and easy to implement [1,2]. The random forest algorithm can be summarized as follows:

1) The bootstrap method is used to select *n* samples from the sample set as a training set.

2) A decision tree is generated from the sample set. Multiple features X_j are randomly selected at each generated node *m* without repetition. Then they are used to divide the sample set until finding the best division feature.

3) Step 1 and step 2 are repeated *k* times, where *k* is the number of decision trees in the random forest.

4) The trained random forest is used to predict the test sample, while the voting method is used to determine the prediction result.

c. Feature importance assessment

Importance evaluation is used to see how much each feature contributes to each tree in the random forest. The Gini index was used for evaluation, which is defined as follows:

$$Gini(p) = \sum_{k=1}^{k} p_k(1 - p_k) = 1 - \sum_{k=1}^{k} p_k^2$$

where *k* is the number of categories and p_k is the weight of category *k*.

For feature X_j at node *m* in the Gini index, the difference before and after the branch generation of node *m* is defined as:

$$VIM_{jm}^{(Gini)} = GI_m - GI_l - GI_r$$

where GI_l and GI_r represent the Gini indices of two new nodes after the branch, respectively.

For feature X_j that appears in decision tree *i*, if the node is in set *M*, then the importance of X_j in decision tree *i* is:

$$VIM_{ij}^{(Gini)} = \sum_{m \in M} VIM_{jm}^{(Gini)}$$

If there are *n* trees in the random forest, then

$$VIM_{j}^{(Gini)} = \sum_{i=1}^{n} VIM_{ij}^{(Gini)}$$

Finally, all the obtained importance scores are normalized:

$$VIM_j = \frac{VIM_j}{\sum_{i=1}^{c} VIM_i}$$

where the denominator is the sum of all features' importance scores, and the numerator is the Gini index of feature *j*.

In this work, the evaluation index of each sample in the data set is calculated by the scores of mobility, threshold voltage (V_T), subthreshold swing (*SS*) and hysteresis with weights of 30%, 30%, 20% and 20% respectively (the percentage values can be adjusted according to devices with different functionalities, e.g. mobility is more important for faster speed and *SS* for low power consumption). Then the random forest algorithm is used to predict the scores of all possible processing combinations.

4. Detailed processing steps for fabricating MoS_2 FETs

Table S1 shows detailed MoS_2 FET processing steps used for machine learning in Fig. 2c in the main text. Steps filled with color are marked in Fig. 2c in the maintext, where device performance (threshold voltage or mobility) is more sensitive to changes in these parameters. In the following session 4–9, we discuss the optimization of these steps.

Table S1.
Detailed processing steps for machine learning.

Step Number	Detailed Process	Step Number	Detailed Process
1	Quality of MoS_2 film	26	Deposition rate 2 of contact
2	1st Photoresist coating	27	3rd Peeling temperature
3	1st Baking temperature	28	3rd Peeling time
4	1st Baking time	29	Annealing machine of contact
5	1st Spinning speed	30	Annealing gas of contact
6	2nd Photoresist coating	31	Annealing temperature of contact
7	2nd Baking temperature	32	Annealing time of contact
8	2nd Baking time	33	Annealing machine of seeding layer
9	2nd Spinning speed	34	Annealing time of seeding layer
10	2nd Exposure dose	35	Annealing temperature of seeding layer
11	2nd Developing time	36	Annealing gas of seeding layer
12	Etching gas	37	Seeding layer
13	Etching time	38	Temperature of the main dielectric growth
14	Etching power	39	Thickness of the main dielectric
15	Vacuum level of etching	40	Materials of top gate
16	2nd Peeling temperature	41	Deposition method of top gate
17	2nd Peeling time	42	Vacuum level of top gate deposition
18	3rd Photoresist coating	43	Deposition rate 1 of top gate
19	3rd Baking temperature	44	Deposition rate 2 of top gate
20	3rd Baking time	45	4th Photoresist coating
21	3rd Spinning speed	46	4th Baking temperature
22	Deposition method of contact	47	4th Baking time
23	Vacuum level of contact deposition	48	4th Spinning speed
24	Contact materials	49	4th Peeling temperature
25	Deposition rate 1 of contact	50	4th Peeling time

5. Impact of contact electrode on the transfer characteristics for top-gated MoS_2 FETs

Regarding the contact between MoS_2 and the metal electrode, there are two aspects that affect the contact resistance: *1*) the tunneling barrier between the metal and MoS_2 below the metal contact because of the van der Waals (vdW) gap and, *2*) the Schottky barrier between the MoS_2 channel and the metal electrodes. In order to compare the influence of different metal contacts on device electrical performance, four types of electrodes (Ti/Au, Au, In/Au and Ag/Au) were deposited as source and drain electrodes (Fig. S2). The results show that in this comparison group, *the devices with Au or Ti/Au electrodes exhibit larger on-state current, which is indictive of a better contact*. The fabrication recipes are shown in Table S2.

Table S2. Comparison group in which the S/D contact material is a variable and other parameter are kept the same.

Process	S/D	Seeding layer	Anneal of SL	Material of TG
a	Ti/Au	2 nm SiO_2	w/o	Au
b	Au	2 nm SiO_2	w/o	Au
c	In/Au	2 nm SiO_2	w/o	Au
d	Ag/Au	2 nm SiO_2	w/o	Au

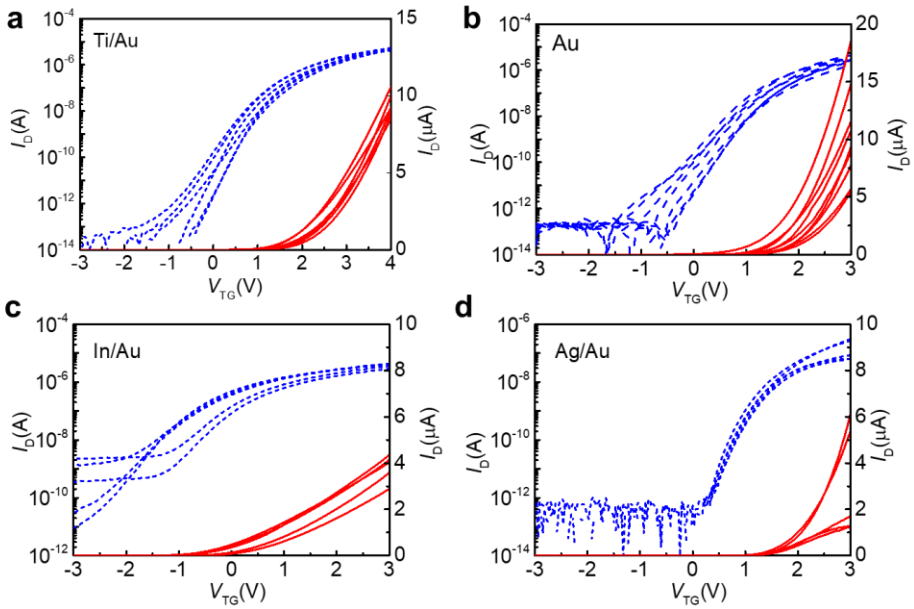

Fig. S2. I_D-V_{TG} curves of top-gated CVD MoS_2 FETs on wafer-scale substrate with **a,** Ti/Au, **b,** Au, **c,** In/Au, and **d,** Ag/Au contacts at V_{DS} = 0.1 V. Blue and red curves correspond to the logarithmic scale on the left and linear scale on the right y-axis, respectively.

In this group of comparison experiments, we further compare the performance of top-gated MoS_2 FETs with different contact electrodes. The contact resistant *R*c extracted using the Y-function method is plotted with error bars for different contact electrodes shown in Fig. S3. Based on these statistical results, we can again conclude that *Au and Ti/Au contact electrodes provide lower contact resistant than that from other electrodes*.

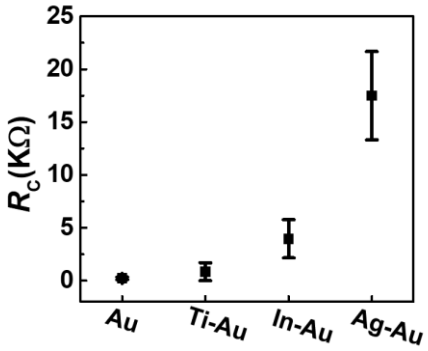

Fig. S3. Extracted contact resistance between MoS_2 and different metals using Y-function fitting to transfer curves.

6. Impact of seeding layer on the transfer characteristics for top-gated MoS_2 FETs

In this group of comparison experiments, we tested different various seeding layers (SLs), and found that both *2-nm-thick SiO_2 and Al_2O_3 are favorable SL materials for FETs to achieve positive V_T and the large on-state current*. The fabrication recipes and transfer characteristics for top-gated MoS_2 FETs are shown in Table S3 and Fig. S4.

Table S3. Comparison group in which the SL material is a variable and other parameter are kept the same.

Process	S/D	Seeding layer	Anneal of SL	Material of TG
a	Au	N/A	w/o	Au
b	Au	2 nm Y_2O_3	w/o	Au
c	Au	2 nm Al_2O_3	w/o	Au
d	Au	2 nm SiO_2	w/o	Au

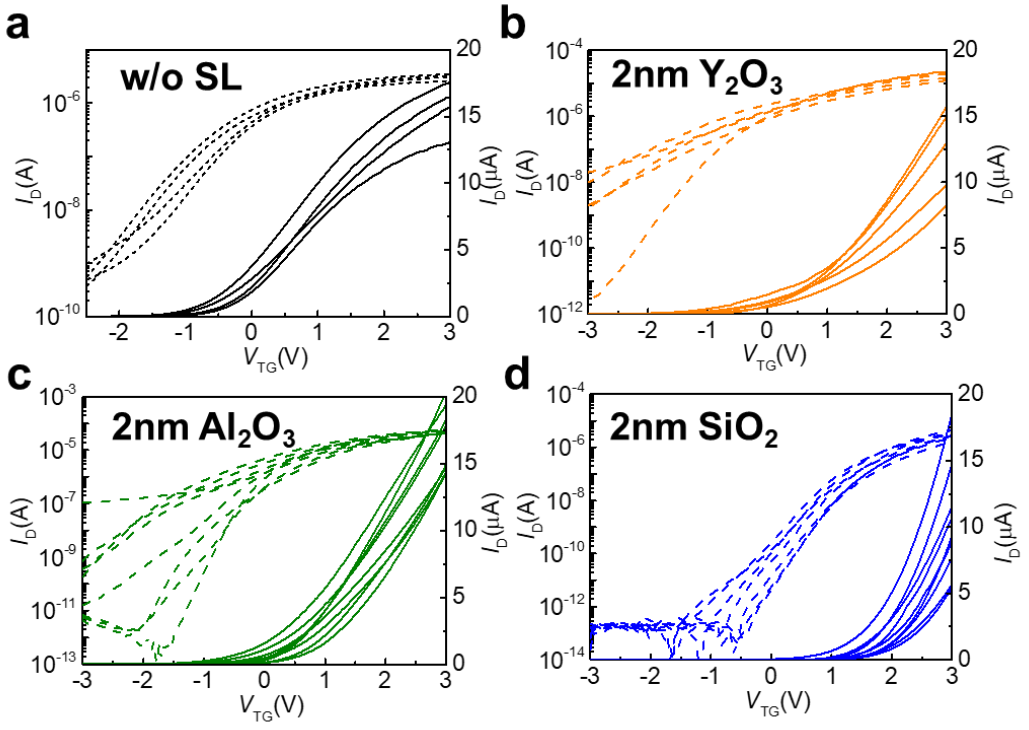

Fig. S4. a-d, I_D-V_{TG} curves of top-gated CVD MoS_2 FETs on wafer-scale substrate with different processes (a-d in Table S3) at V_{DS} = 0.1 V.

7. Transfer characteristics for top-gated MoS_2 FETs with and without annealing after seeding layer deposition

In order to improve the electrical characteristics of MoS_2 FETs, we annealed the devices at 100 °C in nitrogen for 30 min after deposition of a seed layer. Compared with unannealed devices, *V_T is more positive and steeper subthreshold (SS) is obtained after annealing*, most likely due to the improvement of interface between MoS_2 and seed layer, as well as reduction of defects and dipoles in the channel and contact region. The fabrication recipes and transfer characteristics for top-gated MoS_2 FETs are shown in Table S4 and Fig. S5.

Table S4. Comparison group in which the SL annealing is a variable and other parameter are kept the same.

Recipe	S/D	Seeding layer	Anneal of SL	Material of TG
a	Au	2 nm SiO_2	w/o	Au
b	Au	2 nm SiO_2	w/	Au

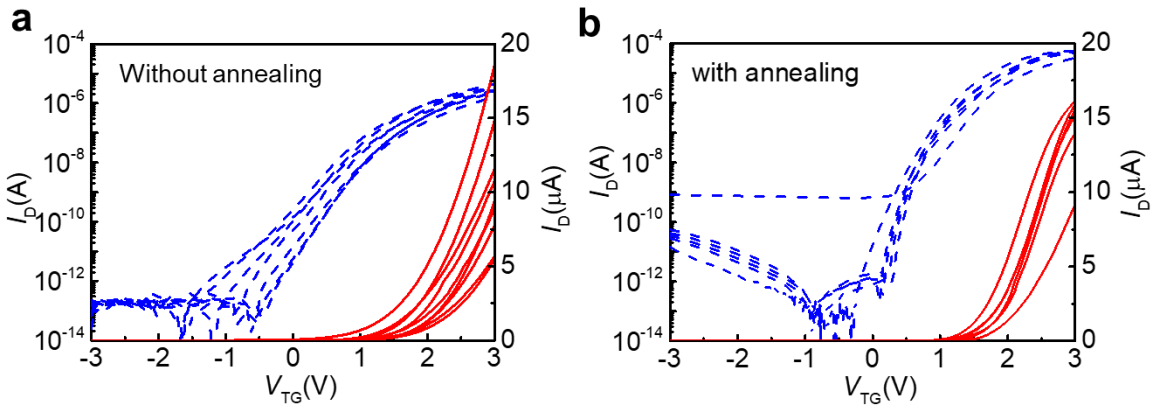

Fig. S5. I_D-V_{TG} curves of the top-gated CVD MoS_2 FETs on a wafer-scale substrate with an **a,** unannealed and **b,** annealed seed layer at V_{DS} = 0.1 V.

8. Impact of TG electrodes on the transfer characteristics for top-gated MoS_2 FETs

Au and Al were deposited to fabricate the top gate of the MoS_2 FETs. The work function of these metals is used to tune the threshold voltage V_T of the devices. The experimental results indicate that an *Au TG is more desirable for fabricating enhanced-mode FETs* due to its larger work function. The fabrication recipes and transfer characteristics for top-gated MoS_2 FETs are shown in Table S5 and Fig. S6.

Table S5. Comparison group in which he material of TG is a variable here and other parameters are kept the same.

Recipe	S/D	Seeding layer	Anneal of SL	Material of TG
a	Au	2 nm SiO_2	w/	Au
b	Au	2 nm SiO_2	w/	Al

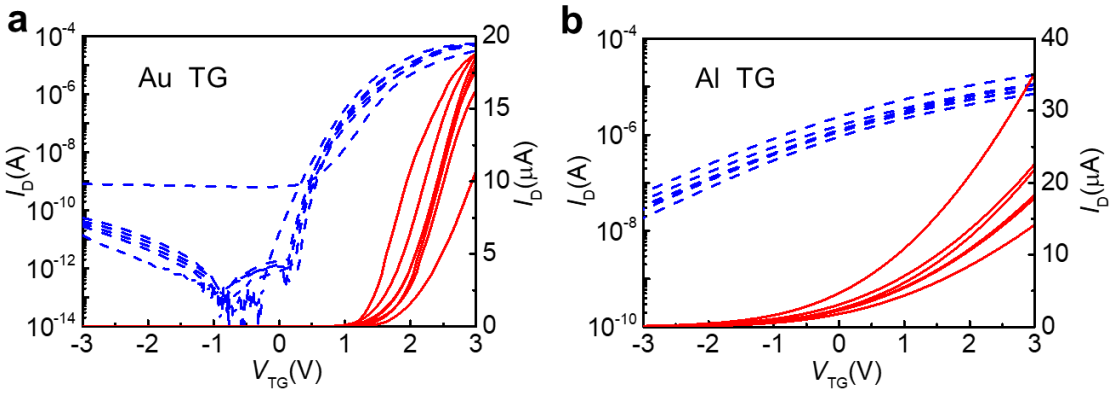

Fig. S6. I_D-V_{TG} curves of top-gated MoS_2 FETs with **a,** Au TG and **b,** Al TG at V_{DS} = 0.1 V.

9. Comparison of device uniformity for top-gated MoS_2

To ensure a wafer-scale homogeneity of device performance, several top-gated MoS_2 FETs arrays were fabricated with different fabrication procedure combinations. Fig. S7a-c shows more than 100 transfer curves from device arrays prepared through three different process combinations (*a*, *b*, and *c* in Table S6). Fig. S7c is the same as Fig. 2g in the main text and presented here for a straightforward comparison. Other than the four processing steps shown in Table S6, all other steps are kept the same for comparison.

The results show that top gated MoS_2 FETs fabricated by combination *c* exhibit positive V_T, large ON-state current and high uniformity, which is the best result for further circuit fabrication. *It is noteworthy that combination c is not simply a combination of all best choices in each processing step from Sections 4–8.*

This confirms that our ML method for fabrication optimization indeed works since *the evaluation score (Fig. 2e) of recipe a and b are lower than that of c, by considering more comparison test results not listed in this SI.*

Table S6. Comparison group with 3 different recipe combinations.

Process combination	S/D	Seed layer	Anneal of SL	Material of TG
a	Au	2 nm Al_2O_3	W/	Au
b	Au	2 nm SiO_2	W/	Au
c	Ti/Au	2 nm SiO_2	W/	Au

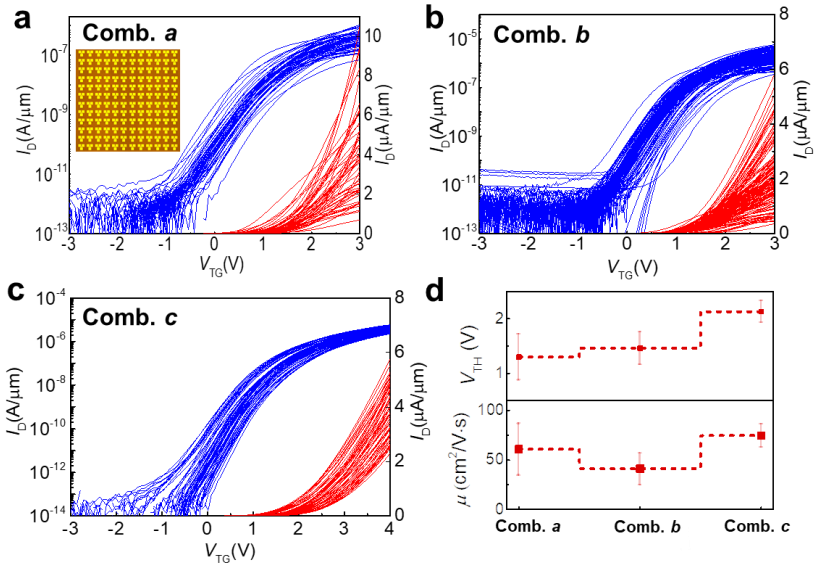

Fig. S7. a-c, I_D-V_{TG} curves of top-gated CVD MoS_2 FETs array on wafer-scale substrates in different batches (a-c in Table S6) at V_{DS} = 0.5 V. **d,** The extracted threshold voltage and mobility with error bar of device arrays prepared through various recipes a-c.

10. Low frequency 1/f noise in top-gated MoS_2 FETs

Low frequency noise measurements were gathered with a semiconductor parameter analyzer (Agilent 4156C), current amplifier (Stanford SR570), and spectrum analyzer (Agilent 35670A) in a manual probe station (Cascade). A schematic diagram of the measurement setup is shown in Fig. S8.

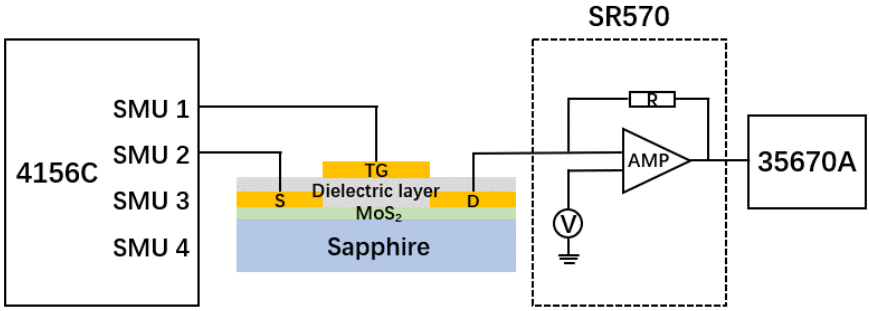

Fig. S8. Schematic diagram of reliability testing equipment of top-gated MoS_2 FET.

In a working FET, the current fluctuates within a small range due to electrical noise. It is generally represented by power spectral density, i.e., noise power per unit frequency.

Border traps can exchange charge with the channel through carrier capture or emission by tunneling when the gate voltage is swept. The border trap density can be further extracted from the low-frequency noise in the transistor, as shown in Fig. S9. Here, the noise power spectra normalized against the drain current I_D are extracted, as shown in Fig. S9a.

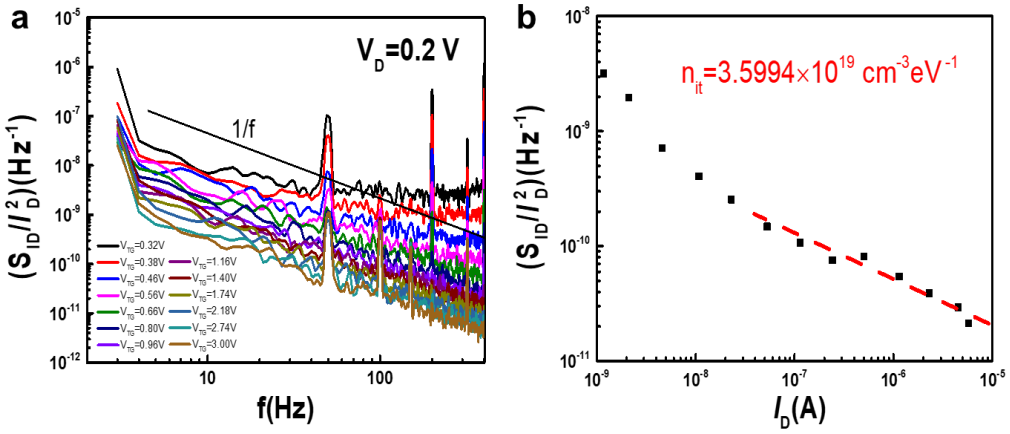

Fig. S9. Low frequency 1/f noise characteristics. **a,** Normalized noise power spectra (S_{ID}/I_D^2) as a function of *f*. **b,** S_{ID}/I_D^2 as a function of I_D at 100 Hz. The dashed line shows a corresponding linear fit.

In order to analyze the border trap intensity, the values of S_{ID}/I_D^2 at 100 Hz are plotted as a function of I_D in Fig. S9b. The trap density N_{bt} can be extracted from the following equation:

$$\frac{S_{I_d}}{I_d^2} = \frac{kT}{\gamma f W L}\left(\frac{1}{N} + \alpha\mu\right)^2 N_{bt} \qquad (1)$$

where W is the channel width, L is the channel length, μ is the mobility, T is

temperature, k is Boltzmann's constant, f = 100 Hz, the tunneling coefficient γ is typically taken to be 10^8 cm^{-1}, the areal density of the carriers is $qN = C_{OX}(V_{GS} - V_{th}) = \frac{I_D}{(W/L)\mu V_{DS}}$, and α is the scattering coefficient.

By fitting discrete points in Fig. S9b, the N_{bt} values in the accumulation regime were extracted using MATLAB and found to be 3.5994×10^{19} cm^{-3} eV^{-1}, which is lower than the value stated in previous reports [3-5].

11. Analysis of inverters with different pull-up transistors

For circuit-level application, we need to increase the noise margin of the inverter. Based on the level-62 RPI model a simulation result is shown in Fig. S10a, where different V_T values are set for load transistor M1 to increases the driving current when V_G = 0 V. Guided by the simulation results, metals with different work functions were used to prepare TG for pull-up transistor (M1) in the inverter circuit, Experimental results are shown in Fig. S10b, when Al is used as the top gate metal, the switching point of V_{TC} is 1.5 V and a largest noise margin can be obtained.

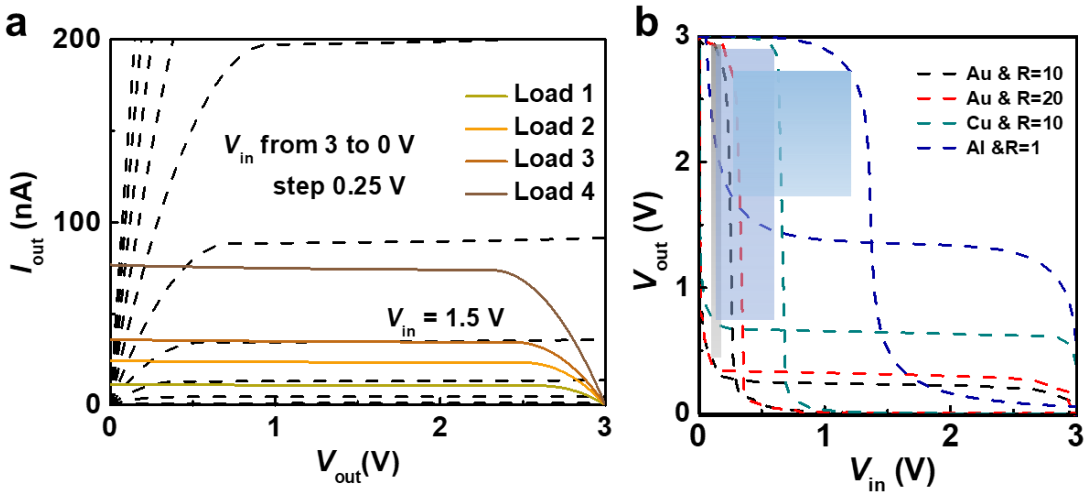

Fig. S10. a, Simulation results of output characteristics (I_{OUT} vs. V_{OUT}) for pull-down transistor (M2) when V_{IN} is scanned from 0 V to 3 V in 0.25 V increments. The solid lines are the output characteristics of pull-up transistors with different V_T. **b,** Experimental voltage transfer characteristics with pull-up transistor designed by different TG metals and transistor geometry R=(W/L)$_{M1}$/(W/L)$_{M2}$.

12. Analog amplifier composed of an inverter based on MoS_2 FET

Thanks to its high voltage gain (>20), the MoS_2 inverter is a promising analog amplifier for small AC signals. By applying an AC signal with a DC bias on the gate electrode of the driver FET, an amplified voltage can be obtained at the output port. To reach maximum output voltage swing, the DC bias value is carefully controlled to set the inverter in the middle of the steepest region of the voltage transfer curve. We achieved this by applying a 920 mV DC bias and mixing 20 mV AC signals on the gate bias. The frequency of the AC signal was set to be 0.1 Hz due to the limited sample rate of the measurement equipment. The input and output signals are displayed in Figure S11, where the output voltage (Vout-amp) has a phase difference of 180° with respect to the input voltage (Vin-amp). It is shown that the gain $V_{in\text{-}amp}/V_{out\text{-}amp}$ is larger than 100, indicating the amplifier circuit has desired functionality. The frequency range can be further extended by reducing the parasitic capacitance in the overlap area and increasing the transistor's transconductance.

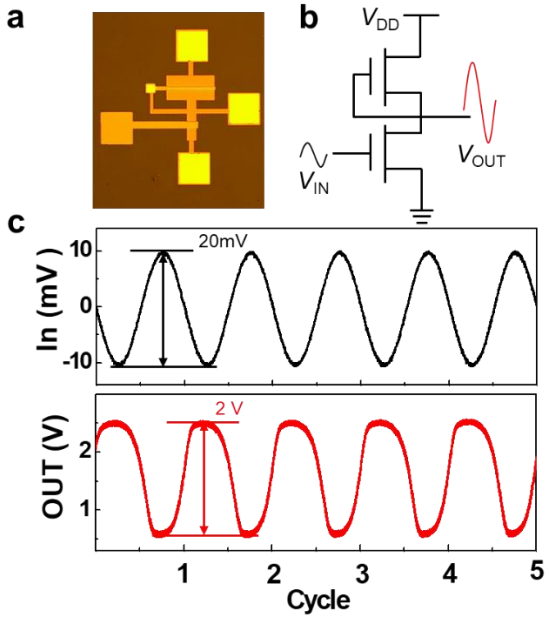

Fig. S11. a, Microscope image and **b,** schematic diagram of the inverter built from a pseudo n-type circuit. **c,** Measured waveforms from the inverter with 20 mV input and ~2 V output indicate high gain (>100).

13. Measurement results of various basic logic circuit units

In addition to the negative edge-triggered D flip-flop and 1-bit full-adder mentioned in the main text, we also prepared and tested a 1-stage inverter, 2-stage inverter, NAND, NOR, XNOR, XOR, LATCH, and 2-bit adder, as shown in Figs. S12 and S13.

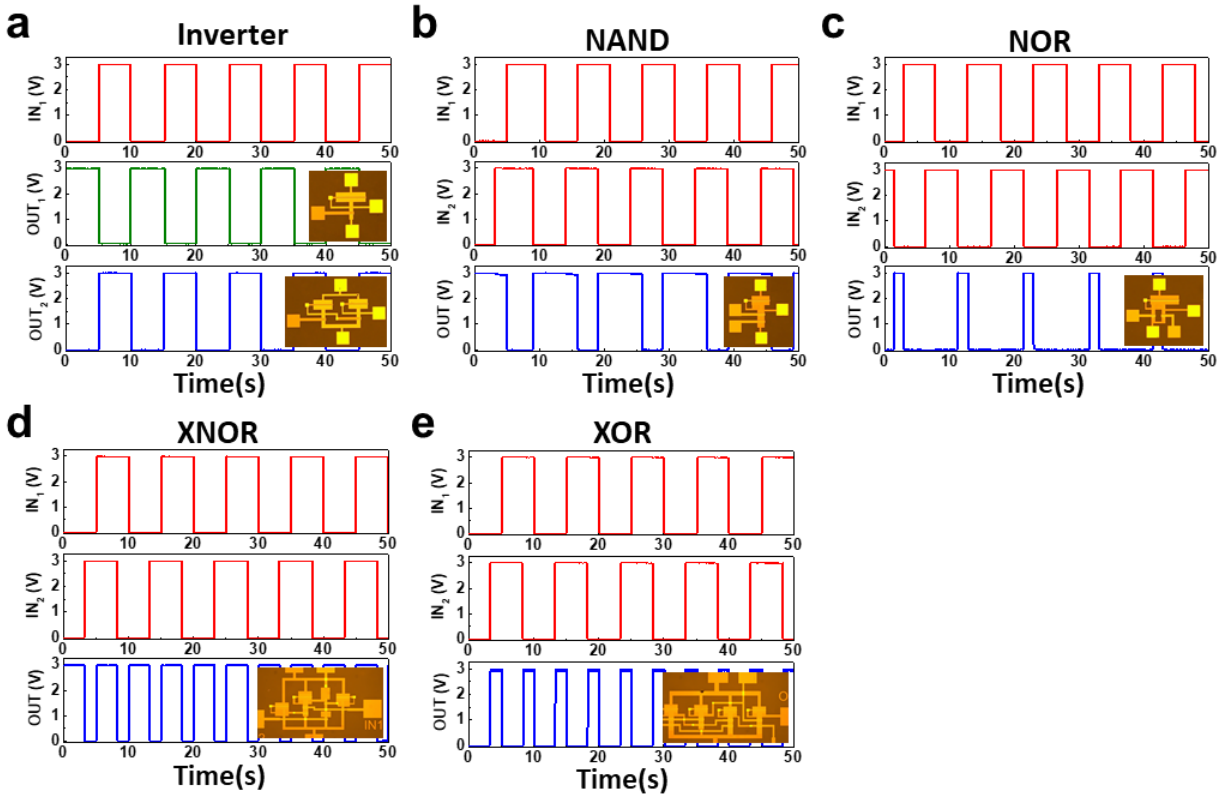

Fig. S12. Micrograph and measurements from the fabricated **a,** inverter, **b,** NAND, **c,** NOR, **d,** XNOR, and **e,** XOR.

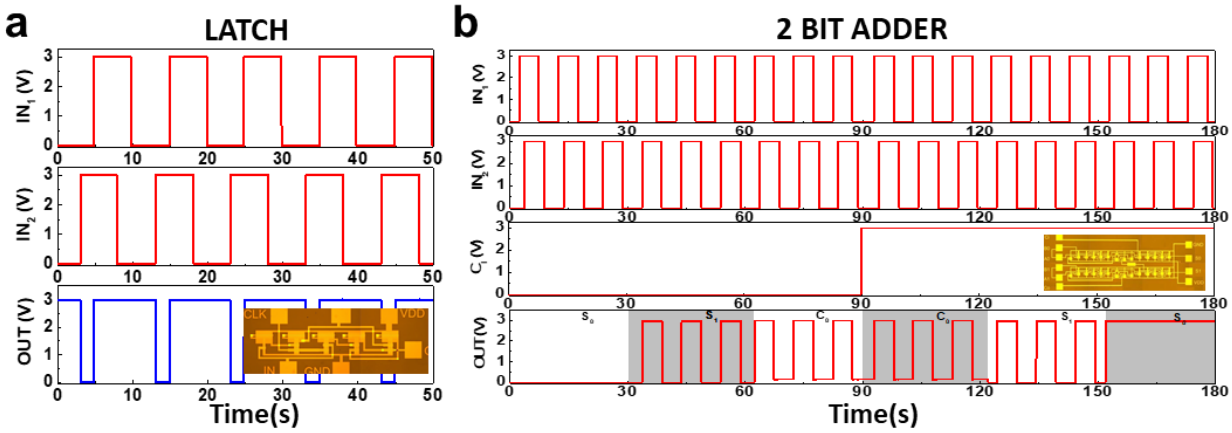

Fig. S13. Micrograph and measurement results from the fabricated **a,** LATCH and **b,** 2-bit adder.

14. Schematic diagram of DRAM testing setup

DRAM testing: A waveform generator was used to generate signals applied to the gate and drain bias of the DRAM transistor, as shown in Fig. S14a. The source was collected with an equivalent circuit, as shown in Fig. S14b.

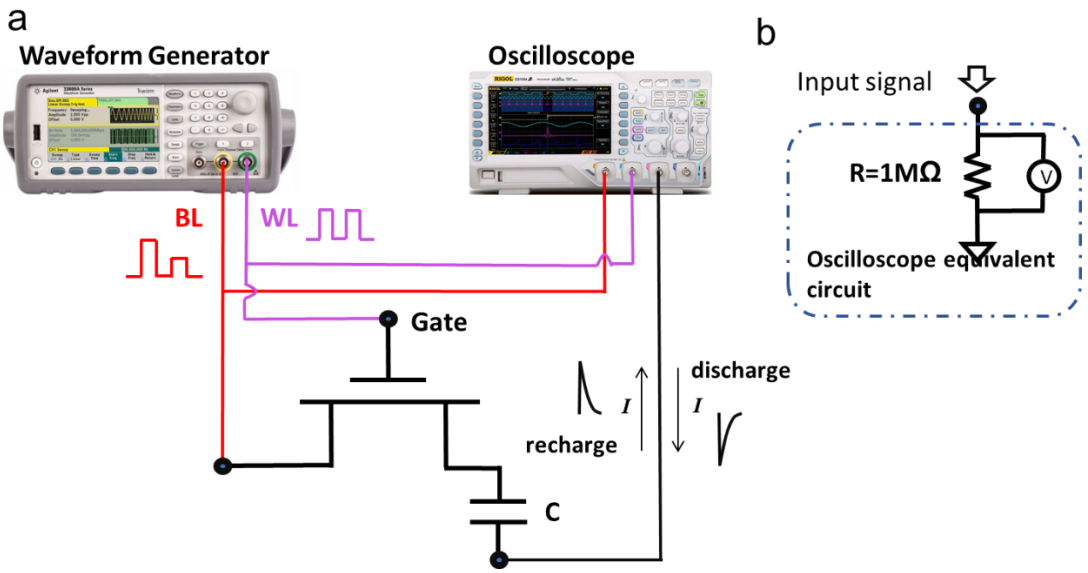

Fig. S14. a, Schematic diagram of DRAM testing equipment and **b,** equivalent oscilloscope circuit.

The characteristics of reading charge pulse after different hold time ranging from 10 to 8000 ms at the read operation are shown in Fig. S15. The reading charge pulse changes from negative to positive as the holding time increases, which means that the charge of DRAM is discharging with the hold time increasing.

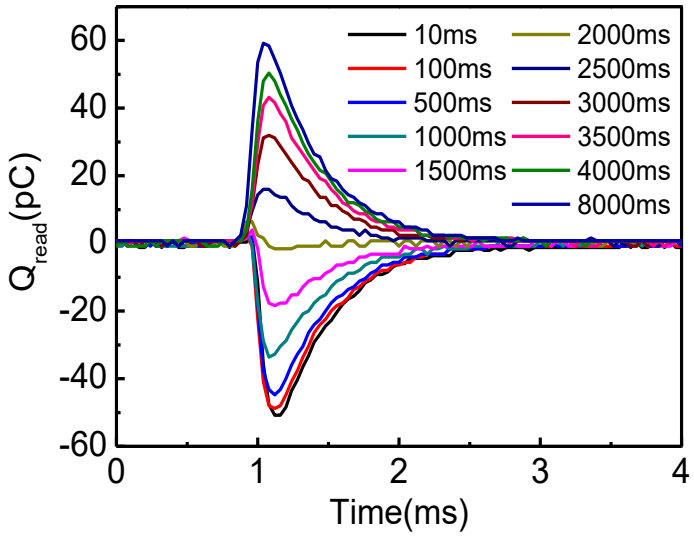

Fig. S15. The characteristics of reading charge pulse after different hold time at the read operation.

15. Photoelectric characteristics for top-gated MoS_2 FETs

In order to characterize the photoelectric characteristics of the top-gated MoS_2 FETs, we measured the transfer characteristics while the devices were illuminated with different wavelengths and power density values at V_{DS} = 1 V. Further, the photocurrent can be extracted, as shown in Fig. S16. The responsivity spectra at different power density values were also calculated.

The time-resolved photoresponse in the top-gated MoS_2 phototransistor is shown in Fig. S17, where the data were gathered at $V_{TG} = -1$ V and $V_{DS} = 1$ V while illuminated with 1.55 mW·cm^{-2} at 550 nm. A rise time of 1.2 s and fall time of 5.76 s were observed in the photocurrent measurements.

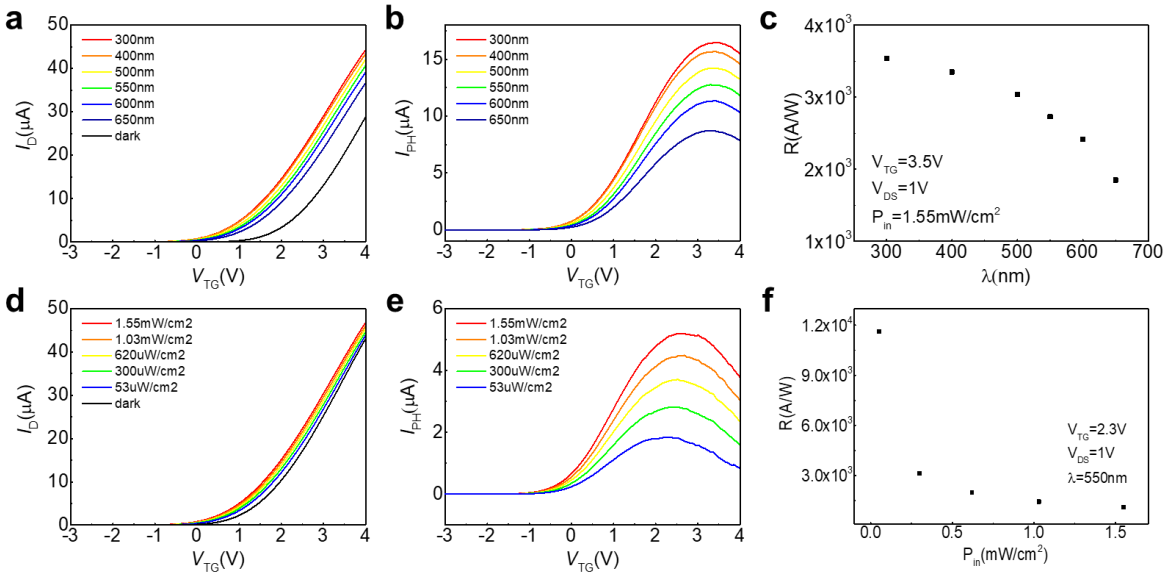

Fig. S16. I_D-V_{TG} curves for a TG MoS_2 FET in darkness and while illuminated with **a,** different wavelengths and **d,** different P_{in} values at V_{DS} = 1 V. I_{PH}-V_{TG} curves for a top-gated MoS_2 FET illuminated with **b,** different wavelengths and **e,** different P in values. **c,** Corresponding wavelength and **f,** P_{in} dependence of R.

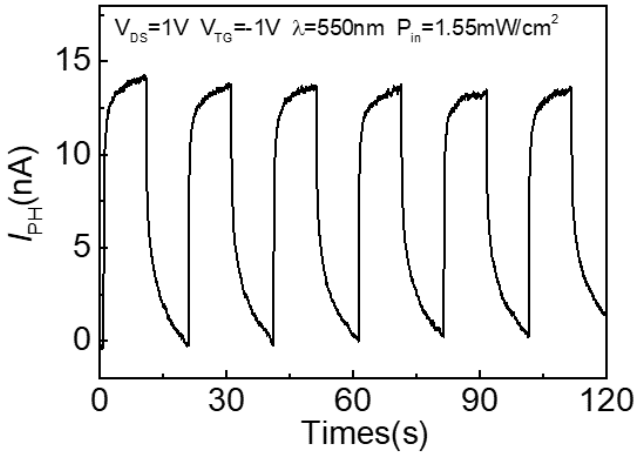

Fig. S17. Time-resolved photoresponse of the TG MoS_2 phototransistor with $V_{TG} = -1$ V and V_{DS} = 1 V under illumination with 1.55 mW·cm^{-2} at 550 nm.

Detailed photocurrent characteristics from 9×9 TG MoS_2 FET arrays mentioned in Fig. 3q are shown in Fig. S18 while illuminated with white light at V_{DS} = 0.5 V.

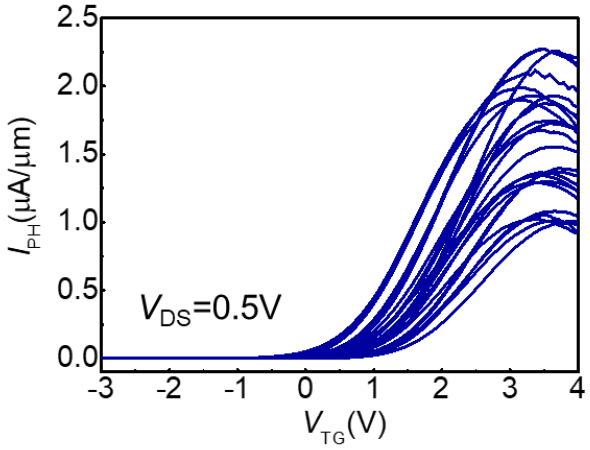

Fig. S18. Photocurrent characteristics of 9×9 top-gated MoS_2 FET arrays shown in Fig. 3q.

16. Comparison with recently published works

Table S7 summarizes the results of the previously reported results and the work of this paper. Among these results our TG MoS_2 FETs exhibit high performance for almost all the important parameters, and the functional circuits in our work have the largest transistor number.

Table S7. Comparison of MoS_2 FET performance with recently published results

Area	V_{DS} (V)	Ion (A)	Ioff (A)	Ion/ Ioff	Mobility μ ($cm^2 V^{-1} s^{-1}$)	V_T (V)	Max. FETs number/IC	W/L	Gate type	Ref
~50mm^2	5	9×10^{-5}	10^{-12}	10^8	~3	~0.65	115	45/2	BG	[6]
2mm×3mm	2	2×10^{-5}	10^{-11}	10^6	3	-	3	45/3	TG	[7]
4 inch	3	10^{-3}	10^{-13}	10^{10}	~55	-	12	30/6	BG	[8]
-	3	10^{-3}	10^{-13}	10^{10}	~50	0.54	9	30/4	BG	[9]
1cm×0.5cm	1	$\sim10^{-5}$	10^{-14}	10^8	> 40	-2	3	1/1	BG	[10]
-	1.5	10^{-5}	10^{-14}	10^9	80	2.41	10	30/4	BG	[11]
2 inch	0.5	5.65×10^{-5}	10^{-14}	10^9	~88	2.47	156	30/20	TG	**This work**

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