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A 28.0%-efficiency THBC cell enabled by submicron scale bevel engineering

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Abstract

Hybrid back contact architectures uniquely integrate a genuine hole-selective emitter and a broad fabrication process window within a single device stack. Building on this platform, we introduce a submicrometre-scale bevel passivation strategy that further suppresses parasitic recombination at the tunnelling junction edge. Together with nanotexturing of the n-type polycrystalline silicon contact, we achieve a certified cell efficiency of 28.0% and a fill factor exceeding 88% on large-area rectangular wafers (105 mm by 182 mm). These advances are enabled by substantial progress toward Auger recombination dominance, alongside extreme optimization of contact resistivity. As a result, the product of the open-circuit voltage and fill factor for our device reaches 98.5% of the Shockley–Queisser limit. Leveraging these cell-level improvements, we demonstrate a large-area module with a third-party certified efficiency of 26.74%, a marked advance over the existing record for single-junction silicon photovoltaic modules, featuring a normalized V_{OC} above 748 mV and an *FF* approaching 85%. This device is reconstructed from the silicon heterojunction and TOPCon passivated contact precursors and the module is immune from damp-heat degradation with a silver paste metallization. Remarkably, the implementation of a patented CSTL gap-protection layer renders the architecture fully compatible with copper-paste metallization, positioning it as a viable pathway toward terawatt-scale clean energy deployment while remaining within a striking distance of the 29.4% crystalline silicon efficiency limit.

Introduction

Tunneling oxide passivated contact (TOPCon)[1] devices currently represent the dominant mainstream in industrial photovoltaic deployment, underpinned by the champion efficiency of 26.55%[2] and typical commercial module efficiencies above 24%. Silicon heterojunction (SHJ) technology offers an alternative high-efficiency pathway, with a confirmed laboratory cell efficiency of 26.9%[2] and an independently verified large-area module efficiency of 25.44%[3]. While front-and-back contact (FBC) architectures now dominate the commercial photovoltaic market, SunPower historically established early performance leadership in the specialized tunnel oxide passivated back-contact (TBC) category from both large-area cells (24.2%) and modules (21.4%)[4]. In recent years, several manufacturers including Sanyo/Panasonic[5], Kanaka[6,7] and LONGi[8] have reported pilot-line demonstrations of heterojunction back-contact (HBC) structures, yet large-area module efficiencies for this platform have remained largely stagnant near 25%. This performance bottleneck arises primarily from excessive surface passivation losses, which originate from the inherent chemical sensitivity of intrinsic and n-type amorphous silicon films[9] used in the stack.

LONGi has previously demonstrated a full-area TBC device with a certified efficiency of 27.0%[10], delivering an open circuit voltage (V_{OC}) of 744.7 mV and short circuit current (J_{SC}) of 42.32 mA/cm^2 on a 170 μm-thick wafer. Notably, the corresponding HBC architecture does not exhibit the Auger recombination dominance that is characteristic of conventional front-and-back SHJ devices. A critical breakthrough came in March of 2023, when Xie ZG and Lin CH announced a hybrid back-contact cell result during the annual conference of the National Engineering Research Center (NERC) for High-Efficiency Solar Cell Equipment and Technology. Inspired by Triex SHJ technology[11] from Silevo/SolarCity, TBC from SunPower and floating busbar technology from Trina, the initial prototype achieved an aperture-area efficiency of 27.08% and a signature V_{OC} of 751 mV and fill factor (FF) of 87.06%, with independent certification issued by the National PV Industry Measurement and Testing Center (Fujian). After an engineering transfer process, as well as a successful replacement of the front-side stack with TBC-like window layers, LONGi reproduced and updated this hybrid architecture to deliver a certified HTBC efficiency of 27.4%, as documented in the 2024 Solar Cell Efficiency Table[12]. Full details of the underlying process and device optimization[13] strategies were subsequently disclosed alongside a new independently confirmed champion efficiency of 27.81%, corresponding to an FF of 87.55%.

Results

Device structure and electrical simulation

We propose a TOPCon-compatible hybrid back-contact cell architecture, designated THBC, built on n-type Czochralski silicon wafers with a base resistivity in the range of 1–2.5 Ω·cm, and an absorber thickness ranging from 130 µm to 175 µm. The full layer sequence and device geometry are schematically illustrated in Fig. 1a. Both the n-type polycrystalline silicon (n-poly-Si) TOPCon contact and the amorphous silicon p-type emitter are processed using a laser selective emitter (SE) patterning step. The front-side stack begins with an 8 nm -thick aluminium oxide (AlO_x) passivation film and is overlaid by a cascaded antireflective coating (ARC) composed of silicon nitride and silicon oxynitride sub-layers. On the rear side, 60–65% of the total area is covered by p-type passivation, with the remaining fraction occupied by the n-type TOPCon passivating contact.

The field-effect passivation provided by both hydrogenated amorphous silicon (a-Si:H) and AlO_x layers can be described by a fixed interface charge density Q_{it}. The typical value for this negative charging density[14,15,16] lies in the range of 0.5–1 µC/cm^2. The corresponding mid-gap interface defect density D_{it} is maintained at the level of 1x10^{11} cm^{-2}eV^{-1} for state-of-the-art passivated interfaces including Si/SiO_x[17], Si/AlO_x[18], or Si/a-Si:H. To quantify the relationship between interface properties and recombination performance, we performed classic drift–diffusion device simulations, the results of which are summarized in Fig. 1b. By extrapolating the saturation current density J_0 from the plot of the surface recombination current J_{rec} versus quasi-Fermi level separation V_a, we established a qualitative correlation between Q_{it} and the resultant J_0. Guilded by this model and validated against our experimental data, the single-sided J_0 for both p-type field-effect passivations and n-type TOPCon passivating contact reaches around 0.5 fA/cm^2, while the p-type TOPCon passivating contact[19] remains limited to around 4 fA/cm^2 at the current stage of development.

We further conducted a systematic device sensitivity analysis to map the dependence of key electrical parameters on the n-Si absorber thickness, as presented in Fig. 1c. Under Scenario A, which assumes high-quality surface passivation (J_0 of 1 fA/cm^2) combined with a moderate bulk minority carrier lifetime of 10 ms, the FF shows a continuous improvement as wafer thickness decreases. This behaviour favours the adoption of a thin 130 µm n-type absorber, consistent with the practice that has enabled high efficiencies in state-of-the-art SHJ cells. For Scenario B, which represents a surface-recombination-limited regime with a high bulk lifetime of 30 ms, both V_{OC} and FF are found to be extremely sensitive to the surface saturation current density J_0. To illustrate this trend, we defined three distinct cases in Fig.1c: J_0 = 1 fA/cm^2 ($J_{0,\,front}$ of 0.5 fA/cm^2, $J_{0,\,back}$ of 0.5 fA/cm^2), J_0 = 2.2 fA/cm^2 ($J_{0,\,front}$ of 0.7 fA/cm^2, $J_{0,\,back}$ of 1.5 fA/cm^2), and J_0 = 5 fA/cm^2 where the surplus J_0 is attributed to parasitic losses at the device bevel edge. For architectures with nonideal surface passivation, as is typical for most

reported back-contact devices, the highest confirmed efficiencies are almost universally achieved using a thicker absorber thickness (about 160 µm).

Drawing on the full set of simulation and experimental insights, we fabricated champion THBC cells across three distinct wafer thickness groups: 135 µm, 165 µm and 175 µm, and submitted representative devices to ISFH CalTeC for independent third-party certification. The 135 µm-thick record cell delivers a certified V_{OC} of 749.3 mV and a power conversion efficiency (PCE) of 27.73%. Our highest performing device, based on the 165 µm-thick absorbers, achieved an independently confirmed *PCE* of 27.83%. However, due to the aperture-area measurement setup[20] (3 mm edge exclusion), there is typically a 1–2 mV reduction in V_{OC}, a 0.3–0.4% absolute increase in *FF*, and a roughly 0.2 mA/cm^2 rise in J_{SC}, leading to a net 0.2–0.3% absolute boost in the reported aperture-area *PCE*. The close agreement between our experimental results and device modelling further confirms that the all-surface J_0 is possibly in the range of 1–2 fA/cm^2.

Submicron-scale bevel passivation

Alkaline texturing of the crystalline silicon wafer inherently forms a slope transition region between the n-type polycrystalline silicon contact area and the adjacent i-a-Si:H and p-a-Si:H emitter regions. leveraging the high etching selectivity between the tunnel oxide and n-poly-Si, this process yields a well-defined plateau bevel structure with a characteristic width *W* typically under 1 µm. Following the final diluted hydrofluoric acid cleaning step, the highly doped crystalline silicon surface is fully exposed with a nominal dopant concentration on the order of 10^{19} cm^{-3}. Fig. 2b highlights the additional J_{rec} increase based on the fact that the interface field effect is partially neutralized by phosphor doping. With an additional weakness from either D_{it} or Q_{it}, such as localized elevation in interface defect density or corner-related electric field crowding, the recombination current density could increase by two orders of magnitude. To address this limitation, we introduce a dedicated bevel passivation sequence, which integrates a 2-step n-poly growth and supplementary etching steps prior to standard RCA cleaning for i-a-Si:H deposition. This passivation treatment concurrently generates a controlled nanotextured surface, which is also crucial for minimizing contact resistivity and ensuring long-term metallization reliability in finished devices. Cross-sectional characterization confirms that the modified surface features a well-defined depth *d* ranging from 30 to 100 nm (Fig. 2c). The insert in Fig. 2d presents electrochemical capacitance-voltage (ECV) measurements of the activated phosphor doping profile: the noncontact area exhibits a nearly uniform doping concentration of 4x10^{19} cm^{-3}, while the laser SE boosts the interface doping concentration to 1x10^{21} cm^{-3} and the subsequent nanotexturing further pushes the value to 1x10^{22} cm^{-3}.

Fig. 2a compares the photovoltaic performance of devices fabricated with the optimized bevel passivation process against a baseline control group. While there are measurable improvements across high-performance devices, the most pronounced benefit of this engineering strategy lies in the substantial enhancement of the FF stability. When implemented in a large-scale manufacturing workflow on 135 μm-thick absorbers, this process yields a median V_{OC} of 748–749 mV, a median *PCE* of 27.4%, and a maximum full-area *FF* reaching 87.2%,

Minority carrier lifetime (MCL) measurements were performed using a Sinton WCT-120[21,22,23] system. Fig. 3a presents a direct comparison of all-surface MCL curves. The reference SHJ sample exhibits an MCL of 12 ms at an excess minority-carrier-density (MCD) of $1x10^{15}/cm^3$, over 5 ms at a high-injection MCD of $1x10^{16}/cm^3$, and an overall all-surface J_0 as low as 1.06 fA/cm^2. In contrast, the THBC sample delivers an MCL of 16 ms at $1x10^{15}/cm^3$, 5 ms at $1x10^{16}/cm^3$, and an all-surface J_0 of 1.4 fA/cm^2 correspondingly. The MCL samples are collected after laser SE steps and prior to transparent conductive oxide (TCO) sputtering and have undergone all preceding fabrication processes. Further data deconvolution reveals an intrinsic bulk lifetime of 15~20 ms for the SHJ sample and about 30 ms for the THBC sample. Given that all devices were fabricated from identical incoming silicon wafers, the difference in bulk performance can be attributed to the sustained phosphorus silicate glass (PSG) gettering effect[24] originating from the n-poly process. We have plugged in the Cox–Strack method[26,27,28] to find the contact resistivity for different passivation contacts and the results are compared in Fig. 3c. Some are further partitioned with the TLM method[25]. The measured contact resistivity integrates contributions from the passivation film/c-Si substrate interface, the vertical resistance of the bulk film, and the passivation film/TCO/metal paste stack interface. The n-poly-Si contact exhibits a lower ρ_c than the oxygen-doped n-nc-Si:H, a typical window layer for SHJ. With laser SE modification, the p-a-Si contact achieves a comparable ρ_c as that of the p-nc-Si:H contact. Even with partial contact coverage (60% for the p-type contact, 35% for the n-type contact), the total FF loss introduced by these passivation contacts is limited to only 0.2–0.3%. With three times the metal-paste amount, the FF loss from the line resistance is also suppressed to below 0.15%. For the record cells, the measured FF is nearly identical to the pseudo-FF (*pFF*) after combining the aperture-measurement artifacts. In addition to the Jan 2026 certification results, we further optimized the SiO_x/MgF_2 ARC stack, increasing J_{SC} from 42.46 mA/cm^2 to 42.62 mA/cm^2. The updated independent certification measurements report two new champion efficiencies of 27.88% and 28.00% with FF values approaching 88% and V_{OC} values of approximately 745 mV (Fig. 3c).

A large-area THBC module

We screened the highest-performance devices from our pilot production line, yielding a subset of top cells with a median *PCE* of 27.5%, V_{OC} of 749 mV and *FF* of 87.0%. With a low-temperature lamination soldering process, 6 strings of cells are first connected in series and then arranged in parallel to form a 90-cell in total, customer-made module for effective area measurement. Independent certification was performed in TUV SUD and the corresponding record module result is shown in Fig. 4a. Measured with a long-pulse solar simulator, the packaged module delivers a stabilized FF of 84.85% after repeated forward scans and backward scans, with a measured hysteresis below 0.1%. Owing to the high maximum output current of 15.7 A in this device category, an additional 0.3–0.5% FF loss originates from the electrical resistance of the junction box interconnections.

To accurately resolve the intrinsic cell-level *FF* performance, we establish a large area module benchmarking framework as an independent cross-validation method. Fig. 4 compiles historical champion module efficiencies dating back to SunPower's 21.4% record reported in 2009. For consistent comparison across different device formats, both the J_{SC} and V_{OC} are normalized by the number of cells and the certified total aperture area. All processed datasets are compiled in Extended Data Table 2. In principle, TBC has a similar J_{SC} as the hybrid BC counterpart, with identical Si absorber thickness. However, a consistent performance gap of roughly 2mV for V_{OC} and about 2% for *FF* persists between these two architectures, which can be quantitatively attributed to differences in internal recombination suppression and contact resistivity. The performance advantage originates primarily from the field-effect-based hole-selective emitter in our THBC design, in contrast to the conventional diffusion-based contact in the TBC structure.

For THBC technology to be qualified as a cost-effective industrial solution, full compatibility with copper metallization must be demonstrated. As shown in Fig. 4c, a set of mini-modules were subjected to highly accelerated damp heat stress testing (HAST). Compared with the industrial TOPCon baseline, THBC modules integrated with SHJ-derived hole-selective emitters exhibit exceptional long-term stability after more than 3 weeks of extended testing. Without an effective Cu diffusion barrier in the isolation trench, however, the devices suffered from rapid performance degradation in the initial stage of stress testing. By introducing a patented capped CSTL layer, the THBC modules achieve stability parity with the TOPCon reference devices and reliably pass the 3-fold IEC test in the category of damp heat degradation.

Discussion

We demonstrate a THBC solar cell architecture with a certified champion efficiency of 28.00%. Based on Auger recombination dominance, the V_{OC} x *FF* performance has reached 98.5% of the theoretical Shockley–Queisser limit. This exceptional cell-level performance is

further validated by an independently certified module result of 26.74%. Beyond representing a leading device architecture towards the 29.4% limit for single junction Si solar cells, this work confirms the manufacturability of the THBC platform, with demonstrated tolerance to thinner silicon wafers, and full compatibility with ongoing copper paste metallization. Looking ahead, we project that this architecture will enable cell efficiencies exceeding 28.5% and large-area module efficiencies above 27% in the immediate near term.

Methods

Cell and module fabrication

The complete THBC device is fabricated via a sequentially optimized, industrial-compatible process flow, detailed as follows:

Step 1. Wafer polishing and precleaning: N-type c-Si (n-c-Si) wafers are first chemically polished in alkaline solution to remove saw damage, followed by a standard RCA cleaning sequence to eliminate surface organic contaminants and metallic impurities.

Step 2. LPCVD SiO_2/ i-a-Si stack: In a low-pressure chemical vapor deposition (LPCVD) furnace, an ultrathin tunnel SiO_2 layer with a controlled thickness of 1–2 nm is thermally grown, followed by in situ deposition of the intrinsic amorphous silicon (i-a-Si) layer.

Step 3. Phosphorus diffusion and in situ gettering: During the phosphorus diffusion process, the amorphous silicon (i-a-Si) layer deposited by LPCVD is fully recrystallized and doped with phosphorus atoms, thereby forming an n-poly-Si layer. The phosphorus diffusion process also delivers a highly effective gettering effect for metallic impurities in the n-c-Si bulk. At a high diffusion temperature close to 900 °C, most metallic impurities from the n-c-Si bulk segregate into the heavily doped n-poly-Si layer rather than being trapped in the ultrathin tunnel SiO_2. A fraction of surface-adjacent impurities further migrates into the PSG layer formed during phosphorus diffusion. This tailored gettering mechanism substantially reduces bulk metal contamination and elevates MCL, without introducing severe parasitic recombination across the ultrathin tunnel oxide.

Step 4. PSG removal: The PSG layer, together with all captured metallic impurities, is completely stripped in a dilute hydrofluoric (HF) wet cleaning step.

Step 5. Mask deposition: A dielectric layer composed of SiN_x, SiO_xN_y or their laminated structure is deposited on the rear side of the wafer, acting as an etching mask in the subsequent wet texturing and cleaning processes.

Step 6. Laser patterning: A picosecond laser with a flat-top intensity is used to selectively ablate the predefined regions of the dielectric mask.

Step 7. Double-sided texturing, mask stripping and n-poly-Si nanotexturing: A temperature-regulated dilute alkaline solution is employed to etch and fully remove the n-poly-Si /tunnel oxide stack in both the exposed local regions and the wrapped-around areas extended onto the front side of the wafer. The exposed bare silicon regions then undergo a standard double-sided alkaline texturing process to form uniform random pyramid morphologies. The remaining dielectric mask layer is completely removed in a subsequent cleaning step. After all the alkaline treatments, the n-poly-Si surface undergoes mild anisotropic etching to form a uniform distribution of nanoscale pit-like textures. The pit depth and spatial distribution are precisely controlled by adjusting the alkaline solution concentration, temperature and processing time, ensuring that the textured structure does not penetrate the full thickness of the n-poly-Si layer.

Step 8. AlO_x/SiN_x (ARC) deposition: The front-side AlOx and SiN_x stacks provide synergistic surface passivation and anti-reflection performance. The tube-type atomic layer deposition (ALD) process achieves full-wafer Al_2O_3 coverage across all surfaces, while the subsequent SiN_x PECVD process naturally forms a thin wraparound SiN_x layer on the rear side.

Step 9. Wraparound AlO_x/SiN_x removal and final predeposition cleaning: The wraparound AlO_x and SiN_x layers on all surfaces except the front side are completely stripped by a precisely controlled diluted HF solution. Then the wafer is processed with a full standard RCA solution sequence to eliminate all residual surface contaminants.

Step 10. i-a-Si/p-a-Si stack deposition: The intrinsic a-Si:H and p-type doped a-Si:H layers are sequentially deposited in a low-temperature PECVD furnace.

Step 11. Laser patterning to remove the i-a-Si/p-a-Si stack: A picosecond laser with a flat-top intensity profile is applied to selectively ablate the predefined regions of the i-a-Si/p-a-Si stack. The optimized laser process fully removes the i-a-Si/p-a-Si stack layer without penetrating the underlying doped n-poly-Si layer.

Step 12. Laser SE: Two independent laser selective doping steps are implemented. The first laser SE process targets local n-poly-Si regions, elevating the phosphorus doping concentration within the near-surface region of several tens of nanometers. The second laser SE treatment is applied to the adjacent p-a-Si region, which raises the boron effective active doping concentration in the local contact region. The two-step laser treatment significantly reduces the contact resistance between the TCO layer and the two types of doped silicon layers, while preserving the integrity of the rear-side passivation structure.

Step 13. TCO film deposition: A TCO layer is deposited on the entire rear side of the

wafer via magnetron sputtering.

Step 14. TCO isolation: This process precisely removes the TCO material located in the gap between the n-type contact region and the p-type contact regions via localized laser ablation or selective chemical etching, forming an electrically isolated nonconductive trench.

Step 15. CSTL coating: The CSTL protective layer is fabricated to fully cover the TCO isolation region. This dense barrier layer effectively blocks moisture, residual impurities and metal ions from penetrating into the narrow isolation gap, preventing the reformation of shunt paths.

Step 16. Metallization: A metallization method is performed after the CSTL step. This process includes a precision-aligned screen-printing step on the exposed n-type and p-type TCO regions, followed by a low-temperature curing step performed below 300 °C. This metallization structure forms a stable ohmic contact between the metal electrodes and the TCO transport layers, and the CSTL isolation barrier prevents the metal paste or metal ions from infiltrating the TCO isolation trench.

Integrated film covering (IFC) technology was adopted for interconnect techniques in our module. The IFC-based 0BB process starts by positioning the ribbon onto the carrier film, followed by arranging the cells on top of this preformed structure. The carrier film is slightly melted at approximately 100 °C to create adhesion. A final lamination occurs at a low temperature of 150 °C for 20 minutes to enable alloying between the ribbon and silver paste. With an overlap of 1–1.5 mm between cells, a flat ribbon with a width of 0.8 mm was used to connect neighbouring cells.

Measurement and characterization

The MCL post-CVD passivation was characterized by a Sinton WCT-120 tool. A standard transient photoconductance decay technique was applied to obtain the inverse lifetime versus excess carrier density curve. After subtracting the Auger recombination, the interception of the derived curve corresponds to the intrinsic bulk lifetime, and the slope is proportional to the saturation recombination current density J_0.

The contact resistivities were measured following the standard Cox–Strack method, where square contact area (instead of conventional circular patterns) was adopted to precisely match the design of the laser DOE. The metal contact area was varied from 3 mm to 15 mm and defined by a metal hard mask, specifically fabricated for precise alignment during TCO and silver evaporation. To further isolate the contribution from the TCO/metal interface to

the total contact resistivity, the transmission line method (TLM) was also implemented on selected samples (Extended Data Fig. 2e, 2f).

For the batch cell I-V testing in Fig. 2a, a HALM I-V tester with an advanced hysteresis measurement mode was deployed to compare performance across different pilot-line run batches. The tester features a 26-busbar rear-side contact design with a front-side glass covering, achieving Class AAA irradiance nonuniformity and temperature stability across a 210 mm × 210 mm measurement area. The series resistance-induced FF correction is calibrated against a golden reference traceable to the ISFH standards, and both V_{OC} and J_{SC} measurements are fully aligned with the ISFH calibration protocols. Champion cells are sent to ISFH CalTec for independent I-V characterization, including the spectrum response (SR).

For the top-performing module certification, a 90-cell module was laminated and assembled into a 1762 mm × 1134 mm frame. The nonactive area was masked out, yielding an effective measurement aperture of 1.677 m^2. The measurement was performed at TUV SUD with a DLSK photovoltaic module IV tester. The test repeatability is less than 0.1% and a repeating forward scan and backward scan are applied until the measured hysteresis is suppressed below 0.1%.

Device simulation

All auxiliary finite element postprocessing and parameter calibration procedures in this work are implemented on the open-source FEniCS framework, using standard second-order Lagrange elements and the default PETSc linear solver backend. No custom numerical algorithm that forms the core novelty of this work is involved in this part of the workflow.

To simulate the impact of charged-induced hole accumulation, we set up a probe inside the n-c-Si absorber at a depth of 3 µm from the interface, where the quasi-Fermi level separation is defined by a forward bias V_a, and the recombination current J_{rec} across the right boundary is calculated. The full simulation scheme and layout are illustrated in Extended Data Fig. 3. When the surface recombination is small (J_0 < 5 fA/cm^2), the recombination current operates in a surface-reaction-limited regime, and the resulting fit yields a standard ideality factor n=1 J-V characteristic, as shown in Extended Data Fig. 2d. For all our simulation work reported here, we adopt an n-type doping of 2.5x10^{15} cm^{-3} (or bulk resistivity of 2.2 Ω.cm), although the simulation result from Fig. 1b is insensitive to variations in doping concentration or doping polarity.

The two-dimensional solar cell device simulations presented in this work (Fig. 1c) were performed using the open-access PC2D software developed by the UNSW PV research team.

The authors thank the team for making this simulation tool publicly available for academic research. The original version of PC2D was modified to incorporate finer grid resolution and an updated value on the Auger recombination coefficient[31] to reflect the recent advances that align the theoretical efficiency limit of silicon solar cells with the established 29.4% benchmark. Furthermore, all device simulations have been independently validated using the Sentaurus TCAD software suite (H-2013.03 version).

Data availability statement

The source data files are provided within the supplementary document.

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Author contributions

Z.X. designed the experiments, wrote the manuscript and was responsible for the simulation. Y.H. led the process integration and contributed to Extended data Fig.1. J.Z. was the head of TOPCon passivation. C.G. and Y.J. were PECVD process and hardware owner. R.L. and L.L. were working on both cell and module integration and were also responsible for metallization. D.X. was in charge of cell characterization and certification. X.P., X.J., and Q.W. worked on module engineering and improvement. G.Y. was involved in the discussion for device optimization. Y.C. and J.G. set the research and development plan and provided technical guidance. All the authors provided feedback and comments.

Declaration of interests

The authors declare that they have no competing interests.

Materials & Correspondence

Further information and requests for resources and materials should be directed to and fulfilled by the lead contact Zhigang Xie (zhigang.xie@trinasolar.com).

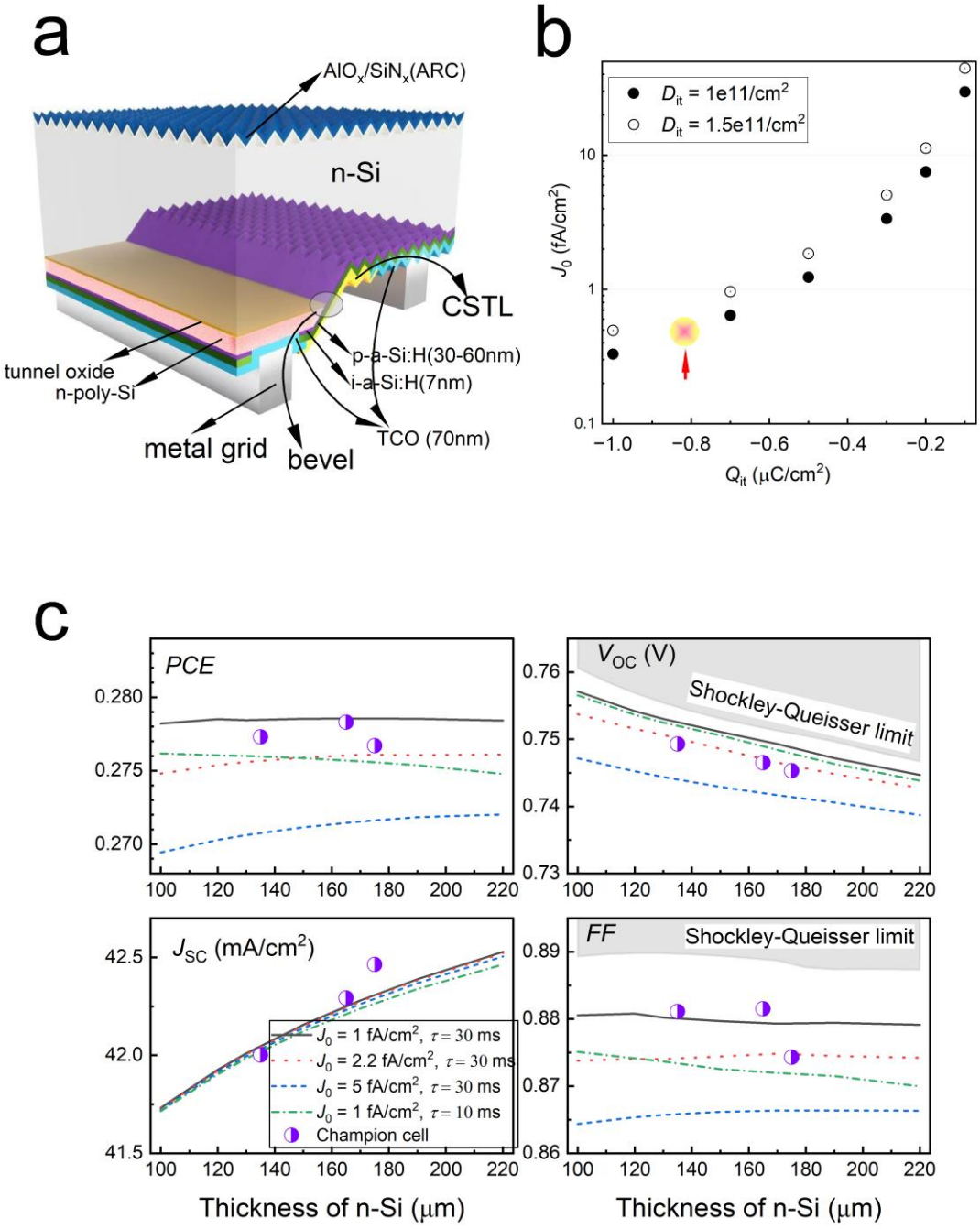
Figure captions

Fig. 1 | THBC cell structure, device sensitivity simulation and matching with the record cells. **a**, The THBC cell structure with a front-side AlO_x/SiN_x stack as the ARC layer and interdigitated backside passivation contact. The hole-selective contact comes from a typical SHJ cell with SE, but the tunnel oxide/n-poly contact is primarily based on TOPCon. **b**, Surface passivation simulation based on an interface field effect, with a negative charge Q_{it} and normalized defect density D_{it}. J_0 is a normalized surface recombination current. **c**, Device parameter simulation based on a 2D drift-diffusion model including a typical behaviour in the bulk-recombination-limited regime (J_0 = 1 fA/cm^2 and τ = 10 ms) and another group of surface-reaction-limited regimes (J_0 varies from 1 fA/cm^2 to 5 fA/cm^2, but with τ = 30 ms). The cells certified by ISFH CalTec are from one process batch with a wafer resistivity of 1–2 Ω·cm. As a comparison, the simulation results from Shockley–Queisser limit are presented.

Fig. 2. | Bevel passivation on the transition slope and nanotexturing on the TOPCon contact. a, THBC cell results based on a pilot-line run, targeting a comparison from the baseline (control) to the bevel passivation group. Each group was repeated twice in an identical setup. time are processed and measured. In particular, the cell efficiency (*PCE*), J_{SC}, V_{OC} and *FF* are shown as notched boxplots with the 1st and 3rd quartiles as the boundary and median values at the notch. The whiskers are shown to guide the outliers. **b**, The surface recombination current at the bevel area with the existence of residual phosphor doping starting from 1x10^{19} cm^{-3}. Insufficient cleaning due to the corner effect may affect PECVD deposition and increase the defect density population. **c**, STEM image for a cross-sectional view of the transition slope and the bevel area. "W" refers to the width of the bevel and "d" refers to the etching depth from the bevel passivation effect. The scale bar is 2 μm. **d**, STEM and EDX for the details of the tunnel oxide/n-poly-Si contact. Between the Si absorber and n-poly-Si film, there is a 1–2 nm tunnel oxide. From the phosphor mapping, there is accumulation in both the grain boundary and tunnel oxide. This cross-section also highlights the nanotexturing effect from this bevel passivation step. The insert shows ECV measurements from the noncontact area, laser SE area and nanotexturing area.

Fig. 3. | A combination approach of cell improvement from both the control of internal/surface recombination and contact resistivity optimization. **a**, Minority carrier lifetimes are measured for both samples with a Sinton WCT-120. Given that the bulk lifetime can reach 30 ms, the minority lifetime measured at an injection level of $1x10^{15}/cm^3$ is improved from 12 ms (SHJ) to 16 ms (THBC), whereas at an injection level of $1x10^{16}/cm^3$, the MCL is at 5 ms at the same level as the SHJ comparison. **b**, Contact resistivity measurement from a Cox–Strack method for THBC contacts. As a direct comparison, the passivation contacts from TBC and SHJ are listed from the same measurement arrangement. The contact resistivities are collected after the actual processing steps. For example, i-a-Si:H and p-a-Si:H films were laminated on top of an n-poly-Si stack and went through laser ablation steps to include any possible residual effect. **c**, Record cell results from certificates of ISFH CalTec. Compared to the previous batch of record cells, the efforts come from ARC optimization (a J_{SC} increase from 42.46 mA/cm^2 to 42.62 mA/cm^2 for a Si absorber thickness of around 160 μm).

Fig. 4. | The champion module results and reliability test for a process compatibility with low-cost copper paste application. a, The certified result from TUV SUD. The module has 90 units of THBC cells and the mask has taped out the ineffective area for an aperture measurement. The normalized V_{OC} is achieved from the total voltage divided by the number of cells in the series connection. **b**, A comparison of all notable results from BC technologies including TBC, HBC and hybrid BC. The original values are listed in Extended Data Table 2 and come from Martin Green's Solar Cell Efficiency Table. For a straightforward comparison, all parameters (V_{OC} and J_{SC}) are normalized to an average cell inside the module. **c**, Reliability test results including a baseline TOPCon group, THBC cells with Ag paste, THBC cells with CSTL layer and different metallization solutions. The samples were prepared with a sandwiched double glass structure to simulate the actual commercial module, and the gap from the cell edge to the glass edge was approximately 2 cm. The HAST condition refers to a 121 °C temperature and 2 atmosphere pressure setting. For example, "HAST 192 hr" refers to a test duration of 192 hours at this setup. All test groups are executed in two separate batches. The test group of pristine THBC cells (without CSTL) failed quickly and and was stopped at 96 hours. The optimized THBC with CSTL can pass the HAST 576 hr test, which is at least equivalent to a damp heat test of 5000 hours and more than IEC 3x in terms of damp-heat degradation concern.



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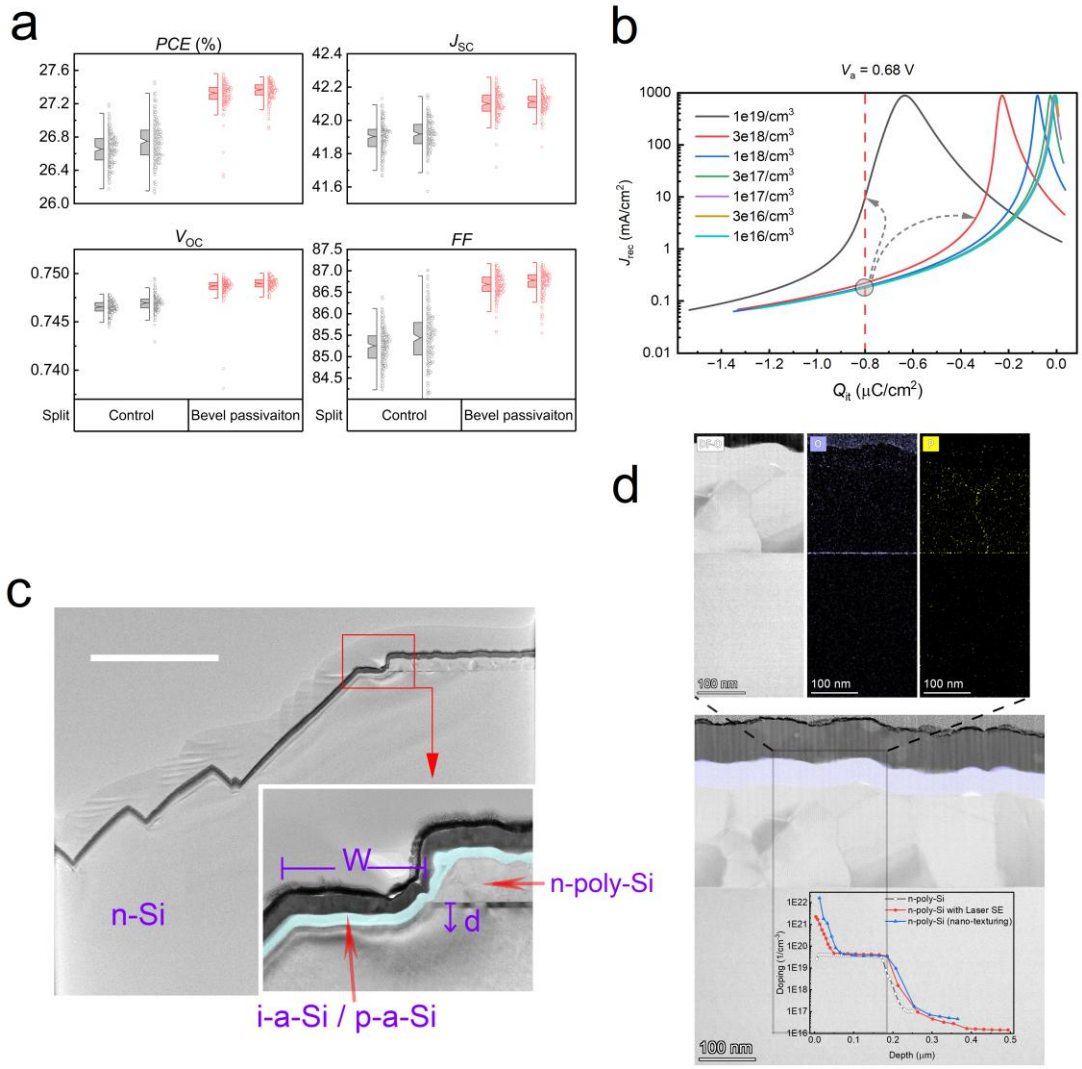
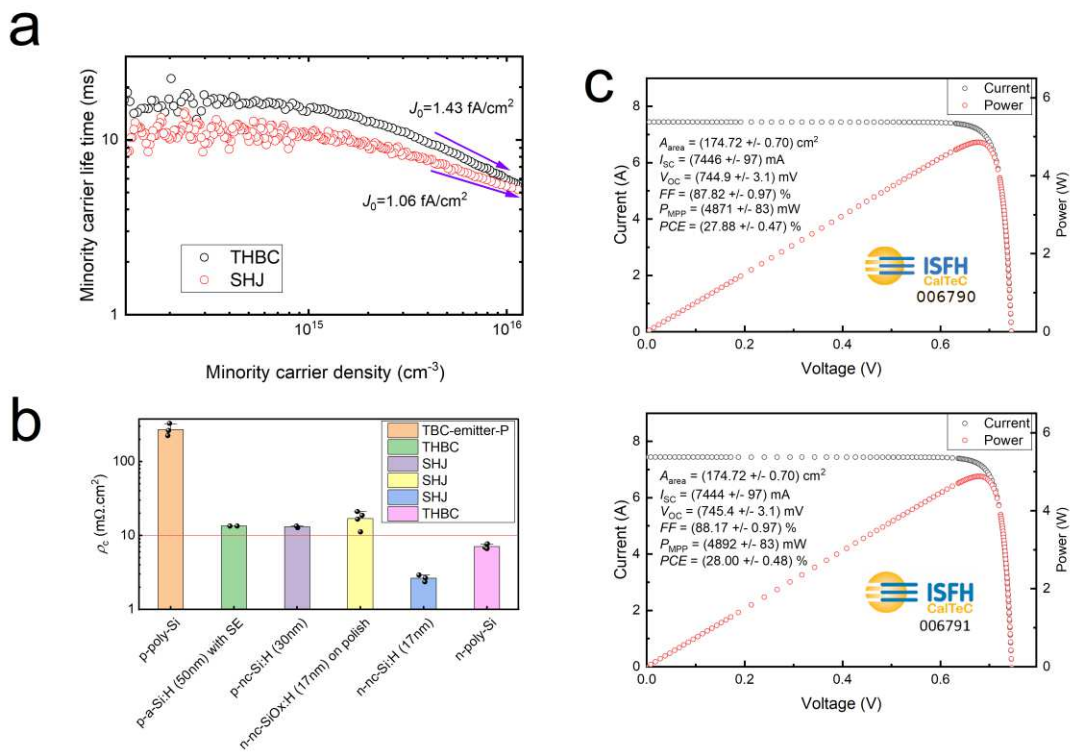


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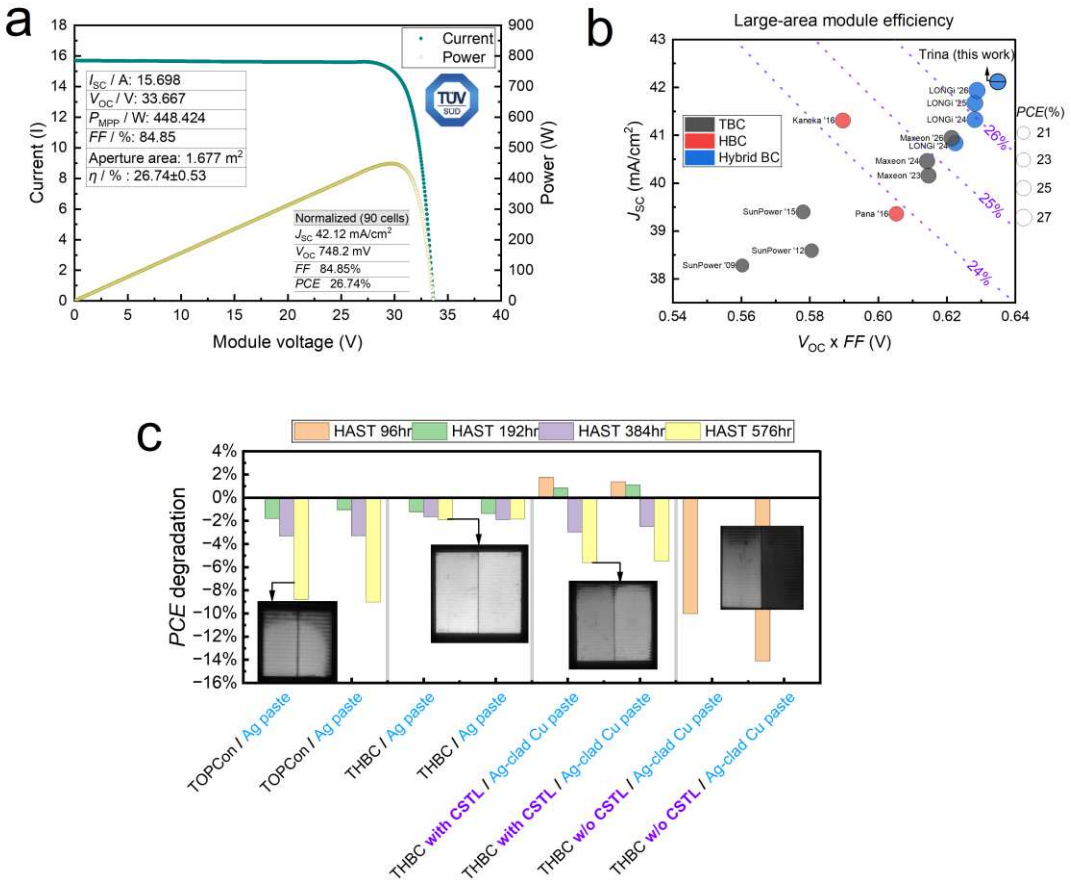


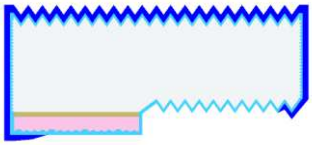
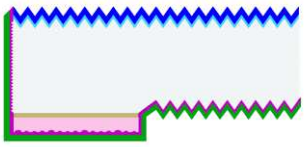
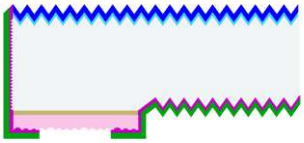
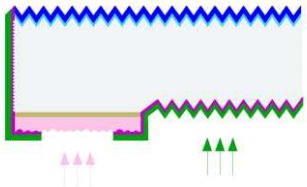
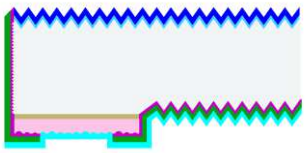
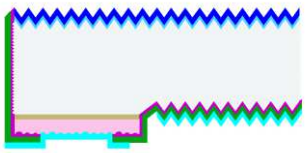
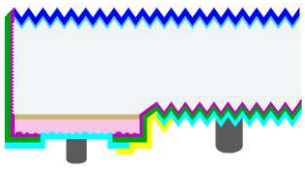
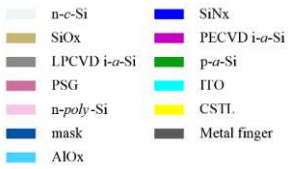
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Cell Name	*PCE*	V_{OC}	*FF*	J_{SC}	V_{OC} x *FF*	Data source
	%	mV	%	mA/cm^2	V	
THBC Cell1	27.73	749.3	88.11	42.00	0.660	This work
THBC Cell2	27.83	746.4	88.15	42.29	0.658	This work
THBC Cell3	27.67	745.3	87.43	42.46	0.652	This work
THBC Batch2A	27.88	744.9	87.82	42.62	0.654	This work
THBC Batch2B	28.00	745.4	88.17	42.61	0.657	This work
LONGi	27.81	744.9	87.55	42.64	0.652	*Nature* **647**, 369 (2025)
GS Solar	27.62	740	87.73	42.54	0.649	*Nature* **652**, 650 (2026)

Extended data Table 1 | The recent top certified cell results. THBC Cell1/Cell2/Cell3 are from one process batch, and THBC Batch2A/2B are from the 2nd batch with further optimization on the front side ARC layer.

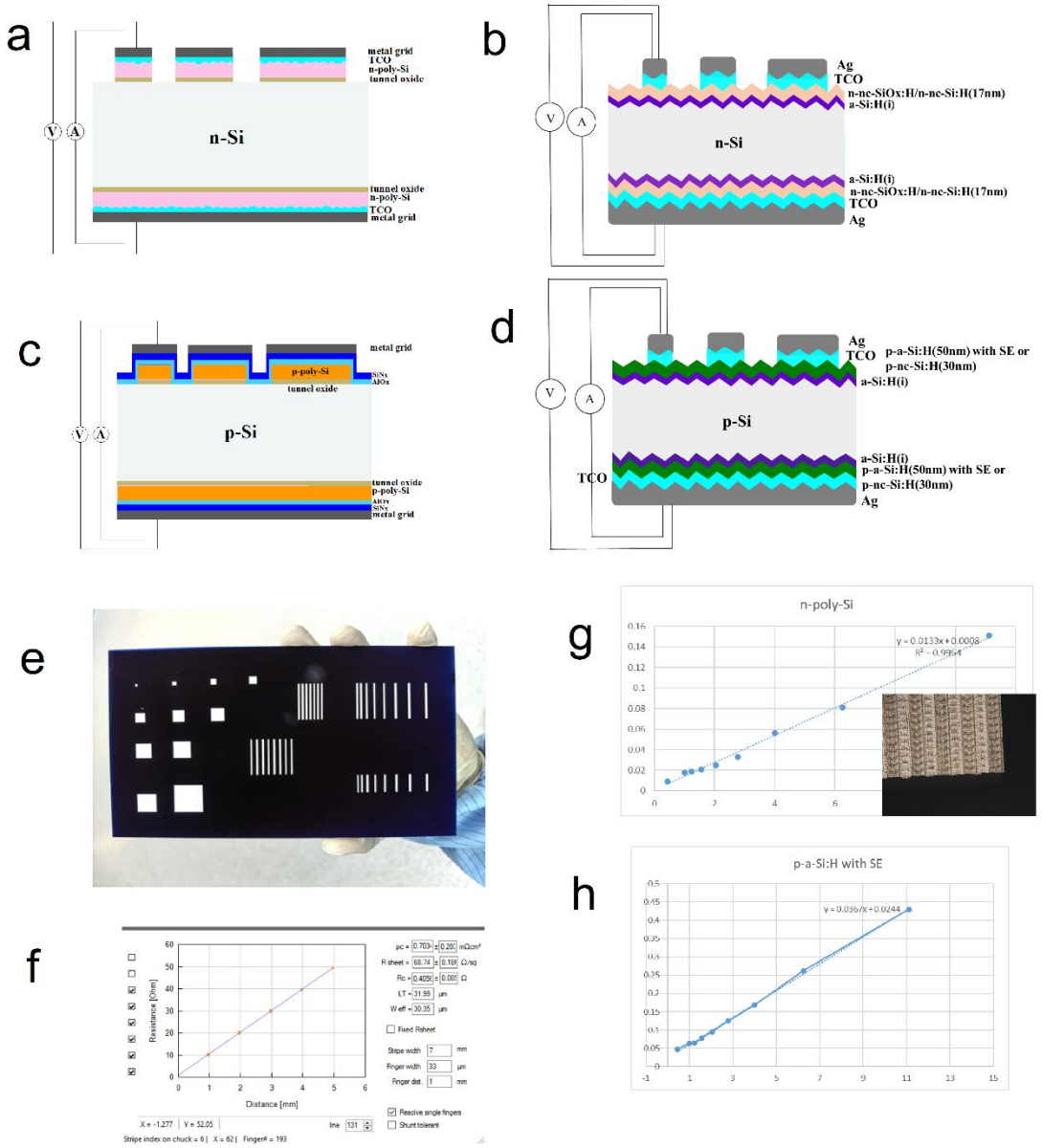
Record	*PCE*	Area	V_{OC}	J_{SC}	*FF*	Test centre (date)	Description
	%	m^2	mV	(mA/cm^2)	%		
1	21.4±0.6	1.578(ap)	714.6	38.28	78.4	NREL (Oct 2009)	SunPower (TBC 96 cells)
2	22.4±0.6	1.5775(ap)	724.7	38.59	80.1	NREL (Aug 2012)	SunPower (TBC 96 cells)
3	22.8±0.6	1.57389(ap)	722.5	39.4	80	NREL (Jun 2015)	SunPower (TBC 96 cells)
4	23.8±0.5	1.1562(ap)	741.7	39.36	81.6	AIST (Jan 2016)	Panasonic (HBC 72 cells)
5	24.4±0.5	1.3177(ap)	736.1	41.31	80.1	AIST (Sep 2016)	Kaneka (HBC 108 cells)
6	24.7±0.3	1.7806(ap)	741.4	40.16	82.9	NREL (April 2023)	Maxeon (TBC 112 cells)
7	24.9±0.3	1.7753(ap)	741.8	40.46	82.8	NREL (Jan 2024)	Maxeon (TBC 112 cells)
8	25.4±0.3	1.8342(ap)	746.3	40.84	83.4	FhG-ISE (July 2024)	LONGi (HTBC 108 cells)
9	26.0±0.3	1.8156(ap)	747.8	41.33	84.0	NREL (Dec 2024)	LONGi (HTBC 108 cells)
10	26.2±0.4	1.8829(ap)	747.8	41.67	84.0	FhG-ISE (Aug 2025)	LONGi (HTBC 108 cells)
11	26.4±0.3	1.9132(ap)	745	41.94	84.4	NLR (Jan 2026)	LONGi (HTBC 108 cells)
12	25.4±0.3	1.8217(ap)	746.8	40.94	83.2	NLR (April 2026)	Maxeon (TBC 120 cells)
This work	26.74±0.53	1.677(ap)	748.2	42.12	84.85	TUV SUD (Oct 2026)	Trina (THBC 90 cells)

Extended data Table 2 | The historical champion data on the large-area module (with an aperture area above 1 m^2). The normalized V_{OC} and J_{SC} values are extracted for the convenience of the cell-to-module CTM calculation. From Records 1 to 12, the data for sourcing come from Martin Green's "Solar Cell Efficiency Table" (versions 39, 42, 47, 48, 49, 62, 63, 64, 66, 67 and 68, respectively).

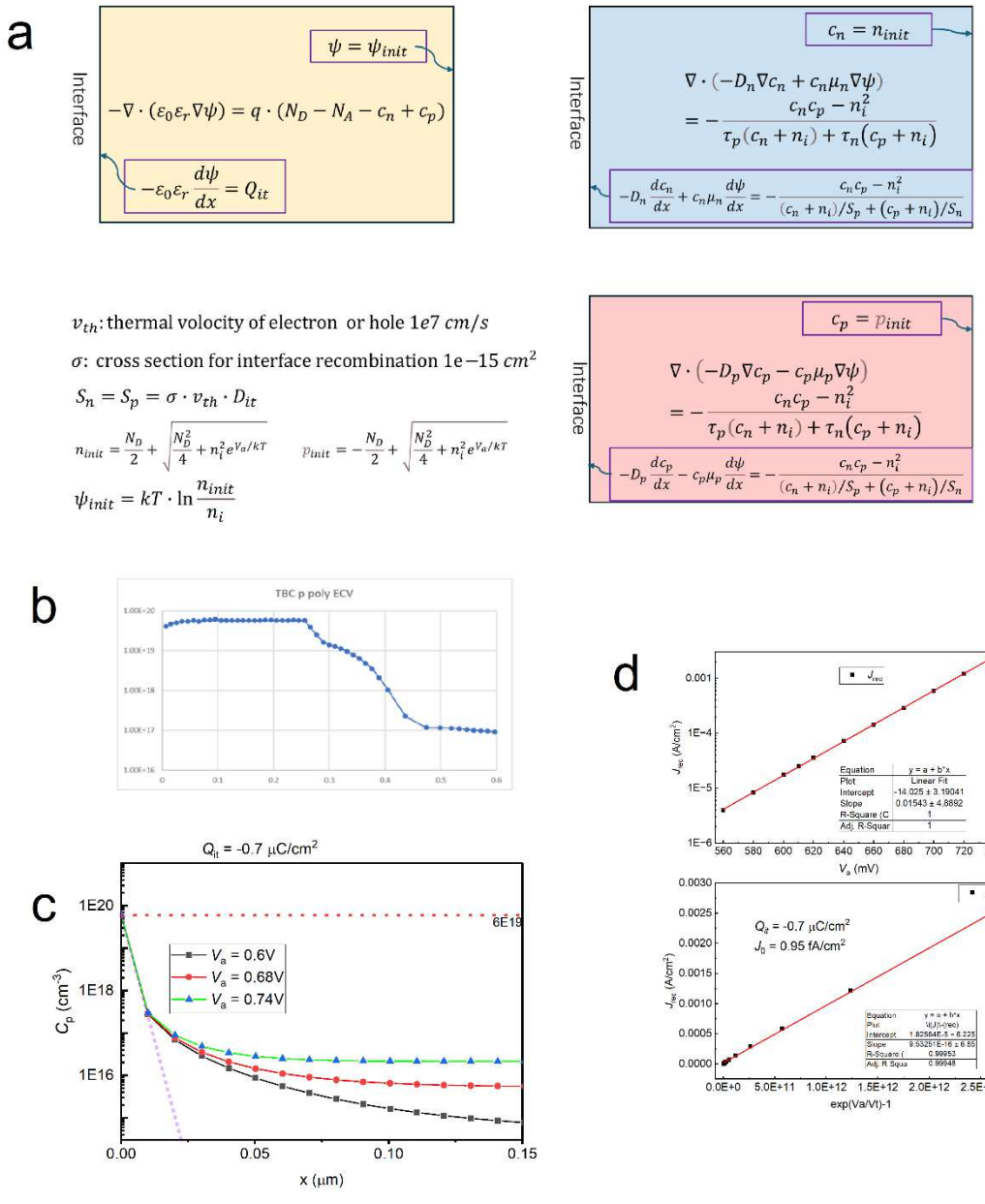
Step 1. Polishing, cleaning	Step 2. LPCVD SiOx/i-*a*-Si stack	Step 3. Phosphorus diffusion, SiO_2/n-*poly*-Si/PSG stack, gettering
		
Step 4. PSG removal	Step 5. Mask deposition	Step 6. Mask laser patterning
		
Step 7. Double-sided texturing, mask removal, n-poly-Si nano-texturing	Step 8. AlOx/SiNx (ARC) depositon	Step 9. Wraparound AlOx/SiNx removal, cleaning
		
Step 10. i-*a*-Si/p-*a*-Si stack deposition	Step 11. i-*a*-Si/p-*a*-Si stack laser patterning	Step 12. Laser SE
		
Step 13. TCO film deposition	Step 14. TCO isolation	Step 15. CSTL
		
Step 16. Metallization		
		

596

597 **Extended Data Fig. 1 | A THBC cell structure and related process flow.** Step 7 is a
598 nanotexturing step for n-poly-Si, which is designed to assist bevel passivation and n-type
599 area contact. Step 12 completes the last step of device passivation, and our MCL sample is
600 collected after this step. Step 15 is designed for copper paste metallization and CSTL is a
601 patented material for cell and module reliability.



Extended Data Fig. 2 | Contact resistivity measurement setup, particularly with the Cox–Strack method. a, n-Si/tunnel oxide/n-poly-Si structure. **b**, n-Si/i-a-Si:H/n-nc-Si:H structure. **c**, n-Si/tunnel oxide/p-poly-Si structure. **d**, n-Si/i-a-Si:H/p-a-Si:H with SE. **e**, The metal hardmask for TCO and Ag deposition is designed to match the square shape of the DOE for laser ablation. **f**, A TLM measurement result to verify the contact opening via laser ablation. **g**, A typical contact resistivity measurement curve for tunnel oxide / n-poly-Si from the Cox–Strack method. **h**, A typical contact resistivity measurement curve for i-a-Si:H / p-a-Si:H with laser SE.



611

612 **Extended Data Fig. 3 | Simulation scheme and results for field-effect-based surface**
613 **passivation. a**, Simulation scheme based on a 1D or 2D drift-diffusion model, for hole
614 selective contact or surface passivation. The left side is the interface (either Si/AlO_x or Si/i-a-
615 Si:H). A probe is set up at the right side to pick up the recombination current from the bulk Si
616 absorber. **b**, ECV measurement to determine the dopant profile for a diffusion-based contact
617 with a depth of at least 200 nm. **c**, A hole accumulation phenomenon due to a negative
618 surface charge density of -0.7 µC/cm^2. The hole concentration is simulated with a forward
619 bias of 0.6 V, 0.68 V and 0.74 V. The peak intensity is close to 6x10^{19} cm^{-3} and similar to the
620 p-poly contact from the TBC device, but the equivalent junction depth is only 10–20 nm. **d**,
621 By changing the applied forward bias or surface Q_{it}, we can simulate the surface
622 recombination current and a typical J-Va curve is plotted. With a typical Q_{it} of -0.7 µC/cm^2, a

623 single side J_0 of 0.96 fA/cm^2 is extrapolated.