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Research Article

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Posted Date: November 17th, 2026

DOI: https://doi.org/10.21203/rs.3.rs-11736181/v1

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Additional Declarations: No competing interests reported.

Series compensation for the ride-through of current-limited grid-forming plants: a power ceiling, a planning criterion and hardware-in-the-loop validation

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Abstract

Grid-forming (GFM) plants limit their current during faults, and while limited they lose much of their ability to stay in synchronism. Many of these plants are connected through long transmission corridors that already carry, or could carry, a thyristor-controlled series capacitor (TCSC) or a static synchronous series compensator (SSSC). This paper asks when such a device can keep a current-limited GFM inverter in synchronism. For a virtual synchronous machine with current-reference saturation, the power transferred while the current is limited has a ceiling set only by the current limit and the grid voltage. Series compensation cannot raise this ceiling, and inserted inductance can only lower the power curve. What a series device can do is restore the post-fault equilibrium after a line outage. A closed-form minimum compensation for each N-1 outage turns this into a screening map that shows which outages need series compensation, how much, and which need a run-back instead. A coordinated scheme of a virtual-rotor angle freeze and a saturation-aware TCSC boost rode through 1 s faults in all 22 single-machine cases of a phasor study. A switched-thyristor Simulink model, a small-signal resonance study, a modified IEEE 39-bus system and controller-hardware-in-the-loop tests on three microcontroller boards support these findings. The hardware critical clearing times matched a desktop run of the same code within one 2 ms bisection step in 30 of 36 comparisons. On resistive corridors the boost can shorten the critical clearing time, so it should be armed only for the outages the map identifies.

Keywords Grid-forming inverter · Current limiting · Series compensation · Thyristor-controlled series capacitor · Transient stability · Hardware-in-the-loop

1 Introduction

Grid-forming (GFM) inverters are the main candidate to take over the voltage- and frequency-setting role of synchronous machines as inverter-based resources replace them (Milano et al. 2018; Matevosyan et al. 2019; Lasseter et al. 2020; Rosso et al. 2021). The stability classification was extended to converter-driven phenomena for this reason (Hatziargyriou et al. 2021; Gu and Green 2023). Most GFM schemes, including the virtual synchronous machine (VSM) or synchronverter (Zhong and Weiss 2011), power-synchronization control (Zhang et al. 2010) and frequency droop (D'Arco and Suul 2014), synchronize through a power loop with swing-like dynamics. Their large-signal behavior has therefore been studied with equal-area and phase-portrait arguments (Wu and Wang 2019; Pan et al. 2020; Fu et al. 2021), and damping-based remedies have been proposed (Xiong et al. 2021).

Current limiting breaks the analogy with a synchronous machine. During a close-in fault the current reference saturates at 1.1 to 1.5 pu, the inverter stops behaving as a voltage source, and its angle keeps advancing. This mechanism has been analyzed for droop control (Huang et al. 2019), current-limiting algorithms have been compared (Qoria et al. 2020), and the stability of GFM converters with current-reference saturation (CRS) has been assessed and improved (Rokrok et al. 2022). A circular limiter can be represented by an equivalent circuit (Fan and Wang 2022), fault recovery with priority-based limiters has been analyzed (Fan and Wang 2023), recovery conditions for CRS-limited converters have been derived (Arjomandi-Nezhad et al. 2025), and a virtual-power method widens the margin once the limit is reached (Kkuni and Yang 2024). Virtual-impedance limiting (Paquette and Divan 2015; Taul et al. 2020) and a review (Fan et al. 2022) complete this line of work. All of these remedies act inside the inverter, and all of the analyses treat the network as a fixed Thevenin source.

Series compensation acts on the network side. Fixed capacitors, the thyristor-controlled series capacitor (TCSC) and the static synchronous series compensator (SSSC) raise the transfer capability of long corridors and improve first-swing stability (Gyugyi et al. 1997; Hingorani and Gyugyi 2000; Mathur and Varma 2002), and stability models of the TCSC exist for this purpose (Kundur 1994; Paserba et al. 1995). For GFM inverters, published work on series compensation deals with subsynchronous oscillation (Islam and Kim 2024, 2026; Hossain and Chaudhuri 2025), and field events involving inverter-based resources on compensated lines have been reported (Cheng et al. 2023). No study has asked whether a controllable series reactance can keep a current-limited GFM inverter in synchronism, and the current-limited power-angle relations of Rokrok et al. (2022), Fan and Wang (2022) and Arjomandi-Nezhad et al. (2025) have not been examined with the network reactance as a control variable.

The question comes up in transmission planning. Large renewable plants are often connected through long double-circuit corridors where a TCSC is already in service or an SSSC is under consideration as part of a smarter, more controllable transmission grid. The obvious control is to insert inductance during the fault, to keep the inverter out of saturation, and maximum capacitance after clearing. This paper shows that the first step is counterproductive and that the benefit of the second is bounded by the current limit. The paper makes four contributions:

1. A closed-form power-angle relation for a VSM with CRS behind a series-compensated corridor. It shows that the limited power equals a ceiling that does not depend on the series reactance, that series inductance never adds synchronizing power, and that no reactance schedule can raise the first-swing critical clearing time (CCT) above an equal-area bound on the ceiling.

2. A closed-form minimum post-fault compensation for N-1 outages and a screening map. Before any time-domain study, the map tells the planner whether an outage needs inverter-side measures, series compensation (and how much) or a run-back.

3. A coordinated scheme of an inverter-side angle freeze and a saturation-aware TCSC boost with a topology-aware release. It uses only local signals and rode through 1 s faults in all 22 single-machine cases. The paper also states when the boost should not be armed.

4. Validation at four levels: a MATLAB/Simulink model with a switched-thyristor TCSC fired from the capacitor voltage, a small-signal study of the series-resonance mode, a modified IEEE 39-bus system, and controller-hardware-in-the-loop (CHIL) tests in which the inverter and TCSC controllers run on separate microcontrollers against a real-time plant.

Earlier studies of current-limited GFM inverters improve the inverter controls for a given network. This paper keeps the inverter controls simple and asks what the network device can and cannot add. The answer is an upper bound and a sizing rule, which a planner can apply before choosing between inverter-side measures, a series device and a run-back.

Online Resource 1 gives the full result tables, the sensitivity and model-variant studies, the details of the Simulink and 39-bus models, and the CHIL set-up and results.

2 System model

Fig. 1 shows the study system. A GFM inverter is connected through its virtual and filter reactance X_v to the point of common coupling (PCC). A series device sits at the sending end of a corridor of two parallel circuits, each of reactance X_{L1}. The corridor ends at bus B, behind which a Thevenin grid has voltage V_g and reactance $X_s = 1/SCR$. All quantities are in per unit on the inverter rating. A three-phase fault through X_f is applied at bus B; in the N-1 cases, circuit 2 trips at clearing.

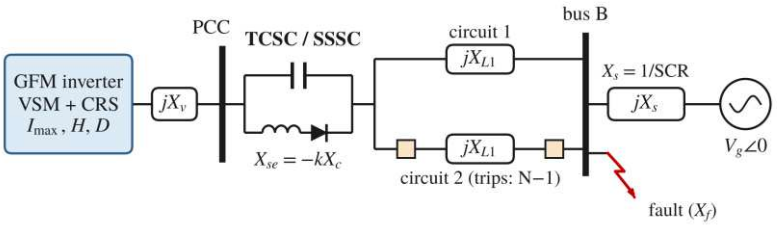


Fig. 1 Study system: GFM inverter, series device (TCSC or SSSC) at the sending end of a double-circuit corridor, and Thevenin grid at bus B

The inverter (Fig. 4a) synchronizes through a VSM,

$$\dot{\delta} = \omega_b(\omega - 1), \qquad 2H\dot{\omega} = P_{ref} - P - D(\omega - 1), \tag{1}$$

where δ is the angle of the internal voltage E, $\omega_b = 2\pi \cdot 50$ rad/s, H is the virtual inertia and D the damping (droop) gain (D'Arco and Suul 2014). The unsaturated current reference follows from the virtual admittance,

$$\mathbf{I}_u = \frac{Ee^{j\delta} - V_{th}}{j(X_v + X_n)}, \qquad X_n = X_{th} + X_c(1-k), \qquad k = -\frac{X_{se}}{X_c}, \tag{2}$$

where X_c is the present corridor reactance and k the compensation degree, positive when capacitive. CRS keeps the angle of the reference (Qoria et al. 2020; Rokrok et al. 2022):

$$\mathbf{I} = \mathbf{I}_u \text{ if } |\mathbf{I}_u| \le I_{\max}; \qquad \mathbf{I} = I_{\max}\mathbf{I}_u/|\mathbf{I}_u| \text{ otherwise.} \tag{3}$$

During the fault $V_{th} = V_g X_f/(X_f + X_s)$ and $X_{th} = X_s X_f/(X_s + X_f)$; otherwise $V_{th} = V_g$ and $X_{th} = X_s$.

In the phasor model the TCSC is a reactance $X_{se} = -kX_c$ that follows its reference through a first-order lag T_d, the usual level of detail for TCSC stability studies (Paserba et al. 1995), with $0 \le k \le k_{\max}$ and an inductive

insertion of up to $k_{ind}X_c$. The SSSC injects a voltage in quadrature with the current (Gyugyi et al. 1997), so $|X_{se}| \le V_{q,\max}/|\mathbf{I}|$. The base model has a reactive network, balanced faults and phasor dynamics, as is usual for first-swing studies (Kundur 1994) and for GFM transient analysis (Huang et al. 2019; Pan et al. 2020; Rokrok et al. 2022). Sections 6.4 to 8 relax each of these assumptions. Table 1 lists the parameters. The nominal $k_0 = 0.25$ corresponds to a TCSC slightly above its blocked-thyristor reactance.

Table 1 Base parameters (per unit on the inverter rating)

Quantity	Symbol	Value
Internal and grid voltage	E, V_g	1.0, 1.0
Virtual and filter reactance	X_v	0.15
Virtual inertia, damping	H, D	3 s, 20
Current limit	$I_{\max}$	1.2
One circuit; fault reactance	$X_{L1}; X_f$	0.6; 0.05
Nominal, maximum, continuous k	$k_0, k_{\max}, k_{cont}$	0.25, 0.70, 0.625
Maximum inductive insertion	k_{ind}	0.30
Device lag, detection delay	T_d, t_{det}	20 ms, 10 ms
Dip/recovery level; release time	$V_{dip}/V_{rec}; T_{rel}$	0.80/0.85; 3 s
SSSC voltage limit	$V_{q,\max}$	0.35

3 Power-angle analysis with current limiting

3.1 Closed-form relation and the current-limit ceiling

Because every branch is reactive, $\mathbf{I}_u$ and $\mathbf{I}$ point in the same direction and the power delivered to the Thevenin source equals the terminal power. Substituting (3) into $P = \mathrm{Re}(V_{th}\mathbf{I}^*)$ and using $\mathrm{Im}\left(Ee^{j\delta} - V_{th}\right) = E\sin\delta$ gives

$$P(\delta) = \frac{EV_{th}\sin\delta}{\max\{X_\Sigma, |Ee^{j\delta} - V_{th}|/I_{\max}\}}, \tag{4}$$

where $X_\Sigma = X_v + X_n$. The limiter acts as an angle-dependent reactance $\left|Ee^{j\delta} - V_{th}\right|/I_{\max}$ that replaces X_Σ whenever it is larger; this is the reactive counterpart of the equivalent circuit of Fan and Wang (2022). Equation (4) agreed with direct evaluation of (2) and (3) to machine precision. Letting $X_\Sigma \to 0$ gives the largest power at a given angle,

$$P_{lim}(\delta) = \frac{I_{\max}EV_{th}\sin\delta}{|Ee^{j\delta} - V_{th}|}, \tag{5}$$

which reduces to $I_{\max}\cos(\delta/2)$ for $E = V_{th} = 1$.

Proposition 1. For every $X_\Sigma > 0$ and $0 < \delta < \pi$, $P(\delta) \le P_{lim}(\delta)$, with equality when the limiter is active, because the maximum in the denominator of (4) is never smaller than $\left|Ee^{j\delta} - V_{th}\right|/I_{\max}$. No series reactance can lift the curve above a ceiling that depends only on E, V_{th} and $I_{\max}$.

Proposition 2. $P(\delta)$ is non-increasing in X_Σ, and on the saturated part of the curve $\partial P/\partial X_\Sigma = 0$. Series inductance can therefore only reduce the synchronizing power or leave it unchanged. In mild faults it keeps the inverter out of saturation only by lowering the unsaturated curve to the level the limiter would impose anyway.

Proposition 3. For the undamped first swing under any schedule of the series reactance, the fault-on and post-fault curves are bounded by the ceilings at $V_{th,f}$ and V_g. The CCT therefore cannot exceed the value the equal-area criterion gives for the ceilings. This value is called the series-FACTS bound below.

Fig. 2 shows these properties for SCR = 1.5 and $P_{ref} = 0.8$. After the N-1 outage at nominal compensation the post-fault curve never reaches P_{ref}, so no post-fault equilibrium exists. Raising k to 0.7 lifts the rising part of the curve until it meets the ceiling, beyond which both post-fault curves coincide with it. The derivation needs a reactive network and a limiter that holds $|\mathbf{I}| = I_{\max}$. An adaptive virtual impedance satisfies the second condition and a fixed-gain one does not, while line resistance breaks the first. Section 6.4 quantifies both departures.

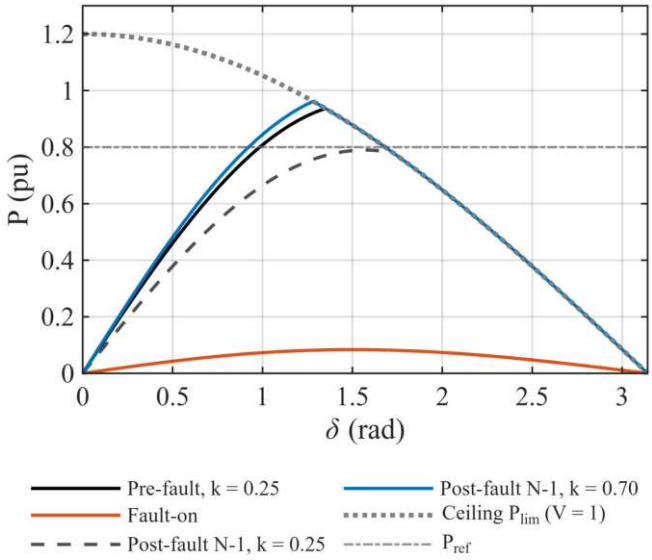


Fig. 2 Power-angle curves with CRS for SCR = 1.5 and $P_{ref} = 0.8$ pu, and the ceiling (5)

3.2 Post-fault equilibrium and minimum compensation

A stable post-fault equilibrium needs $P(\delta) = P_{ref}$ on the rising branch, whose maximum occurs at $\delta = \pi/2$ or at the saturation boundary δ_s, whichever comes first. From $\left|Ee^{j\delta} - V_g\right| = I_{\max}X_\Sigma$,

$$\cos\delta_s = \frac{E^2+V_g^2-I_{\max}^2X_\Sigma^2}{2EV_g}, \tag{6}$$

and the peak power on the stable branch is $P_{pk} = EV_g\sin\delta_s/X_\Sigma$ if $\cos\delta_s > 0$ and EV_g/X_Σ otherwise. Since P_{pk} decreases with X_Σ, the largest admissible post-fault reactance X_Σ^* solves $P_{pk}(X_\Sigma^*) = P_{ref}$, and the minimum compensation of the remaining corridor is

$$k_{\min} = 1 - \frac{X_\Sigma^* - X_v - X_s}{X_{c,post}}. \tag{7}$$

Equation (7) is necessary for survival but not sufficient, since the trajectory must also be caught during the first swing.

3.3 Extended equal-area criterion

For $D = 0$, (1) is the classical swing equation with the curves of (4), and the critical clearing angle follows from (Kundur 1994)

$$\int_{\delta_0}^{\delta_{cr}} \left[P_{ref} - P_f(\delta)\right] d\delta = \int_{\delta_{cr}}^{\delta_u} \left[P_{post}(\delta) - P_{ref}\right] d\delta, \tag{8}$$

where δ_u is the unstable equilibrium of P_{post}. The CCT is the time at which the fault-on trajectory reaches δ_{cr}, and it is zero if $P_{post} < P_{ref}$ everywhere. Replacing P_f and P_{post} by the ceilings gives the bound of Proposition 3.

4 Planning criterion and screening map

Equation (7) needs only the grid strength, the dispatch, the current limit and the corridor data. For the base N-1 case (SCR = 1.5, $P_{ref} = 0.8$) it gives $k_{\min} = 0.278$, slightly above $k_0 = 0.25$, so a device that cannot reach 0.278 cannot save the plant whatever its control. The phasor model gives a second estimate: the smallest constant compensation with which the plant survives an N-1 outage cleared after 1 ms. In the weakest grid the two agree within 0.011 (0.278 against 0.279 at $P_{ref} = 0.8$, and 0.524 against 0.534 at 0.9). In stronger grids the simulated value is higher by up to 0.094 (SCR = 2.5, $P_{ref} = 0.95$: 0.220 against 0.313). The difference is the margin needed to catch the swing caused by the trip, which a static condition cannot see. Equation (7) is thus a lower bound that is tight close to the loss of equilibrium, which is where a planner needs it.

Fig. 3 applies (7) over SCR from 1.2 to 10 and dispatch from 0.4 to 1.0 pu (14 520 points). Each point falls into one of four regions:

(a) no pre-fault equilibrium (3% of the points);

(b) the equilibrium survives the outage, so inverter-side measures are enough (90%);

(c) the outage removes the equilibrium and $k_{\min} \le k_{\max}$, so series compensation is needed and its size can be read from the contours (7%);

(d) $k_{\min} > k_{\max}$, so a run-back is needed (no points for $k_{\max} = 0.7$).

Region (c) lies where a weak grid and a high dispatch coincide. The dashed line shows that oversizing the inverter to 1.5 pu recovers only a thin strip of it. The map takes a fraction of a second per point to compute. Used as a screening step, it shows the planner which outages need a time-domain study and which device rating to study.

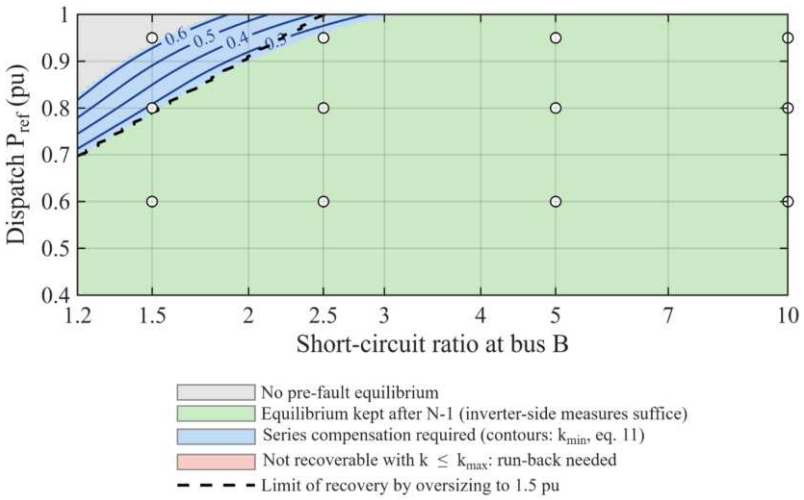


Fig. 3 Screening map for the N-1 outage with contours of $k_{\min}$ from (7). Circles mark the single-machine cases of Sect. 6

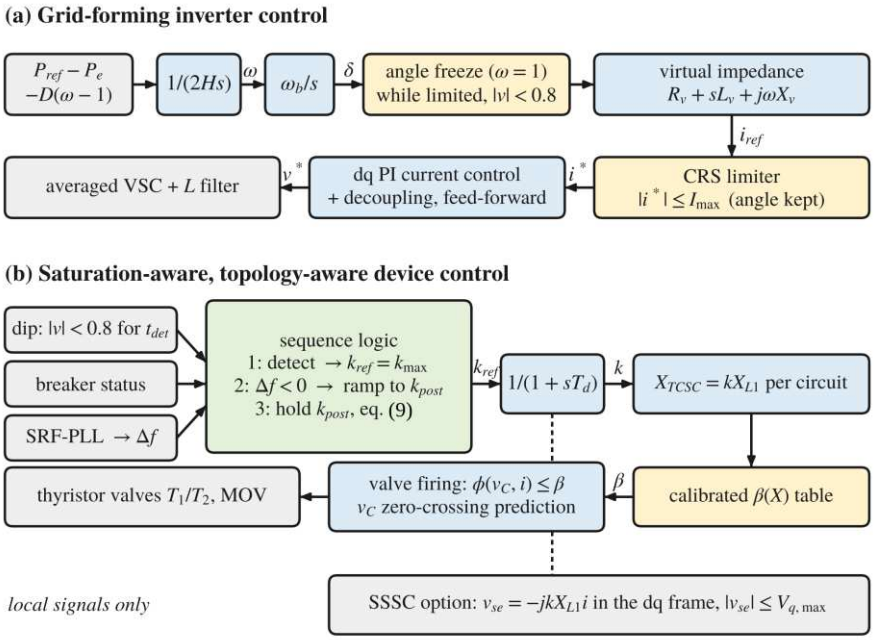
5 Coordinated control

The device controller (Fig. 4b) uses only its terminal voltage and the status of the corridor breakers. A disturbance is declared when the voltage stays below 0.8 pu for $t_{det} = 10$ ms or a breaker opens, and recovery when the voltage stays above 0.85 pu for t_{det}. From detection until the first-swing peak the reference is $k_{\max}$. By Proposition 2 a capacitive reactance costs nothing while the inverter is limited, so the boost is already in place when the limiter releases. The peak is detected as the first zero crossing of the frequency deviation measured by a synchronous-reference-frame phase-locked loop (PLL) with a 20 ms filter. The reference then ramps over $T_{rel} = 3$ s to

$$k_{post} = \min\left\{k_{\max},\ \max\left[k_0,\ 1 - \frac{X_{c,pre}(1-k_0)}{X_{c,post}}\right]\right\}, \tag{9}$$

which keeps the net corridor reactance at its pre-fault value. For the loss of one of two circuits $k_{post} = 0.625$, which is taken as the continuous rating.

On the inverter side, while the current reference is saturated and the PCC voltage is below 0.8 pu, the VSM frequency is held at nominal so the angle stops advancing. This is a simple form of the freezing and mode-switching schemes of Rokrok et al. (2022), Kkuni and Yang (2024) and Arjomandi-Nezhad et al. (2025). It is used here as a representative inverter-side measure and is not claimed as a contribution. The two parts complement each other. The freeze removes the acceleration that the current limit causes during the fault, which no network device can do (Proposition 1). The series device restores the post-fault equilibrium after an outage, which no inverter-side measure can do without reducing the dispatch.



193

194 **Fig. 4** Control structure. (a) GFM inverter with VSM, angle freeze, virtual impedance, CRS and dq current
195 control. (b) Series-device control with the valve firing of the switched TCSC

196 Nine strategies are compared: *fixed* ($k = k_0$); *inductive* ($-0.3X_c$ from detection to recovery); *post-clearing*
197 ($k_{\max}$ after recovery only); *inductive + capacitive*; *boost* (the device control above); *freeze* (the inverter control
198 above with $k = k_0$); *freeze + boost* (the coordinated scheme); and two inverter-side alternatives without a
199 device, *oversizing* ($I_{\max} = 1.5$ pu) and a *voltage-dependent* P_{ref} scaled by $\min(1, V_{PCC}/0.9)$.

200 # 6 Single-machine results

201 CCTs were found by bisection with 1 ms resolution. A case counts as stable when the frequency returns within
202 10^{-4} pu of nominal with the limiter inactive. In the tables, "Inf" means the plant rode through a 1 s fault and 0
203 means a loss of synchronism for the shortest fault tested (0.5 ms), which happens when no post-fault equilibrium
204 exists.

205 ## 6.1 Accuracy of the analysis

206 Table 2 compares the CCT from (8) with the undamped first swing in twelve cases. The two agree within 1 ms.
207 With the boost, the equal-area CCT matches the series-FACTS bound within 1 ms and the simulation within 2
208 ms, so a boost to 0.7 already obtains almost all that series compensation can offer in the first swing. In the
209 strongest cases the bound is reached even with fixed compensation. The largest gain is in the N-1 case with SCR
210 = 2.5 and $P_{ref} = 0.8$ (from 64 to 100 ms, against a bound of 101 ms).

211 **Table 2** CCT (ms) from the equal-area criterion (EAC), the undamped simulation (Sim.) and the series-FACTS
212 bound

Corridor	SCR	P_{ref}	Fixed, EAC	Fixed, Sim.	Boost, EAC	Boost, Sim.	Bound
Intact	2.5	0.6	197	196	197	196	197
Intact	2.5	0.8	99	98	101	100	101

Corridor	SCR	P_{ref}	Fixed, EAC	Fixed, Sim.	Boost, EAC	Boost, Sim.	Bound
Intact	5	0.6	228	227	228	227	228
Intact	5	0.8	123	123	123	123	123
Intact	10	0.6	287	286	287	286	287
Intact	10	0.8	151	150	151	150	151
N-1	2.5	0.6	190	189	197	196	197
N-1	2.5	0.8	64	64	100	99	101
N-1	5	0.6	228	227	228	227	228
N-1	5	0.8	110	109	123	123	123
N-1	10	0.6	287	286	287	286	287
N-1	10	0.8	146	146	151	150	151

6.2 Critical clearing times with damping

Table 3 lists the CCTs of the damped system. Five observations follow from it.

Inductive insertion never raised the CCT and lowered it in 13 of the 22 cases, by up to 17 ms, and following it with a capacitive boost was never better than the boost alone. This is Proposition 2 at work in the damped system.

The boost was the best device-only strategy in every case, and its gain was concentrated in the N-1 cases with a weak grid and a high dispatch. It turned a CCT of zero into 103 ms at SCR = 1.5, $P_{ref} = 0.8$ and into 62 ms at SCR = 2.5, $P_{ref} = 0.95$. It changed nothing at SCR ≥ 5 with $P_{ref} = 0.6$, where the ceiling limits the CCT.

The freeze rode through 1 s faults in every case that keeps a post-fault equilibrium and failed at once in the two N-1 cases without one. The first of these lies in region (c) of the map. The second lies just inside region (b) because of the trip swing noted in Sect. 4, so a band next to region (c) should be treated as uncertain.

The coordinated scheme rode through 1 s faults in all 22 cases.

Oversizing raised the CCT wherever an equilibrium existed, because the ceiling scales with $I_{\max}$, but did not help in the base N-1 case. The voltage-dependent reference kept the base N-1 case in synchronism only by settling at 0.789 pu.

Table 3 CCT (ms) with damping, given as N-1 outage / intact corridor (Inf: survives a 1 s fault; 0: no post-fault equilibrium)

SCR / P_{ref}	Fixed	Inductive	Post-clearing	Ind. + cap.	Boost	Freeze	Freeze + boost	Overs.	V-dep.
1.5 / 0.6	252 / 259	245 / 258	257 / 259	252 / 258	259 / 259	Inf / Inf	Inf / Inf	284 / 313	922 / Inf
1.5 / 0.8	0 / 100	0 / 96	96 / 103	90 / 99	103 / 105	0 / Inf	Inf / Inf	0 / 151	231* / 675
2.5 / 0.6	302 / 302	298 / 302	302 / 302	299 / 302	302 / 302	Inf / Inf	Inf / Inf	367 / 367	Inf / Inf
2.5 / 0.8	141 / 150	131 / 148	147 / 150	140 / 148	150 / 150	Inf / Inf	Inf / Inf	202 / 212	919 / 748
2.5 / 0.95	0 / 62	0 / 56	55 / 62	48 / 58	62 / 63	0 / Inf	Inf / Inf	90 / 129	642 / 466
5 / 0.6	368 / 368	368 / 368	368 / 368	368 / 368	368 / 368	Inf / Inf	Inf / Inf	467 / 467	Inf / Inf
5 / 0.8	189 / 189	180 / 189	189 / 189	183 / 189	189 / 189	Inf / Inf	Inf / Inf	268 / 268	Inf / 910
5 / 0.95	80 / 97	67 / 94	93 / 97	84 / 95	97 / 97	Inf / Inf	Inf / Inf	171 / 176	688 / 396
10 / 0.6	524 / 524	524 / 524	524 / 524	524 / 524	524 / 524	Inf / Inf	Inf / Inf	837 / 837	Inf / Inf
10 / 0.8	243 / 243	238 / 243	243 / 243	239 / 243	243 / 243	Inf / Inf	Inf / Inf	376 / 376	Inf / Inf
10 / 0.95	121 / 127	104 / 126	124 / 127	115 / 126	127 / 127	Inf / Inf	Inf / Inf	237 / 237	Inf / 406

Overs.: oversizing; V-dep.: voltage-dependent P_{ref}. *Settles at $P = 0.789$ pu and $V_{PCC} = 0.888$ pu (sustained run-back). SCR = 1.5 with $P_{ref} = 0.95$ has no pre-fault equilibrium.

Fig. 5 shows the case SCR = 2.5, $P_{ref} = 0.95$ with a 50 ms fault. With fixed or inductive compensation the angle runs away. The freeze stops the runaway, but the post-fault curve lies below P_{ref}, so the inverter stays current-limited at about 0.88 pu. The boost alone survives with a visible swing. The coordinated scheme keeps the angle almost constant, leaves the current limit shortly after clearing and settles at $k_{post} = 0.625$.

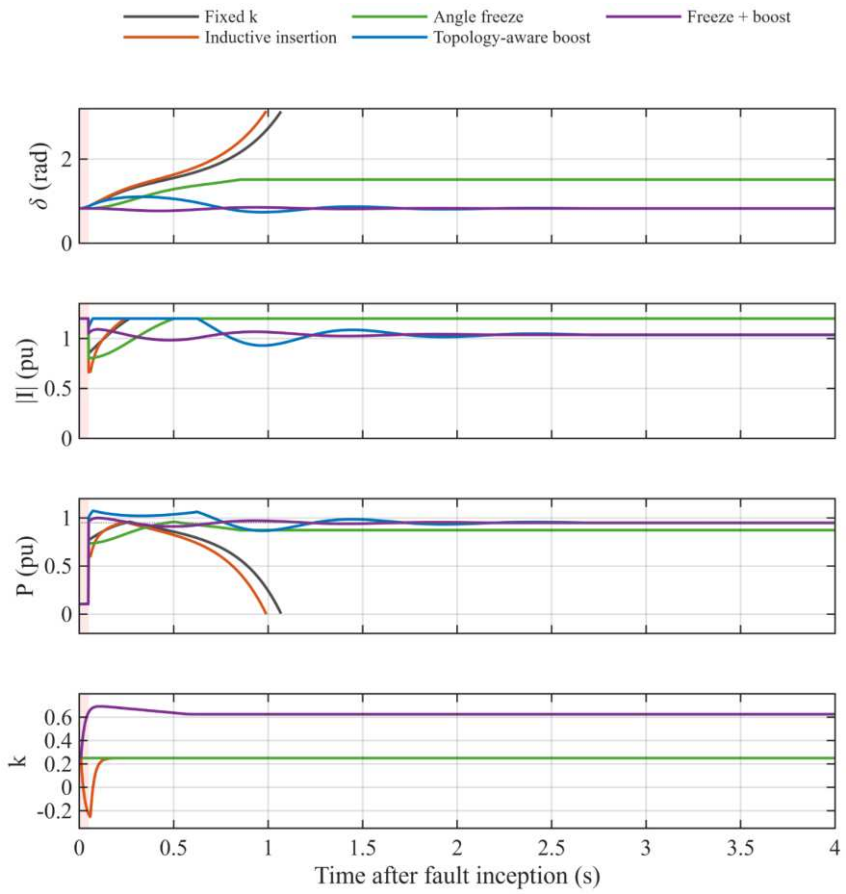


Fig. 5 Phasor-model trajectories for SCR = 2.5, $P_{ref} = 0.95$ pu, a 50 ms fault and the N-1 outage (shaded: fault)

6.3 Device rating and sensitivity

In the base N-1 case the boost gives a CCT of zero for $k_{\max} < k_{\min} = 0.278$, 53 ms at $k_{\max} = 0.30$ and 105 ms at 0.80, while the coordinated scheme rides through 1 s faults for every $k_{\max} \geq 0.30$. The rating that matters for the coordinated scheme is therefore $k_{\min}$ from (7), which is smaller than the rating the boost needs on its own. A slower device ($T_d = 200$ ms) or a 100 ms detection delay reduces the boost CCT from 103 ms to 91 and 98 ms respectively, but does not affect the coordinated scheme. An SSSC with $V_{q,\max} = 0.15$ pu cannot reach $k_{\min}$ at the post-fault current and fails with every strategy. With 0.20 to 0.35 pu its boost CCT (54 to 94 ms) stays below that of the TCSC, because its reactance falls as the current rises. The full sensitivity table is in Online Resource 1 (Table S1).

6.4 Effect of the modeling assumptions

The study was repeated for six cases under twelve model variants: line resistance (R/X from 0.1 to 0.3), reactive-power droop, an automatic voltage regulator, adaptive and fixed-gain virtual-impedance limiting, faults at 10%

and 50% of circuit 2, and unbalanced faults. Line resistance changes the picture most. It adds a power component that bypasses the reactive path of the limiter, so the ceiling no longer binds and the fixed-compensation CCT rises (base N-1 case: from 0 to 202 ms at R/X = 0.3). The boost then helps only where the outage threatens the equilibrium, and elsewhere it costs CCT, by up to 39 ms at R/X = 0.3 (SCR = 5, $P_{ref} = 0.95$, N-1). It should therefore be armed only for outages that the map places in or next to region (c). The other conclusions held in every variant: inductive insertion never beat fixed compensation, the freeze rode through whenever an equilibrium existed, and the coordinated scheme rode through 1 s faults in all 78 combinations of variant and case.

7 EMT and hardware-in-the-loop validation

7.1 Model

An instantaneous-value model was built in Simulink with four MATLAB Function blocks (network, GFM control, device control and monitor) that exchange signals through unit delays at a fixed step of 20 µs (structure in Online Resource 1, Sect. S3). The three-phase network, integrated by a fourth-order Runge-Kutta method, contains the converter L filter (0.10 pu), a shunt capacitor at the PCC (0.10 pu), the two corridor circuits with R/X = 0.05, a shunt capacitor at bus B and the Thevenin grid. The inverter uses the control of Sect. 5 with a dq PI current controller (300 Hz bandwidth) and is represented by its averaged voltage. The multi-kilohertz PWM harmonics of the converter are attenuated by the L filter and the PCC capacitor and lie far above both the fundamental-frequency synchronization swing and the 3 to 35 Hz subsynchronous range associated with the TCSC, so they do not interact with the phenomena studied here.

Each circuit carries a switched TCSC: a 0.135 pu capacitor in parallel with a 0.020 pu thyristor-controlled reactor (resonance ratio 2.6), two antiparallel valves that conduct only when gated and forward-biased and turn off at current zero, and a metal-oxide varistor at 1.0 pu. The firing unit estimates the angle to the next zero crossing of the capacitor voltage,

$$\phi = \operatorname{atan2}(|v_C|,\ -\operatorname{sgn}(v_C i_L) X_C |i_L|), \tag{10}$$

and fires the discharging valve when ϕ falls to the commanded angle β. The firing is thus synchronized to the capacitor voltage itself, as in commercial TCSCs, and needs no PLL. A first version that synchronized the firing to the line current through a PLL locked into an inductive vernier mode after the trip of circuit 2 and lost synchronism even for a 5 ms fault. This is reported because line-current synchronization is the usual textbook description of TCSC firing. The reactance-angle relation of the switched model was measured on the model itself at sixteen firing angles and used as a monotonic firing table, with which the steady-state reactance tracked its reference within 0.2% for k from 0.25 to 0.70. An SSSC-type device that injects $-jkX_{L1}\mathbf{i}$, limited to 0.6 pu, serves as a second device. Fig. 6 shows the boost: k rises from 0.25 to 0.7 within about three cycles, and the capacitor voltage stays well below the varistor level.

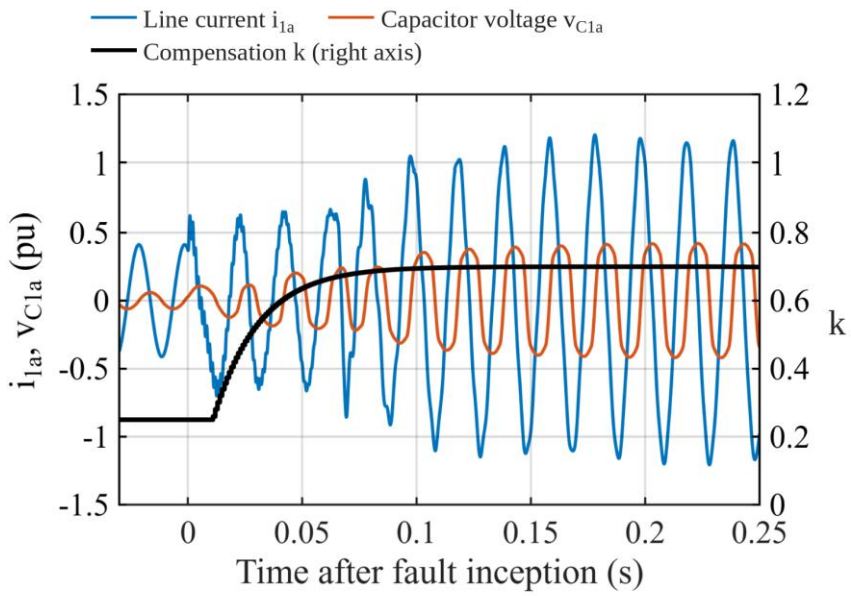


Fig. 6 Switched TCSC in Simulink during the boost (N-1, 60 ms fault): line current, capacitor voltage and compensation degree

7.2 Critical clearing times

Table 4 compares the EMT CCTs with those of the phasor model at the same R/X (2 ms bisection). The differences are systematic. In the weak N-1 cases the EMT model gives longer CCTs (98 against 68 ms for fixed compensation at SCR = 1.5), because the shunt capacitance supports the voltage after clearing. In stronger cases it gives shorter ones (120 against 154 ms at SCR = 2.5 with the corridor intact), because the current controller and the measurement delays let the current overshoot the limit briefly. The TCSC and the SSSC-type device agreed within one bisection step in 26 of 30 comparisons. The qualitative findings carry over. Inductive insertion was never better than fixed compensation, and the freeze and the coordinated scheme rode through 1 s faults in all cases with both devices. The boost raised the CCT where the outage threatens the equilibrium (from 98 to 120 ms and from 49 to 65 ms) but lowered it in the two N-1 cases with ample margin (from 123 to 120 ms and from 94 to 79 ms), in line with the resistive phasor variants.

Table 4 CCT (ms) of the EMT model with TCSC / SSSC-type device / phasor model (R/X = 0.05). Freeze + boost: Inf in all cases

Case	Fixed	Inductive	Boost	Freeze
N-1, 1.5/0.8	98/98/68	98/98/60	120/120/116	Inf/Inf/Inf
N-1, 2.5/0.8	123/123/154	120/120/143	120/120/155	Inf/Inf/Inf
N-1, 2.5/0.95	49/55/0	43/43/0	65/65/67	Inf/Inf/0
N-1, 5/0.95	94/98/88	79/79/74	79/79/96	Inf/Inf/Inf
Intact, 1.5/0.8	120/120/111	114/120/107	120/114/112	Inf/Inf/Inf
Intact, 2.5/0.8	120/120/154	120/120/152	120/120/151	Inf/Inf/Inf

7.3 Series resonance

A capacitor on the remaining circuit forms a series-resonant circuit with the corridor and grid inductance. Linearizing a dq model of the same structure around the N-1 operating point (Fig. 7) places the mode at 61 to 82

Hz in the dq frame for k from 0.1 to 0.8, that is, at 11 to 32 Hz in the stationary frame. With a lossless network its damping is small and falls to zero at $k \approx 0.72$ (SCR = 2.5) and $k \approx 0.60$ (SCR = 5). With R/X = 0.05 it stays at or above 1.27%, and the SSSC-type device gives at least 4.0%. In the EMT model with the remaining circuit at $k = 0.625$ and R/X = 0.01, a fixed capacitor of the same reactance produced a 28 to 29 Hz component of 14.4% of the fundamental current, which is the predicted resonance. The vernier-controlled TCSC showed no component at that frequency; its largest subsynchronous component was 6.0%, at 9 Hz. Vernier operation thus removes the resonance (Hingorani and Gyugyi 2000), so the setpoint of 0.625 should be realized by thyristor control rather than by a switched capacitor bank. Subsynchronous control interaction with the inverter controls should still be checked with the manufacturer's model for a given project (Cheng et al. 2023).

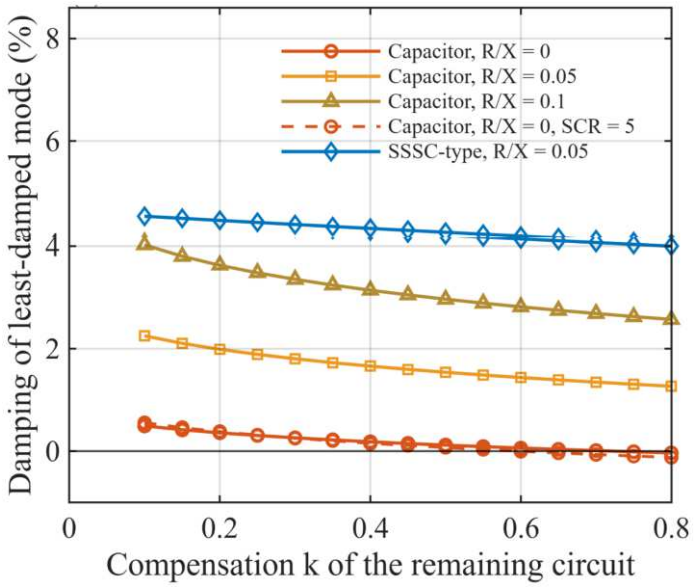


Fig. 7 Damping of the least-damped series-resonance mode of the dq model against the compensation of the remaining circuit

7.4 Controller-hardware-in-the-loop tests

The inverter and device controllers were also tested on hardware with three LAUNCHXL-F28379D boards (TI C2000, 200 MHz). Board A emulates the plant: the per-phase network of Sect. 7.1 with both switched TCSCs, discretized exactly with a zero-order hold at a step of 50 µs, breakers and fault arcs that open at a current zero, varistors at 1.0 pu, and the firing unit of circuit 2. Board B runs the GFM control of Sect. 5 every 100 µs and drives three 10 kHz PWM outputs. Board A measures their duty cycles with its capture units and applies them as the averaged inverter voltage. Board C runs the device controller and the capacitor-voltage-synchronized firing of circuit 1 every 50 µs and drives six gate lines, which board A reads as digital inputs. Board A sends its measurements to B and C over SPI links in frames protected by a check word. The longest plant step was 44.6 µs, so the bench ran in real time without a missed step. Board B used about 8 µs of its 100 µs period, and board C at most 11.6 µs of its 50 µs period.

The same source code was compiled for the boards and, as a desktop reference, for a PC, where it follows the frame schedule and link delays of the bench. The real-time plant differs from the Simulink model in step size, integration method and controller delays, so its CCTs are compared with this reference rather than with Table 4.

The firing table, measured on the plant model, held the steady-state compensation within 1.9% of its reference for k from 0.25 to 0.70.

The hardware CCTs of five strategies in the six cases of Table 4 were found by the bisection of Sect. 7.2 and then measured again in a second, identical sweep (417 runs in total). The angle freeze and the coordinated scheme rode through 1 s faults in all six cases in both sweeps, as in the reference. Of the 36 finite CCTs, 24 equalled the reference and 30 were within one bisection step. The largest deviation, 16 ms, was for inductive insertion in the N-1 case with SCR = 5 in the first sweep, and no hardware CCT exceeded the reference. The two sweeps gave the same value in 9 of 18 cells and values within 2 ms of each other in 13. The qualitative findings carry over. Inductive insertion never raised the CCT by more than one bisection step. The boost raised it in the N-1 cases where the outage threatens the equilibrium (from 120 to 138 ms at SCR = 1.5, and from 58 to 78 ms at SCR = 2.5 with $P_{ref} = 0.95$), and elsewhere changed it by between +4 and −8 ms.

Fig. 8 compares the hardware with the reference for a 250 ms fault, longer than the 168 ms CCT of fixed compensation. With fixed compensation the inverter loses synchronism. With the freeze and the boost its angle stays within 0.04 rad of the pre-fault value, and the traces of the bench and the reference overlap. The capacitor voltage never exceeded 0.48 pu, so the varistors did not conduct.

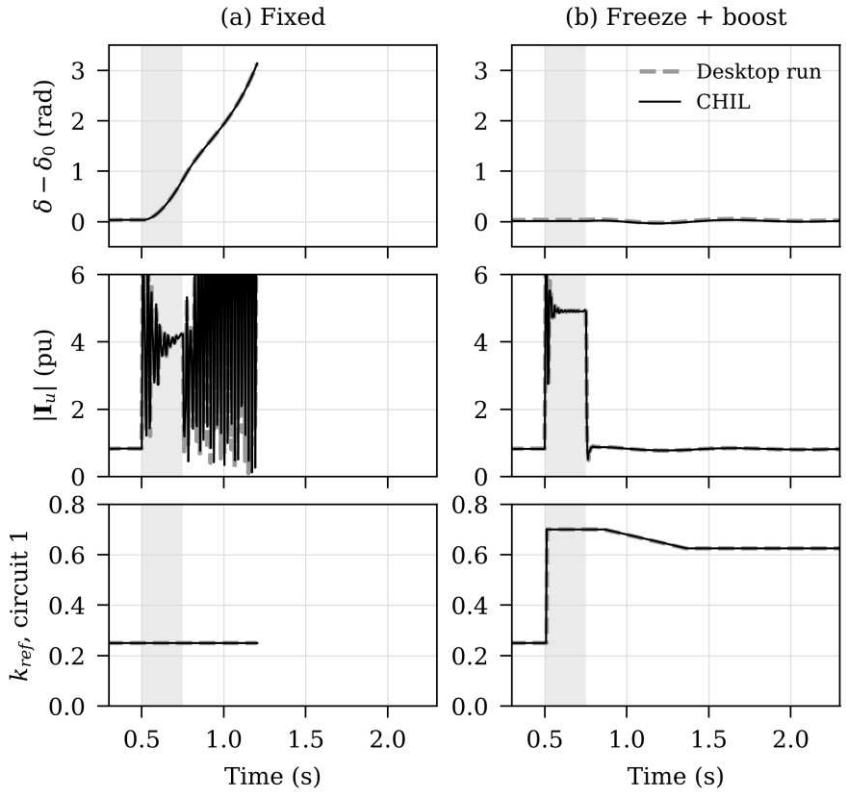


Fig. 8 CHIL (solid) and desktop run of the same code (dashed) for the N-1 case with SCR = 2.5, $P_{ref} = 0.8$ pu and a 250 ms fault (shaded): angle deviation, magnitude of the unsaturated current reference, and compensation reference of circuit 1. (a) Fixed compensation. (b) Freeze and boost

No frame was lost on the A-C link. On the A-B link, which carries 10 000 frames per second, a median of 15 frames per run failed the check word, with a maximum of 147. Board B discards such a frame and uses the frame

counter to advance its virtual-rotor angle by the missed periods, so a lost frame does not shift the angle. Online Resource 1 (Sect. S6) describes the bench and gives its timing, link statistics and full results.

8 Multi-machine study

The New England 39-bus system was modified with network and dispatch data from MATPOWER (Zimmerman et al. 2011) and machine data from Athay et al. (1979). The generators at buses 38 and 30 are replaced by GFM plants of 1000 and 300 MVA. The bus-38 plant connects to bus 29 through a new bus 40 and a double-circuit corridor with a TCSC ($k_0 = 0.25$, R/X = 0.05) on each circuit. The other eight machines use a flux-decay model with a static exciter (gain 50, 0.05 s) and a TGOV1 governor (5% droop), and loads are constant impedances. A solid fault at the bus-29 end of circuit 2 is cleared by tripping the circuit. The dispatch (830 and 950 MW) and the circuit reactance (0.5, 0.8 and 1.2 pu) set the stress. The network is solved algebraically at each 1 ms step, with an exact solution of the CRS condition on the Thevenin equivalent seen by each plant.

Table 5 CCT (ms) in the modified IEEE 39-bus system (Inf: survives a 1 s fault)

MW, X_{L1}	Fixed	Ind.	Boost	Overs.	V-dep.	Freeze	F+B
830, 0.5	182	175	186	241	512	885	Inf
830, 0.8	138	128	181	149	227	670	984
830, 1.2	0	0	167	0	0	0	Inf
950, 0.5	97	91	116	157	307	481	Inf
950, 0.8	0	0	104	0	0	0	Inf
950, 1.2	0	0	83	0	0	0	Inf

Table 5 confirms the single-machine findings. Inductive insertion lowered every non-zero CCT (for example from 138 to 128 ms). In the three most stressed cases the trip removes the post-fault equilibrium. Fixed compensation, inductive insertion, oversizing, the voltage-dependent reference and the freeze all failed there even for a 1 ms fault. Only the strategies that raise the compensation of the remaining circuit survived: the boost with 167, 104 and 83 ms, and the coordinated scheme with 1 s faults. Where the equilibrium survives, the inverter-side measures carry most of the benefit (freeze 481 to 885 ms), and the coordinated scheme rode through 1 s faults in two of the three cases (984 ms in the third). Online Resource 1 (Sect. S5) gives the trajectories.

9 Discussion

For a synchronous generator a capacitive boost is a reliable first-swing aid, because the internal voltage stays behind a fixed reactance. A current-limited GFM inverter behaves differently. While it is limited, its power is set by the current limit and the retained voltage, and the corridor reactance does not matter (Propositions 1 and 2). The device acts only through the unlimited part of the trajectory and, above all, through the post-fault equilibrium. This explains why inductive insertion never helps, why the boost brings the first-swing CCT close to a bound that strong grids reach without it, and why the device is most useful after outages that would otherwise remove the equilibrium.

The criterion (7) and the map turn these findings into a planning procedure. If $k_{\min} \leq k_0$ (region (b)), inverter-side measures such as the freeze are enough, and the boost should stay unarmed on resistive corridors. If $k_0 <$

$k_{\min} \le k_{\max}$ (region (c)), the coordinated scheme is the appropriate remedy, and the device rating must cover $k_{\min}$ plus a margin for the trip swing (up to 0.094 here). If $k_{\min} > k_{\max}$ (region (d)), a run-back or a larger device is needed. The setpoint (9) keeps the post-outage power flow unchanged. Inverter-side methods (Rokrok et al. 2022; Fan and Wang 2022, 2023; Kkuni and Yang 2024; Arjomandi-Nezhad et al. 2025) are enough wherever the equilibrium exists, which covers about 90% of the map, but they cannot help where it is lost. The series device covers those cases with equipment the transmission owner may already operate.

The study has limits. The EMT model and the CHIL plant use an averaged converter, and the firing table is calibrated in steady state. The CHIL tests run the controllers on microcontrollers against a plant emulated on a third microcontroller at a 50 µs step; no power-hardware or field tests were performed. The multi-machine study uses phasor models without power system stabilizers. Subsynchronous control interaction was examined only for the electrical resonance mode, and post-fault voltage recovery, protection coordination and the thermal duty of the TCSC during long boosts were not studied in detail.

10 Conclusions

When a GFM inverter is current-limited, its power is bounded by a ceiling that does not depend on the series reactance. Series inductance therefore never increases the synchronizing power, and no reactance schedule can raise the first-swing CCT above an equal-area bound on the ceiling; a capacitive boost to 0.7 came within 2 ms of that bound. The main value of a series device lies in restoring the post-fault equilibrium after an outage. The closed-form minimum compensation (7) and its screening map tell the planner which outages need the device, how large it must be, and when a run-back is needed instead.

The coordinated freeze-and-boost scheme rode through 1 s faults in all 22 single-machine cases and in all 78 model-variant combinations. A Simulink model with a switched TCSC fired from the capacitor voltage confirmed the findings and showed that firing synchronized to the line current can lock into an inductive mode after an outage. The modified IEEE 39-bus system confirmed them in a multi-machine setting. In CHIL tests with the inverter and TCSC controllers on separate microcontrollers, the CCTs matched a desktop run of the same code within one bisection step in 30 of 36 comparisons, and the coordinated scheme rode through in every case. Because the boost can reduce the CCT on resistive corridors where the outage does not threaten the equilibrium, it should be armed only for the outages that the map places in or next to the region that needs series compensation.

Statements and Declarations

Funding The author did not receive support from any organization for the submitted work.

Competing interests The author has no relevant financial or non-financial interests to disclose.

Author contributions Muzeeb Khan Patan carried out the conceptualization, analysis, modeling, simulation, hardware tests and writing of this paper.

Data availability The MATLAB and Simulink models are available from the author on reasonable request.

Ethics approval Not applicable.

References

Arjomandi-Nezhad A, Guo Y, Pal BC, Yang G (2025) Modeling fault recovery and transient stability of grid-forming converters equipped with current reference limitation. IEEE Trans Energy Convers 40(2):1140–1152. https://doi.org/10.1109/TEC.2024.3507544

Athay T, Podmore R, Virmani S (1979) A practical method for the direct analysis of transient stability. IEEE Trans Power Appar Syst PAS-98(2):573–584. https://doi.org/10.1109/TPAS.1979.319407

Cheng Y, Fan L, Rose J, Huang S-H, Schmall J, Wang X, Xie X, et al (2023) Real-world subsynchronous oscillation events in power grids with high penetrations of inverter-based resources. IEEE Trans Power Syst 38(1):316–330. https://doi.org/10.1109/TPWRS.2022.3161418

D'Arco S, Suul JA (2014) Equivalence of virtual synchronous machines and frequency-droops for converter-based microgrids. IEEE Trans Smart Grid 5(1):394–395. https://doi.org/10.1109/TSG.2013.2288000

Fan B, Wang X (2022) Equivalent circuit model of grid-forming converters with circular current limiter for transient stability analysis. IEEE Trans Power Syst 37(4):3141–3144. https://doi.org/10.1109/TPWRS.2022.3173160

Fan B, Wang X (2023) Fault recovery analysis of grid-forming inverters with priority-based current limiters. IEEE Trans Power Syst 38(6):5102–5112. https://doi.org/10.1109/TPWRS.2022.3221209

Fan B, Liu T, Zhao F, Wu H, Wang X (2022) A review of current-limiting control of grid-forming inverters under symmetrical disturbances. IEEE Open J Power Electron 3:955–969. https://doi.org/10.1109/OJPEL.2022.3227507

Fu X, et al (2021) Large-signal stability of grid-forming and grid-following controls in voltage source converter: a comparative study. IEEE Trans Power Electron 36(7):7832–7840. https://doi.org/10.1109/TPEL.2020.3047480

Gu Y, Green TC (2023) Power system stability with a high penetration of inverter-based resources. Proc IEEE 111(7):832–853. https://doi.org/10.1109/JPROC.2022.3179826

Gyugyi L, Schauder CD, Sen KK (1997) Static synchronous series compensator: a solid-state approach to the series compensation of transmission lines. IEEE Trans Power Deliv 12(1):406–417. https://doi.org/10.1109/61.568265

Hatziargyriou N, Milanovic J, Rahmann C, Ajjarapu V, Canizares C, Erlich I, et al (2021) Definition and classification of power system stability: revisited and extended. IEEE Trans Power Syst 36(4):3271–3281. https://doi.org/10.1109/TPWRS.2020.3041774

Hingorani NG, Gyugyi L (2000) Understanding FACTS: concepts and technology of flexible AC transmission systems. IEEE Press, New York

Hossain F, Chaudhuri NR (2025) A dynamic phasor framework for analysis of grid-forming converter connected to series-compensated line. In: Proc IEEE PES General Meeting, pp 1–5. https://doi.org/10.1109/PESGM52009.2025.11225603

Huang L, Xin H, Wang Z, Zhang L, Wu K, Hu J (2019) Transient stability analysis and control design of droop-controlled voltage source converters considering current limitation. IEEE Trans Smart Grid 10(1):578–591. https://doi.org/10.1109/TSG.2017.2749259

Islam SU, Kim S (2024) Comparative analysis of sub-synchronous oscillations with various grid-forming control schemes under series-compensated line. IEEE Access 12:132763–132772. https://doi.org/10.1109/ACCESS.2024.3444889

Islam SU, Kim S (2026) Design and implementation of coordinated adaptive virtual oscillator control strategy for grid-forming converters to mitigate subsynchronous oscillations. Electronics 15(4):809. https://doi.org/10.3390/electronics15040809

Kkuni KV, Yang G (2024) Effects of current limit for grid forming converters on transient stability: analysis and solution. Int J Electr Power Energy Syst 158:109919. https://doi.org/10.1016/j.ijepes.2024.109919

Kundur P (1994) Power system stability and control. McGraw-Hill, New York

Lasseter RH, Chen Z, Pattabiraman D (2020) Grid-forming inverters: a critical asset for the power grid. IEEE J Emerg Sel Top Power Electron 8(2):925–935. https://doi.org/10.1109/JESTPE.2019.2959271

Matevosyan J, et al (2019) Grid-forming inverters: are they the key for high renewable penetration? IEEE Power Energy Mag 17(6):89–98. https://doi.org/10.1109/MPE.2019.2933072

Mathur RM, Varma RK (2002) Thyristor-based FACTS controllers for electrical transmission systems. Wiley-IEEE Press, New York. https://doi.org/10.1109/9780470546680

Milano F, Dörfler F, Hug G, Hill DJ, Verbič G (2018) Foundations and challenges of low-inertia systems. In: Proc Power Systems Computation Conference (PSCC), Dublin, pp 1–25. https://doi.org/10.23919/PSCC.2018.8450880

Pan D, Wang X, Liu F, Shi R (2020) Transient stability of voltage-source converters with grid-forming control: a design-oriented study. IEEE J Emerg Sel Top Power Electron 8(2):1019–1033. https://doi.org/10.1109/JESTPE.2019.2946310

Paquette AD, Divan DM (2015) Virtual impedance current limiting for inverters in microgrids with synchronous generators. IEEE Trans Ind Appl 51(2):1630–1638. https://doi.org/10.1109/TIA.2014.2345877

Paserba JJ, Miller NW, Larsen EV, Piwko RJ (1995) A thyristor controlled series compensation model for power system stability analysis. IEEE Trans Power Deliv 10(3):1471–1478. https://doi.org/10.1109/61.400931

Qoria T, Gruson F, Colas F, Kestelyn X, Guillaud X (2020) Current limiting algorithms and transient stability analysis of grid-forming VSCs. Electr Power Syst Res 189:106726. https://doi.org/10.1016/j.epsr.2020.106726

Rokrok E, Qoria T, Bruyere A, Francois B, Guillaud X (2022) Transient stability assessment and enhancement of grid-forming converters embedding current reference saturation as current limiting strategy. IEEE Trans Power Syst 37(2):1519–1531. https://doi.org/10.1109/TPWRS.2021.3107959

Rosso R, Wang X, Liserre M, Lu X, Engelken S (2021) Grid-forming converters: control approaches, grid-synchronization, and future trends. A review. IEEE Open J Ind Appl 2:93–109. https://doi.org/10.1109/OJIA.2021.3074028

Taul MG, Wang X, Davari P, Blaabjerg F (2020) Current limiting control with enhanced dynamics of grid-forming converters during fault conditions. IEEE J Emerg Sel Top Power Electron 8(2):1062–1073. https://doi.org/10.1109/JESTPE.2019.2931477

Wu H, Wang X (2019) Design-oriented transient stability analysis of grid-connected converters with power synchronization control. IEEE Trans Ind Electron 66(8):6473–6482. https://doi.org/10.1109/TIE.2018.2875669

Xiong X, Wu C, Hu B, Pan D, Blaabjerg F (2021) Transient damping method for improving the synchronization stability of virtual synchronous generators. IEEE Trans Power Electron 36(7):7820–7831. https://doi.org/10.1109/TPEL.2020.3046462

Zhang L, Harnefors L, Nee H-P (2010) Power-synchronization control of grid-connected voltage-source converters. IEEE Trans Power Syst 25(2):809–820. https://doi.org/10.1109/TPWRS.2009.2032231

Zhong Q-C, Weiss G (2011) Synchronverters: inverters that mimic synchronous generators. IEEE Trans Ind Electron 58(4):1259–1267. https://doi.org/10.1109/TIE.2010.2048839

Zimmerman RD, Murillo-Sánchez CE, Thomas RJ (2011) MATPOWER: steady-state operations, planning, and analysis tools for power systems research and education. IEEE Trans Power Syst 26(1):12–19. https://doi.org/10.1109/TPWRS.2010.2051168

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