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Comprehensive Investigation of Surface Fields Effect on Breakdown Voltage for CMOS SPADs

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ABSTRACT

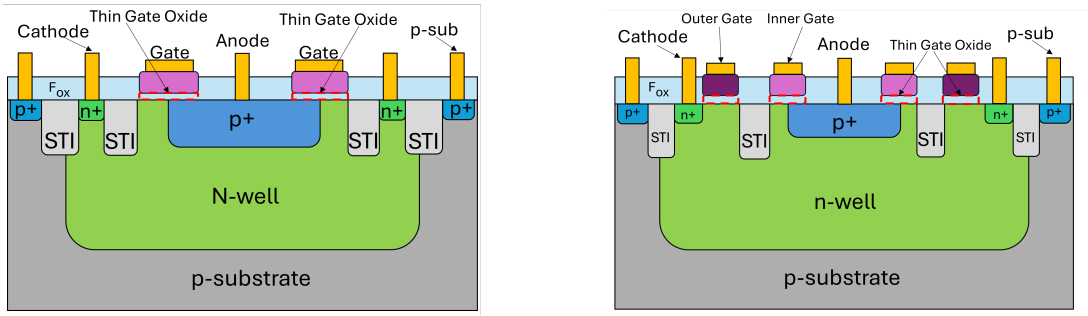
This article presents a comprehensive modeling, design, fabrication, and characterization of single-photon avalanche diodes (SPADs) with surface fields implemented in a standard CMOS process to fully investigate their effect on breakdown voltage. We examine the impact of both single and multiple surface fields on the breakdown voltage by incorporating surface fields over the junction and other diffusion regions of the designed SPAD devices. To the best of our knowledge, this work presents the first comprehensive investigation of SPADs incorporating multiple surface fields, encompassing device design, modeling, fabrication, and experimental characterization. A physics-based device model has been developed using Sentaurus TCAD device simulator, which includes all the features of a real SPAD device with the added surface fields fabricated in a commercial CMOS deep submicron process, including shallow trench isolation (STI). Based on the model, we have conducted a comprehensive parametric analysis to study how the surface field affects breakdown voltage by considering the effect of various key SPAD device parameters, such as gate (surface field) length, gate oxide thickness, active region and N-well geometry and doping concentration. Furthermore, we examine the effect of the applied surface field on other critical device performance parameters, such as electric field distribution, total current density, electrostatic potential, and impact ionization. We further demonstrate that the applied surface field improves SPAD noise performance through modulation of the breakdown voltage. To fully investigate the impact of surface fields on breakdown voltage, we implement and analyze a SPAD device incorporating multiple surface fields in a Sentaurus TCAD simulation framework, with one surface field positioned over the junction and a second over the N-well diffusion region. Finally, we have fabricated and tested the SPAD device incorporating a single and multiple surface fields implemented in a standard 180 nm CMOS process to investigate its effect on breakdown voltage for a real SPAD device and validate the model. Experimental results verify the breakdown voltage modulation with the surface fields, thereby confirming the model accuracy. These findings establish surface-field-induced breakdown voltage modulation as a promising approach for precisely tuning and enhancing SPAD device performance.

Index terms: Single photon avalanche diode (SPAD), Device modeling and simulation, Device fabrication, I-V characteristics, breakdown voltage, surface field.

Introduction

Single Photon Avalanche Diodes (SPADs) are reverse-biased p-n junction photodetectors capable of detecting single photons[1–5]. SPADs are operated in Geiger mode by biasing them above their breakdown voltage, generating a high electric field at the junction that enables single-photon sensitivity. Single-photon sensitivity makes SPADs an ideal photodetector for use in applications requiring high timing precision and low-light operation, including quantum communication[6], quantum computing[7], quantum imaging and sensing[8,9], fluorescence lifetime imaging[10], light detection and ranging (LiDAR)[11], and biomedical applications[12].

To achieve optimal performance, SPADs are traditionally manufactured using specialized processes that ensure avalanche profiles are correctly controlled[2]. However, they have limitations, such as high manufacturing costs, limited scalability, and a lack of integration capabilities with readout electronics. Therefore, CMOS SPADs have attracted significant attention due to their cost-effectiveness and integration capability with readout electronics, resulting in high-speed photodetectors[2–5,13–15]. Despite these advantages, CMOS implementation introduces critical device-physics challenges that directly impact the device performance. A key limitation is the high electric field near the junction edges due to the planar nature of CMOS technology, which triggers premature edge breakdown (PEB)[2]. A common mitigation strategy is the use of guard rings[16–18], which laterally spread the electric field and suppress PEB. However, guard rings consume valuable area and reduce fill factor significantly, affecting the device performance, especially when SPAD pixels are arranged as large arrays for high-resolution imaging.



(a) SPAD incorporates a single surface field

(b) SPAD incorporates multiple surface fields

Figure 1. A cross-sectional view of a SPAD device implemented in a deep submicron CMOS process, incorporating additional (a) single surface field over the junction and (b) multiple surface fields over the junction and N-well diffusion region.

In recent years, perimeter-gated SPADs[16,19–25] have gained significant attention for their ability to prevent PEB and overcome the area-performance tradeoff without unnecessarily enlarging the device. This is achieved by modulating the electric field distribution around the junction through the bias voltage applied to the additional polysilicon gate integrated into the SPAD structure. This concept was first explored for a planar p-n junction in the early research of Grove *et al.*[26] and Temple *et al.*[27]. Later, Dandin *et al.*[16,19,28] incorporated a poly-silicon gate over the high field region of CMOS SPADs (perimeter gated SPADs), as well as using lateral diffusion of adjacent N-wells to suppress PEB and improve their performance. As demonstrated by Habib *et al.* in[20,21], the breakdown voltage of SPADs and their performance, including dark count rate (noise), dynamic range, and sensitivity, can be controlled through the perimeter gate voltage. Based on simple TCAD simulations and experiments, Shawkat *et al.*[22–25] verified the electric field and breakdown modulation of the perimeter-gated SPADs, as well as investigated the performance improvement of silicon photomultipliers implemented using perimeter-gated SPADs.

All these prior works on perimeter-gated SPADs reported in the literature[16,21,23,24] studied the use of a single surface field over the junction using a simple model and large-feature-size CMOS process. However, while this surface field is beneficial for modulating breakdown, it can also induce charge trapping at the oxide surface[26], potentially leading to instability or drift in the breakdown voltage and increased noise levels. Moreover, the single surface field configuration controls the surface potential only over the immediate junction perimeter. However, carriers accumulated at the Si–SiO_2 interface can migrate laterally into the adjacent N-well region beyond the gate boundary, perturbing the near-junction surface potential and causing instability or drift in breakdown voltage, as well as increased dark count rate[21,26,28]. A second surface field placed over the N-well diffusion region can extend surface-potential control over this lateral migration path, similar in principle to the use of multiple biased field plates in planar silicon pn junctions to prevent drift-region charge redistribution[26]. Multiple surface fields, therefore, offer both wider breakdown voltage tuning and improved surface stability, but SPADs with multiple surface fields have not yet been explored.

In this article, we present a comprehensive modeling, design, fabrication, and characterization of SPAD devices with surface fields. We model and design the SPAD device, incorporating both single surface field (Fig. 1a) and multiple surface fields (Fig. 1b) over the junction and N-well diffusion to fully investigate the effects of the surface field on the breakdown voltage. To the best of our knowledge, this is the first implementation and analysis of a SPAD device incorporating multiple surface fields. We have previously explored the effect of the surface field with initial simulations based on a simple model[29–31]. Here, we develop a comprehensive model that includes all features of a real SPAD device with surface fields (gate terminals) implemented in a standard CMOS deep-submicron process, including shallow trench isolation (STI), which was not considered in the prior perimeter-gated SPAD models. Based on the model, we conduct a comprehensive parametric analysis on how device parameters such as gate length, oxide thickness, and doping concentration affect the breakdown voltage of the SPAD device with surface fields, which impacts the device performance. In addition, we examine the effects of the applied surface field on other critical device performance, including electric field distribution, total current density, electrostatic potential, and impact ionization. We further demonstrate the noise improvement of SPAD devices by the applied surface field through modulation of the breakdown voltage. Furthermore, we design, model, and investigate a SPAD device with multiple surface fields for an in-depth understanding of their effect for the first time in this work. Finally, to investigate the modulation of breakdown voltage by surface electric fields in a real SPAD device and validate the proposed model, we fabricate and characterize SPAD devices incorporating single and multiple surface-field configurations using a standard 180 nm CMOS process.

The remainder of this paper is organized as follows. Section 1 presents the operating principle of the surface-field-enhanced SPAD device. Section 2 briefly describes the TCAD modeling framework developed for the implemented SPAD device with

single and multiple surface fields using Sentaurus. Section 3 fully investigates the impact of a single surface field on breakdown voltage across a wide range of important device parameters, including gate length, oxide thickness, and doping concentration. Section 4 presents the analysis of SPADs with multiple surface fields, examining how the inner and outer gates modulate the breakdown voltage independently and jointly. Section 5 demonstrates the noise improvement of SPAD devices by the applied surface field through modulation of the breakdown voltage. Section 6 presents the experimental I-V characteristics of the fabricated SPAD devices with a single surface and multiple surface fields, validating the simulation against measured data. Finally, Section 7 concludes the paper with a summary of the key findings and future works.

1 Operation of SPAD with Surface Field

The SPAD device with surface field functions similarly to a regular SPAD device but offers the additional benefit of a more evenly distributed electric field around the junction due to the applied surface field. The operation of a SPAD begins with photon absorption in the active region. By applying a bias at the gate terminal, a surface field is induced at the junction. This surface field modulates the local carrier concentration near the junction perimeter, thereby reshaping the electric field distribution at the junction edge, preventing PEB, and modulating the breakdown voltage (V_{Br}).

The multiplication factor (M)[32] in a SPAD with surface-field can be expressed as,

$$M = \left\{ 1 - \int_0^{W_D} \alpha_n \exp\left[- \int_0^{W_D} (\alpha_n - \alpha_p) dx \right] dx \right\}^{-1} \tag{1}$$

where α represents the ionization rate, the balance between electron and hole ionization rates determines the uniformity and reliability of avalanche multiplication within the device. Breakdown is reached when the denominator approaches zero, i.e., when the ionization integral satisfies the self-sustaining avalanche condition.

The electric field distribution across the junction follows a parabolic profile[32–34], E:

$$E = E_M \left[1 - \left(\frac{2x}{W} \right)^2 \right] \tag{2}$$

where E_M is the peak electric field and W is the junction width. At the junction perimeter, the corner electric field is significantly elevated due to geometric curvature[16,26,27,35] and is given by:

$$E_{corner} = \frac{V_R}{W_f} + \frac{V_R - V_G}{3C_{ox}} \tag{3}$$

where V_R is the reverse bias voltage, W_f is the field width, V_G is the applied surface field through the gate, and C_{ox} is the oxide capacitance. This equation highlights the role of the geometrical and applied surface field, V_G, in determining the peripheral field strength.

The breakdown voltage of a SPAD with surface field is influenced by the applied surface field near the junction. The relation between the applied surface field and the breakdown voltage has been defined in[20,21,26], and can be expressed as,

$$V_{Br} = mV_G + \beta \tag{4}$$

where m is the slope, which is a function of the oxide thickness and impurity concentration. β is a constant. This linear dependence suggests that the breakdown voltage can be systematically controlled by varying the surface field through the gate voltage, which modulates the carrier concentration in the device.

In an SPAD with a surface field, the breakdown voltage is influenced by the surface field (applied through the gate), oxide thickness, and the critical electric field[26]. It is described by,

$$V_{Br} = \frac{1}{1 + \frac{3C_{ox}}{W_f}} V_G + \frac{3E_{crit}C_{ox}}{1 + \frac{3C_{ox}}{W_f}} \tag{5}$$

where E_{crit} is the critical electric field for breakdown. This equation illustrates how device parameters and external biases affect the breakdown voltage.

In the multiple-surface-field configuration (Fig. 1b), an inner gate is placed over the junction perimeter, serving the same role as the single gate (Fig. 1a), while an outer gate is placed over the N-well diffusion region. The inner gate provides the primary modulation of the junction-edge electric field and controls V_{Br}. The outer gate provides an additional degree of control over the surface potential in the N-well region, helping to manage the carrier distribution across the broader device surface. Together, the two gates offer a wider and more flexible tuning range of V_{Br}.

2 Device TCAD Modeling

A physics-based TCAD model has been developed using the Sentaurus Device simulator[36] to investigate the effect of surface fields on SPAD breakdown behavior. The model incorporates all key features of a real SPAD device fabricated in a standard 180 nm CMOS deep-submicron process. It includes a p^+/N-well junction embedded in a p-type substrate, STI-defined isolation, two symmetric gate segments, one on each side of the junction perimeter, forming a single electrically connected surface field, and Gaussian doping profiles[16] for all regions. The key device parameters used in the model are listed in Table 1.

The electrical behavior of the device is simulated by solving a fully coupled Poisson–electron–hole system of equations self-consistently. Fermi statistics are enabled, and the effective intrinsic carrier density is modeled using the OldSlotboom formulation[37–39] to account for bandgap narrowing in heavily doped regions. To account for surface-field effects near the oxide interface, the van Dort quantum correction model[40] is also included. Carrier transport includes doping-dependent mobility, normal-field mobility degradation, and high-field velocity saturation based on the gradient of the quasi-Fermi potential[36]. The silicon mobility model is further strengthened using the Philips unified mobility model[39] to better represent carrier transport in the doped regions.

The total mobility combining all surface and bulk contributions is obtained via Matthiessen's rule[32,41]:

$$\frac{1}{\mu_T} = \frac{1}{\mu_b} + \frac{1}{\mu_{ap}} + \frac{1}{\mu_{srs}} \tag{6}$$

where μ_b is the bulk mobility from the Masetti and Canali models[42–44], μ_{ap} accounts for acoustic-phonon scattering, and μ_{srs} accounts for surface-roughness scattering at the Si–SiO_2 interface.

Generation and recombination mechanisms are modeled to capture both pre-breakdown leakage and the onset of avalanche multiplication. Trap-assisted recombination is modeled using the Shockley–Read–Hall (SRH) model[45,46] with doping-dependent carrier lifetimes:

$$R_{\mathrm{SRH}}^{\mathrm{net}} = \frac{np - n_{i,\mathrm{eff}}^2}{\tau_p(n+n_1) + \tau_n(p+p_1)} \tag{7}$$

where n and p are the electron and hole densities, $n_{i,\mathrm{eff}}$ is the effective intrinsic carrier density from the OldSlotboom model, τ_n and τ_p are doping-dependent electron and hole lifetimes, and n_1, p_1 are SRH reference densities determined by the trap energy level E_{trap} relative to the intrinsic level. Band-to-band tunneling is also considered for generation and recombination. Impact ionization is modeled[47,48] with the driving field taken as the component of the electric field parallel to the current flow direction, which is the physically appropriate choice for the laterally non-uniform SPAD geometry. The avalanche generation rate is:

$$G_{ii} = \alpha_n n v_n + \alpha_p p v_p \tag{8}$$

where α_n and α_p are the electron and hole impact ionization coefficients, and v_n, v_p are the carrier drift velocities. The multiplication factor M and the self-sustaining breakdown condition are determined from the ionization integral[32,49], as defined in (1). Breakdown occurs when M tends to infinity (∞), i.e., when the ionization integral equals unity.

The electrostatic potential distribution is obtained by self-consistently solving Poisson's equation at each bias step[32,34,36]:

$$\nabla \cdot \left(\varepsilon \nabla \varphi + \vec{P}\right) = -q\,(p - n + N_D - N_A) - \rho_{\mathrm{trap}} \tag{9}$$

where ε is the material permittivity, $\vec{P}$ is the ferroelectric polarization (zero for silicon and SiO_2), q is the electron charge, N_D and N_A are the ionized donor and acceptor doping concentrations, and ρ_{trap} is the trapped and fixed charge density at the oxide interface. The resulting electric field $\vec{E} = -\nabla\varphi$ drives both avalanche multiplication and the gate-induced surface carrier modulation that controls the breakdown voltage.

Table 1. Key Device Parameters Used in TCAD Modeling[16,25,53]

Parameter	Value
P^+ peak doping (N_a)	1×10^{20} cm^{-3}
N-well peak doping (N_d)	1.22×10^{17} cm^{-3}
P-substrate doping	1×10^{15} cm^{-3}
Gate oxide thickness	12.5 nm
Polysilicon gate Length	3.0 μm
Active region Length	15.0 μm
N-well length	30.0 μm
P-substrate	40.0 μm

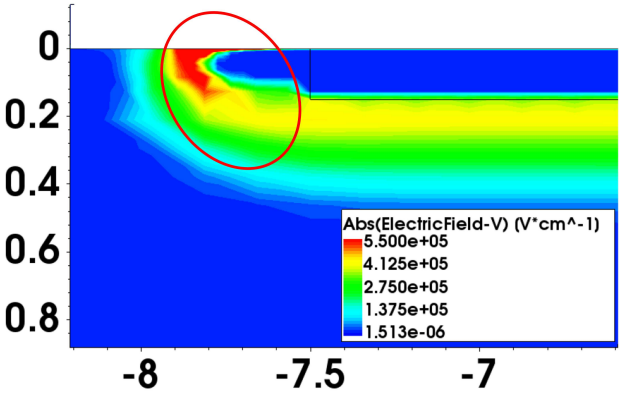


Figure 2. Electric field distribution of a conventional SPAD showing the highest electric field at the perimeter, causing PEB (circled in red). The x-axis and y-axis represent length and width in μm, respectively.

For breakdown voltage extraction, the resistor-based method[50] is used in the device simulation. The gate terminal is first biased quasistatically to the desired value, after which the reverse bias at the anode is increased gradually through a large external resistor while the cathode and substrate contacts are kept at ground. The breakdown voltage is then extracted from the simulated I–V characteristics using the second-order derivative method[51,52]. The physical models are solved self-consistently with Poisson's equation at every bias step, ensuring that the simulated breakdown behavior and surface-field modulation are physically accurate and directly comparable to the measured I–V characteristics of the fabricated SPAD devices with surface fields.

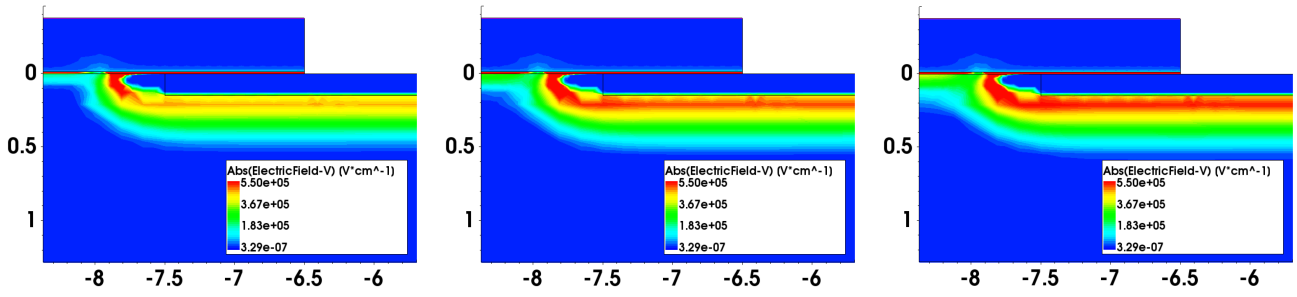
3 Investigation of the Impact of Single Surface Field on Breakdown Voltage of SPAD with Device Parameters Effect

This section presents the simulation results and analysis of the developed model for the SPAD device with surface field implemented in the Sentaurus Device physics TCAD simulation framework. We have implemented the SPAD device with a single-surface field around the junction, incorporating all features of a real SPAD device with a gate terminal, implemented in a standard deep-submicron CMOS process, including STI. First, we verify the modulation of the electric field by the applied surface field, resulting in PEB mitigation. In addition, we conduct a comprehensive investigation of the effects of active region doping concentration, active region length, active region thickness, gate oxide thickness, gate (surface field) length, N-well thickness, and N-well doping concentration on the breakdown voltage of SPAD devices with a single surface field. Furthermore, we examine how the surface field affects the total current density, electrostatic potential, and impact ionization, taking device parameters into consideration.

3.1 Effect of Surface Field on Electric Field Distribution

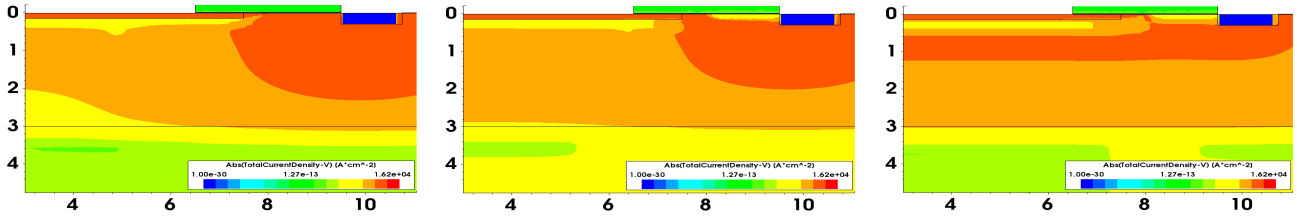
Fig. 2 shows the electric field distribution of a regular SPAD without any STI and applied surface field. It is observed that the electric field is maximum at the periphery of the junction, causing PEB. The circled region (in Fig. 2) highlights a strong electric field, a hot spot at the junction corner or edge. Since the CMOS technology is planar, the peak electric field occurs at the junction perimeter, reaching the critical level required for breakdown much earlier than at the remainder of the junction. Therefore, the junction edge breaks down earlier than the rest of the junction, causing PEB[2].

Fig. 3 presents the electric field distribution for a SPAD with STI at three applied surface-field magnitudes ($|Vg|$). The figures show that, with $|Vg|$ at 2 V (Fig. 3a), some field enhancement near the surface/perimeter is still visible; however, as $|Vg|$ increases, the surface potential increasingly reshapes the near-surface field lines and suppresses the localized electric field. At $|Vg|$ of 4 V (Fig. 3b), the high electric field region becomes less at the corner and spreads more evenly along the junction. Increasing $|Vg|$ to 6V (Fig. 3c), the distribution is noticeably more even across the junction. The applied surface field induces carrier accumulation near the silicon–oxide interface, which electrostatically limits the peak peripheral electric field. As a result, the maximum electric field shifts away from the junction edge, leading to a uniform electric field distribution throughout the junction and causing a uniform, junction-wide breakdown. This observation verifies that the applied surface field modulates the electric field, making it uniform throughout the junction by controlling the carrier concentration.



(a) $|Vg|$ *at* 2 *V* **(b)** $|Vg|$ *at* 4 *V* **(c)** $|Vg|$ *at* 6 *V*

Figure 3. Electric field distribution of SPAD at different applied surface fields, improving electric field uniformity throughout the junction, thereby preventing PEB. The x-axis and y-axis represent length and width in μm, respectively.



(a) N_a of 1×10^{19} cm^{-3} and $|Vg|$ at 0 V **(b)** N_a of 1×10^{19} cm^{-3} and $|Vg|$ at 6 V **(c)** N_a of 1×10^{20} cm^{-3} and $|Vg|$ at 6 V

Figure 4. Effect of applied surface field and active region doping concentration on the Total Current Density of the designed SPAD device.

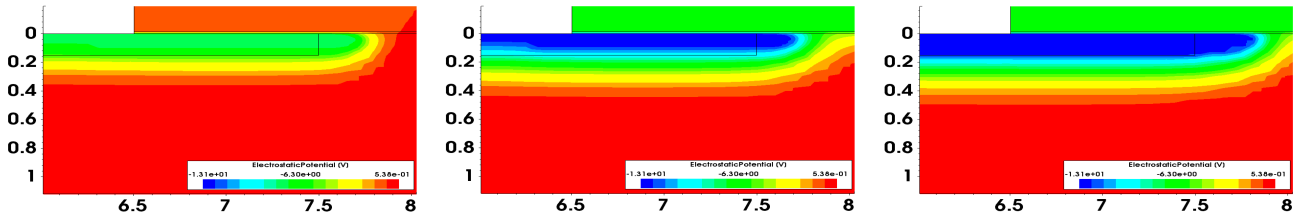
3.2 Effect of Active Region Doping Concentration on Performance of SPAD with Surface Field

The performance of SPAD devices is significantly influenced by the active-region doping concentration, particularly through its effects on junction properties and the distribution of electric fields within the device. First, we examine the effect of the surface field on total current density, electrostatic potential, and impact ionization with variation of active region doping concentration. Finally, we investigate how active-region doping concentration and gate bias affect the breakdown voltage of SPAD devices, which ultimately impacts their key performance[51,54,55].

Fig. 4 shows the effect of the applied surface field and p^+ doping concentration on the total current density of the device. For N_a of 1×10^{19} cm^{-3} and $|Vg|$ of 0 V (Fig. 4a), the current density is strongly concentrated at the junction perimeter, forming a narrow high-current channel along the device edge. This edge-dominated current path arises because the locally elevated electric field at the junction perimeter drives carrier drift preferentially through the edge region rather than through the bulk junction, creating current crowding that represents a reliability concern due to localized power dissipation. Applying $|Vg|$ of 6 V (Fig. 4b) effectively reroutes the current path by modulating the carrier concentration at the Si–SiO_2 interface, suppressing the edge channel and forcing the current to flow through the bulk junction region, producing a uniform distribution with no localized hot spots. Increasing N_a to 1×10^{20} cm^{-3} while maintaining $|Vg|$ at 6 V (Fig. 4c) creates a localized current near the surface despite the applied gate bias. This higher doping both narrows the depletion width, raising the peak electric field at the junction perimeter[21,56], and produces a much higher carrier concentration on the p^+ side that dominates the current path independently. These results demonstrate that the doping concentration directly influences the current-flow pattern, while the surface field is the dominant factor.

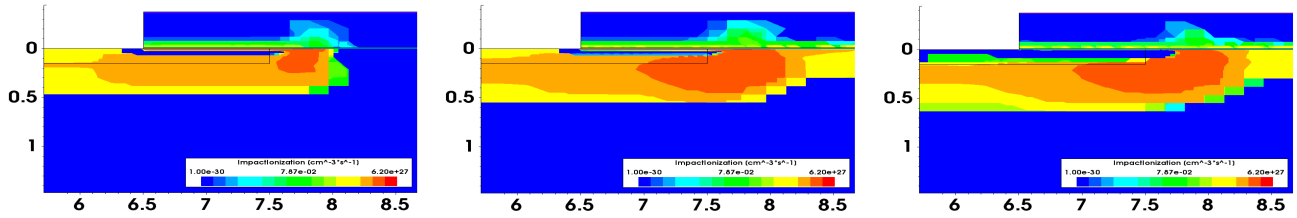
Fig. 5 presents the electrostatic-potential (ϕ) distribution as a function of the bias applied at the surface field and the p+ doping concentration. For N_a of 1×10^{19} cm^{-3} and $|Vg|$ of 0 V (Fig. 5a), the bulk potential is relatively uniform, but a sharp electrostatic potential drop concentrates at the STI corner, where fixed oxide charges and the geometric curvature of the planar junction force the depletion region to terminate abruptly. This compresses the reverse-bias potential drop into a narrow region at the edge, producing the steep $\nabla\phi$. Applying $|Vg|$ of 6 V (Fig. 5b) introduces a surface potential that widens the electrostatic potential drop and makes the $\nabla\phi$ uniform at the junction edge, reducing the peak perimeter field without changing the reverse bias or device geometry. Increasing N_a to 1×10^{20} cm^{-3} at $|Vg|$ of 6 V (Fig. 5c). The gate modulates the near-surface potential, while the doping governs the bulk distribution[26,32]. Thus, the surface field progressively redistributes the potential profile, while higher N_a narrows the depletion region and steepens the potential drop.

The spatial distribution of impact ionization under varying applied surface fields and p^+ doping concentrations is shown in Fig. 6, directly indicating the regions where the ionization integral approaches unity and avalanche breakdown is most likely to



(a) N_a of 1×10^{19} cm^{-3} and $|Vg|$ at 0 V **(b)** N_a of 1×10^{19} cm^{-3} and $|Vg|$ at 6 V **(c)** N_a of 1×10^{20} cm^{-3} and $|Vg|$ at 6 V

Figure 5. Effect of applied surface field and active region doping concentration on Electrostatic Potential.



(a) N_a of 1×10^{19} cm^{-3} and $|Vg|$ at 0 V **(b)** N_a of 1×10^{19} cm^{-3} and $|Vg|$ at 6 V **(c)** N_a of 1×10^{20} cm^{-3} and $|Vg|$ at 6 V

Figure 6. Change in Impact Ionization due to applied surface field with doping concentration variation.

occur. In all cases, ionization is confined to the near-surface junction region. At N_a of 1×10^{19} cm^{-3} and $|Vg|$ of 0 V (Fig. 6a), ionization is sharply localized at the junction perimeter, where α_n and α_p reach their critical values, so the ionization integral of Eq. (1) saturates at the perimeter before the bulk junction, confirming edge-triggered breakdown. Increasing $|Vg|$ to 6 V (Fig. 6b) suppresses the perimeter field peak and reduces edge ionization, forcing the integral to be satisfied across a broader junction area rather than at a single edge point. Leading to a desirable junction-wide avalanche. Increasing N_a to 1×10^{20} cm^{-3} at $|Vg|$ of 6 V (Fig. 6c) produces a broader, more intense ionization region, as the higher doping narrows the depletion region and raises the peak field, increasing α_n and α_p and lowering the voltage required to satisfy the ionization threshold[47,48,56]. Overall, applying the surface field broadens the impact ionization toward a junction-wide avalanche, and increasing the doping intensifies and widens the ionization.

Finally, we have investigated the impact of the surface field on the breakdown voltage for varying p^+ doping concentrations and have presented in Fig. 7. Fig. 7a and 7b illustrate the I–V characteristics for two p^+ doping concentrations of 1×10^{19} cm^{-3} and 1×10^{20} cm^{-3}, while varying the applied surface field $|Vg|$ from 0V to 6V. In both cases, the breakdown voltage increases with the increase of $|Vg|$, confirming that the applied surface field provides strong tunability for V_{Br}. This is because the applied surface field modulates the carrier concentration. This change in the carrier concentration reshapes the electric field distribution and changes the breakdown voltage[57,58].

Fig. 7c, the 3D surface plot, further demonstrates the variation of the breakdown voltage for both the active region doping concentration and the gate voltage. The figure clearly shows that, for higher active-region doping concentrations, the breakdown voltage decreases significantly, particularly at $|Vg|$ of 6 V. The active-region doping concentration directly affects the depletion region. This results in a lower breakdown voltage because the depletion region becomes narrower, requiring less energy to initiate avalanche multiplication. The difference in breakdown voltage between the two doping concentrations can be attributed to the impact ionization process, which is more efficient in regions of higher doping concentrations. A higher active-region doping concentration results in a larger number of carriers accelerated to initiate the impact ionization, thereby decreasing the breakdown voltage[56].

3.3 Effects of Active Region Length on Breakdown Voltage

Fig. 8a and Fig. 8b show the reverse I–V characteristics of the SPAD device with surface field for active region lengths of 11 μm and 19 μm, respectively, with the applied surface field $|Vg|$ varied from 0 V to 6 V. In both cases, increasing $|Vg|$ systematically shifts the breakdown voltage to higher reverse voltages, confirming that the applied surface field is the control parameter for V_{Br}. This behavior arises because the gate-induced surface potential modulates the carrier concentration[57,58], which electrostatically reshapes the electric field distribution at the junction perimeter and raises the reverse voltage required to satisfy the self-sustaining avalanche condition defined in Eq. (1). Furthermore, in both figures, the breakdown transitions remain sharp and well-defined across all $|Vg|$ steps, indicating a smoother avalanche operation.

Fig. 8c shows the breakdown voltage as a function of the applied surface field $|Vg|$ for both active region lengths of 11 μm

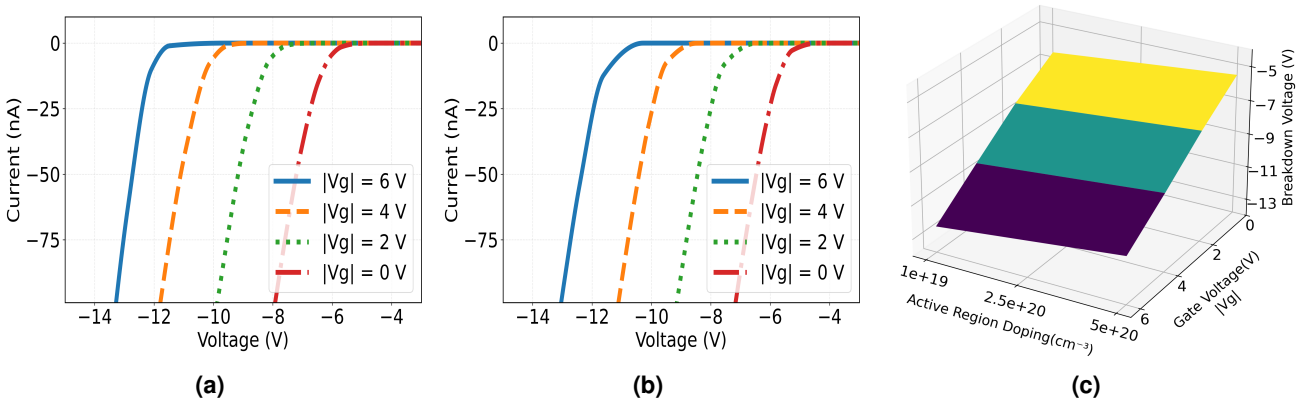


Figure 7. Reverse I–V characteristics of the designed SPAD device for different surface field $|Vg|$, with two P^+ peak doping concentrations of (a) 1×10^{19} cm^{-3} and (b) 1×10^{20} cm^{-3} illustrating the modulation of avalanche breakdown voltage. (c) 3D surface plot of breakdown voltage of SPAD device as a function of active region doping (Na) and applied surface field $|Vg|$.

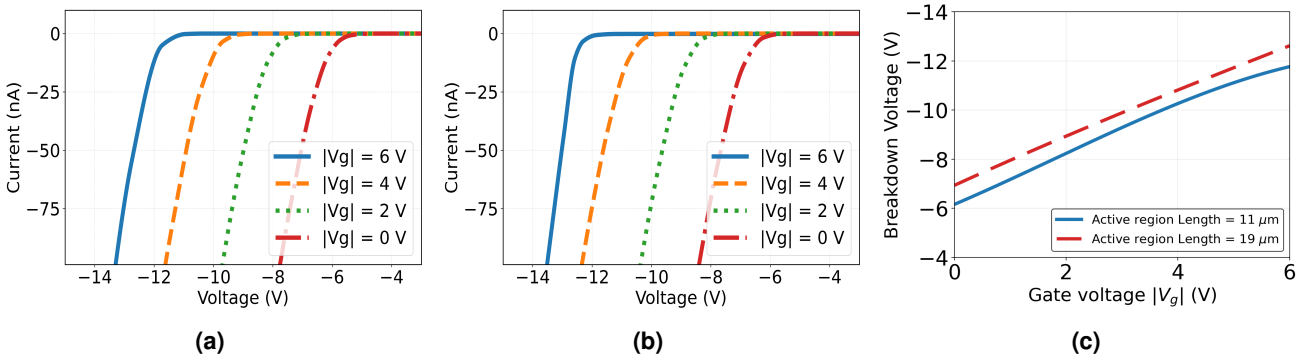


Figure 8. Modulating breakdown voltage of a SPAD device by the surface field at different active region lengths of (a) 11 μm and (b) 19 μm, (c) Breakdown voltage of SPAD with surface field as a function of active region length and gate bias $|Vg|$.

and 19 μm. Both curves show a nearly linear increase in V_{Br} with $|Vg|$, consistent with Eq. (4), confirming that the surface field is the primary control parameter for V_{Br} regardless of the active region length. The longer active region (19 μm) has a higher breakdown voltage magnitude than the shorter one (11 μm) at each $|Vg|$. This behavior occurs because a longer active region extends the depletion region over a greater lateral distance, distributing the electric field over a wider spatial extent. For a given applied reverse bias, this reduces the peak field intensity at the junction. A higher reverse voltage is therefore required to accelerate carriers to the energy threshold for impact ionization and sustain the avalanche condition, thereby increasing the breakdown voltage.

3.4 Effect of Active Region Thickness on Breakdown Voltage

We have presented the I–V characteristics with variation in the active region thickness from 0.10 μm to 0.25 μm with a variation of the applied surface-field ($|Vg|$) in Fig. 9. As shown in Fig. 9a and 9b, increasing $|Vg|$ increases the breakdown voltage, indicating that the applied surface field increases V_{Br} as expected. In addition, for any fixed $|Vg|$, the thicker p$^+$ region exhibits a higher breakdown voltage, and this offset becomes more pronounced at higher $|Vg|$. This trend suggests that increasing the active-region thickness alters the junction field profile by expanding the depletion region and reducing the peak electric field for a given reverse bias; therefore, a higher reverse voltage is required to reach the critical impact-ionization condition, leading to an increased V_{Br}[52,59]. In summary, these results provide crucial insights for optimizing device performance. Both the active region thickness and the applied surface field can effectively modulate the breakdown voltage and improve device performance.

3.5 Gate Oxide Thickness Effects on Breakdown Voltage

Fig. 10a and Fig. 10b show the current-voltage characteristics of the SPAD under different applied surface fields and oxide thicknesses of 10 nm and 12 nm. The oxide thickness range considered in this study is consistent with that of a standard

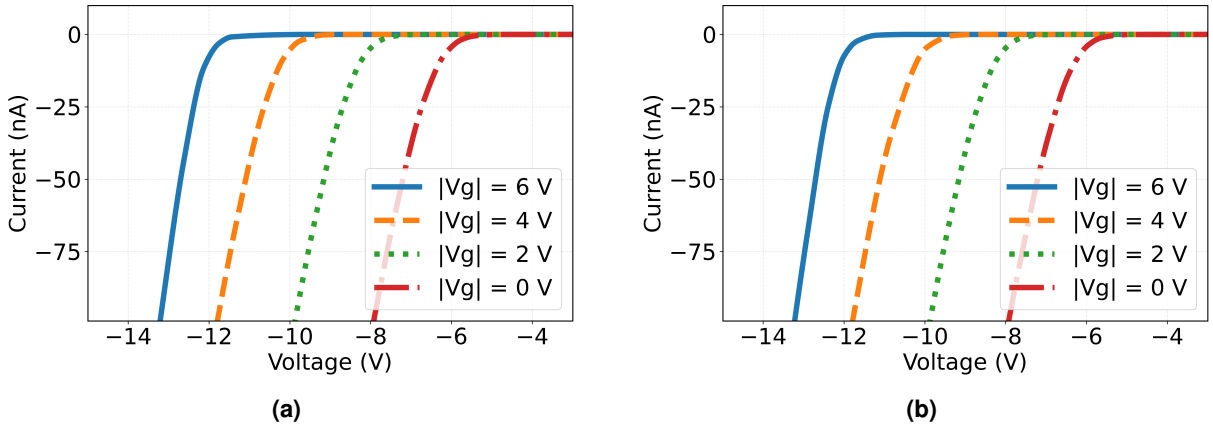


Figure 9. I–V characteristics of the SPAD device for variation of surface fields at different active region thickness of (a) 0.10 μm and (b) 0.25 μm, showing the shift in breakdown voltage as $|Vg|$ is varied from 0 to 6 V.

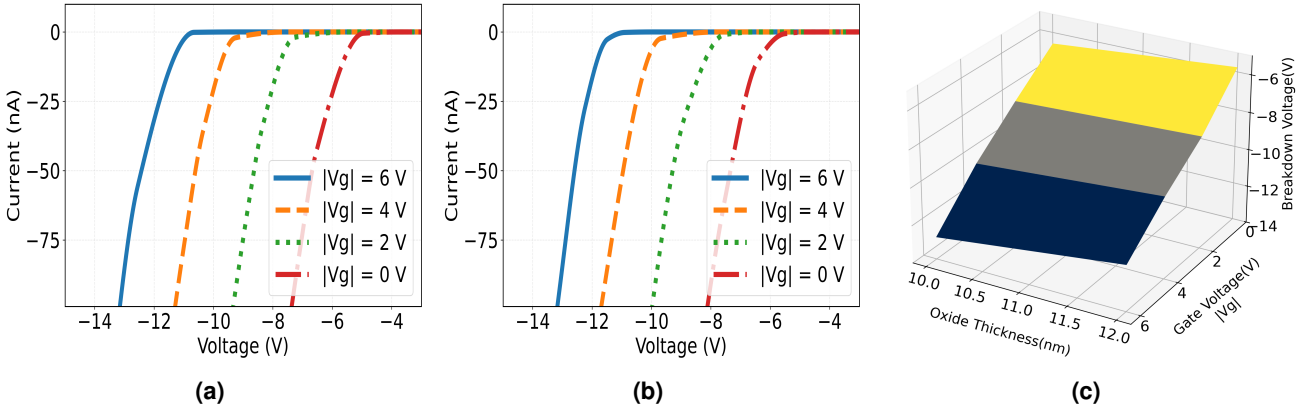


Figure 10. Effects of applied surface field on breakdown voltage of a SPAD device at different oxide thickness, with oxide thickness of (a) 10 nm and (b) 12 nm. (c) Dependence of breakdown voltage on oxide thickness of the designed SPAD device with surface field for different applied biases at surface fields $|Vg|$.

commercial 180 nm CMOS process[53,60–62]. In both cases, the breakdown voltage increases with the increase in applied surface field $|Vg|$ as expected. The increase in breakdown voltage is also the same in both cases. This behavior is consistent with gate-induced modulation of the carrier concentration and its effect on the breakdown voltage[26].

Fig. 10c represents the extracted breakdown voltages as a function of oxide thickness and $|Vg|$ in a 3D surface plot. The surface plot shows that the V_{Br} decreases with increasing gate oxide thickness. This behavior arises from the dependence of gate–silicon electrostatic coupling on oxide thickness. A thicker gate oxide reduces the gate capacitance, thereby weakening the coupling between the applied surface field and the silicon surface potential. Consequently, the surface-field modulation of the peripheral electric field is reduced, leading to a lower breakdown voltage for thicker oxides[63]. These results strongly suggest that both oxide thickness and gate voltage significantly affect the breakdown behavior of SPAD. Optimizing these parameters enables better control of the device's breakdown voltage, thereby improving device performance.

3.6 Gate Length Effects on Breakdown Voltage

Fig. 11 shows the I–V characteristics of the designed SPAD device with surface field for two different gate lengths of 1.5 μm and 3 μm with variation of the applied surface field bias ($|Vg|$). As shown in Fig. 11, with increasing gate voltage, the breakdown voltage increases in a similar way as observed earlier. In addition to the strong $|Vg|$ dependence, a systematic gate-length effect is observed. For a fixed $|Vg|$, increasing the gate length from 1.5 μm to 3.0 μm yields a lower breakdown-voltage magnitude. This indicates that extending the gate length changes the electrostatic coupling between the surface field and the junction edge, thereby modifying the local peak-field condition required for avalanche initiation. A longer gate provides a larger effective field-control region along the perimeter, which can shift the edge-field distribution and lower the breakdown voltage for the

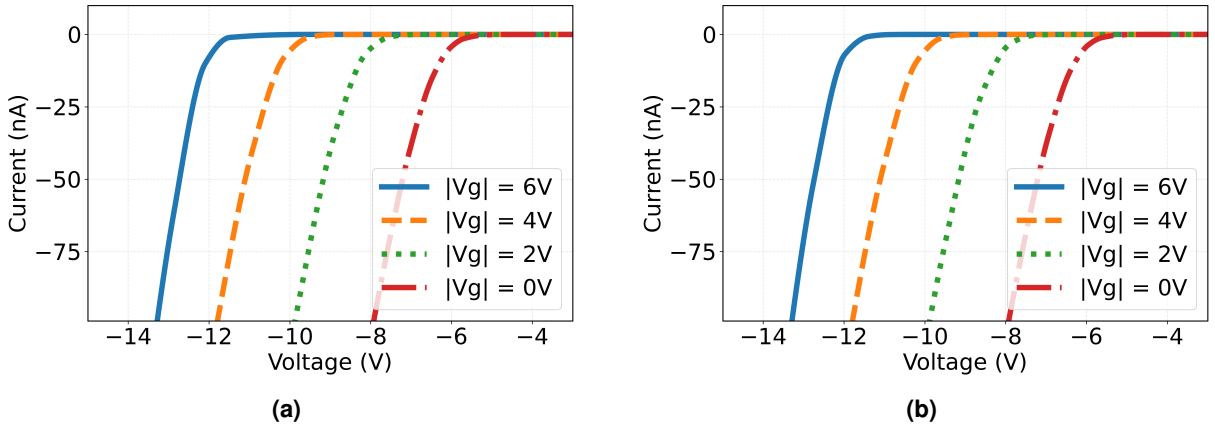


Figure 11. Breakdown voltage modulation through the applied surface field at different gate lengths of (a) 1.5 μm and (b) 3.0 μm.

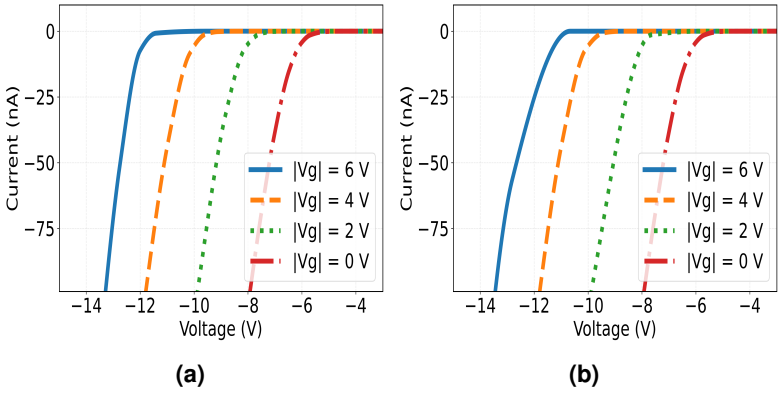


Figure 13. Effects of applied surface field on breakdown voltage of a SPAD device for two different N-well thicknesses, with N-well thickness of (a) 1 μm and (b) 5 μm.

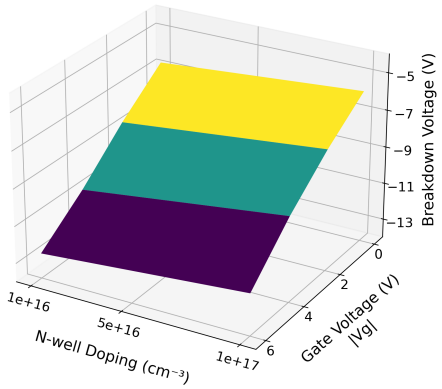


Figure 14. Impact of N-well doping concentration and applied surface field on the breakdown voltage.

same applied $|Vg|$[64]. Overall, these findings highlight the impact of gate length and applied surface fields on optimizing the SPAD breakdown voltage for enhanced device performance, as both the gate length and the applied surface field can modulate the breakdown voltage.

3.7 N-well Thickness Effect on Breakdown Voltage

Fig. 13 demonstrates the effect of varying the N-well thickness for 1 μm (Fig. 12a) and 5 μm (Fig. 12a) on the breakdown voltage at different applied surface fields ($|Vg|$ of 0 V and 6 V). It is observed that the breakdown voltage increases as the applied surface field increases for both N-well thicknesses. However, a direct comparison between Fig. 12a and Fig. 12b indicates that changing the N-well thickness from 1 μm to 5 μm does not produce a noticeable change in the breakdown voltage at a given $|Vg|$. In both cases, V_{Br} increases with $|Vg|$, confirming that the surface field modulates the breakdown voltage for both N-well thicknesses. The overall variation in breakdown voltage due to changes in N-well thickness remains negligible, suggesting that the avalanche condition is primarily governed by the local electric-field profile at the p^+/N-well junction rather than by the overall N-well thickness. This is because the depletion width and peak electric field at breakdown are determined mainly by the doping levels and the applied reverse bias, while the additional N-well thickness beyond the depletion edge remains quasi-neutral and contributes minimally to the peak-field condition responsible for avalanche initiation[65].

Table 2. Summary of the effect of each device parameter on the breakdown voltage of the SPAD with a single surface field. The direction indicates the change in V_{Br} magnitude when the listed parameter is increased, and the strength reflects the relative magnitude of the V_{Br} shift observed over the simulated parameter range.

Parameter increased	Effect on V_{Br}	Strength
Applied surface field $\|Vg\|$	↑ Increase	**Strong**
Active region doping N_a	↓ Decrease	**Strong**
N-well doping N_d	↓ Decrease	**Strong**
Active region thickness	↑ Increase	Moderate
Gate oxide thickness	↓ Decrease	Moderate
Gate length	↓ Decrease	Moderate
Active region length	↑ Increase	Weak
N-well thickness	Negligible	Negligible

3.8 N-well Doping Concentration Effect on Breakdown Voltage

Fig. 14 presents the breakdown voltage as a function of both N-well doping concentration and applied surface field $|Vg|$, capturing both dependencies simultaneously. In the figure, V_{Br} increases with $|Vg|$, consistent with the surface-field modulation mechanism described throughout Section 3. The dominant effect in the surface plot is the strong dependence on N-well doping, as the donor concentration increases from $1 \times 10^{16}\,\mathrm{cm}^{-3}$ to $1 \times 10^{17}\,\mathrm{cm}^{-3}$, the breakdown voltage decreases substantially as expected. This is because higher N-well doping narrows the depletion width and raises the peak electric field at the p^+/N-well junction for a given applied reverse bias, increasing the impact ionization rate and lowering the required avalanche breakdown voltage[66]. These results confirm that both the applied surface field and the N-well doping concentration significantly influence V_{Br}. Overall, higher gate voltages increase the breakdown voltage, whereas higher N-well doping concentrations reduce it.

3.9 Summary of Key Device Parameter Effects on Breakdown Voltage of SPAD with Surface Field

Table 2 summarizes the influence of each investigated device parameter on the breakdown voltage of the SPAD with a single surface field, consolidating the results presented in Section 3. The parameters fall into three groups according to the magnitude of their effect on V_{Br}. The first group, consisting of the applied surface field $|Vg|$, the active-region doping N_a, and the N-well doping N_d, has the strongest influence. Increasing $|Vg|$ raises V_{Br} across every device configuration studied, because the gate-induced surface potential modulates the carrier concentration at the Si–SiO_2 interface and relieves the field crowding at the junction perimeter. In contrast, increasing either N_a or N_d lowers V_{Br}, because higher doping narrows the depletion region and raises the peak electric field at the p^+/N-well junction for a given reverse bias. The second group, comprising the active region thickness, the gate oxide thickness, and the gate length, has a moderate effect. A thicker active region widens the depletion region and increases V_{Br}, whereas a thicker gate oxide weakens the gate–silicon electrostatic coupling and a longer gate alters the edge-field distribution along the perimeter, both of which reduce V_{Br}. The third group includes the active region length, which produces only a weak increase in V_{Br} through lateral spreading of the depletion region, and the N-well thickness, which has a negligible effect because the region beyond the depletion edge remains quasi-neutral and does not contribute to the peak-field condition. Notably, among all the parameters considered, the applied surface field is the only one that can be adjusted electrically after fabrication, whereas the remaining parameters are fixed by the process and layout. The surface field therefore provides a post-fabrication control knob for tuning V_{Br} and suppressing PEB, while the process and geometric parameters set the baseline breakdown voltage around which this tuning operates. These results provide practical design guidelines for SPADs with surface fields implemented in standard CMOS technologies.

4 Investigation of the Impact of Multiple Surface Fields on Breakdown Voltage of SPAD device

Despite the benefits of incorporating a single-surface field over the junction into the SPAD device, some carriers may migrate toward the oxide surface, causing charge trapping and instability[26]. This limitation of the SPAD with a single-surface field design can be addressed by considering a multiple-surface field configuration while adopting the benefits of surface fields. To comprehensively examine the impact of surface fields on the breakdown voltage, we have designed and implemented a SPAD device with multiple surface fields using the Sentaurus Device physics TCAD simulator for the first time in this work. For this implementation, we have incorporated one surface field over the junction (inner gate) and a second surface field over the N-well

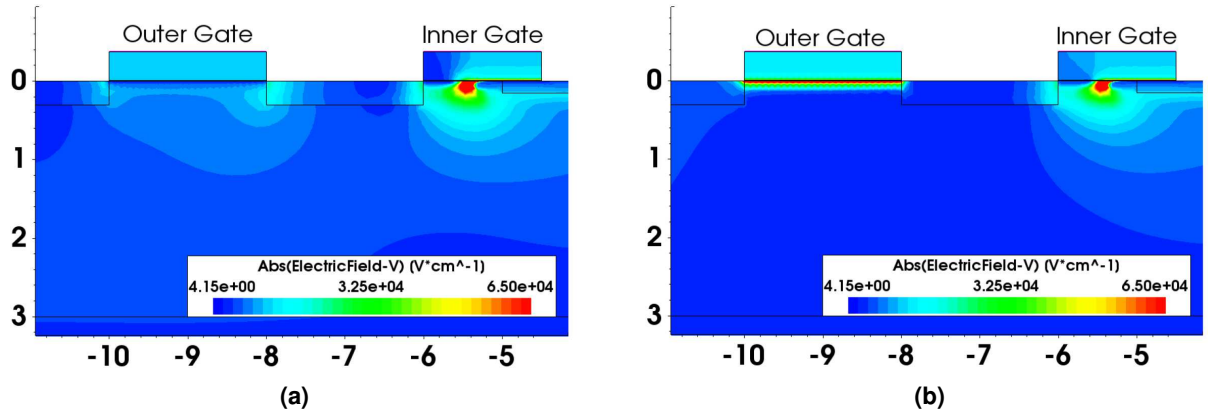


Figure 15. Electric field distribution of double-gated SPAD varying outer gate voltage $|Vg\ out|$ of (a) 0 V and (b) 6 V with constant $|Vg\ in|$ of 0 V.

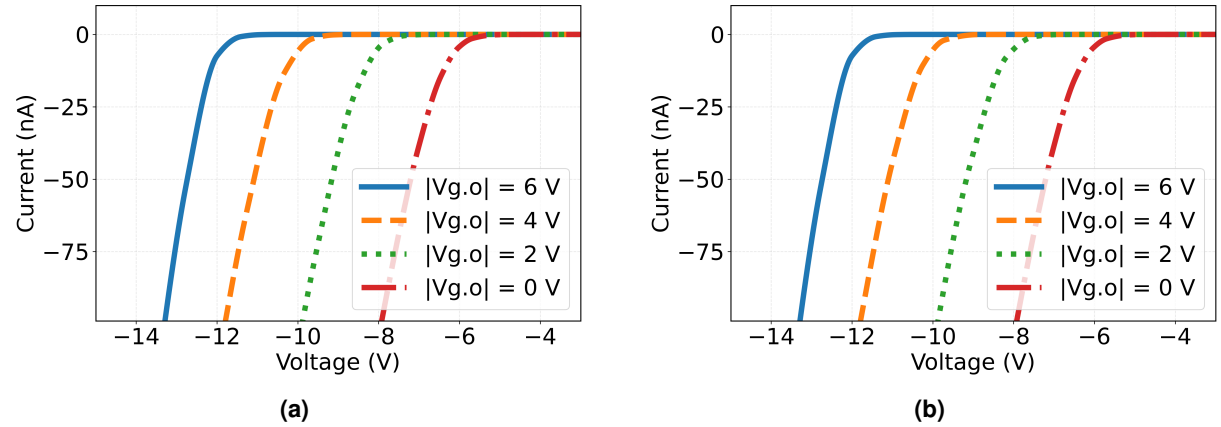


Figure 16. Simulated I–V characteristics of the double-gated SPAD with (a) inner gate ($|Vg\ in|$) held at a constant bias of 0 V and (b) $|Vg\ in|$ held at a constant bias of 6 V, while the outer gate ($|Vg\ out|$) is being swept from 0 V to 6 V, showing the modulation of breakdown voltage by the controlling gate.

diffusion region (outer gate). In our developed model, we have considered all features of a real SPAD device with double gate terminals implemented in a standard deep-submicron CMOS process, including STI, as shown in the cross-section of Fig. 1b. Using the developed model, we investigate how each surface field independently modulates the breakdown voltage and how multiple surface fields interact when biased simultaneously. This section presents the results and analysis for the implemented SPAD device with multiple surface fields.

4.1 Effect of Surface Field on Electric Field Distribution

Fig. 15 shows the electric field distribution of the multiple-surface-fields SPAD at two different applied surface field conditions, where outer voltage $|Vg\ out|$ is kept fixed at 0 V at first (Fig. 15a) and then at 6 V (Fig. 15b). The inner gate voltage $|Vg\ in|$ is set to 0 V in both cases. Some localized field enhancement near the junction perimeter is still visible, similar to what is observed in the single-surface-field case in Fig. 3a. When the outer gate voltage $|Vg\ out|$ is increased to 6 V (Fig. 15b), the electric field near the junction perimeter becomes noticeably more uniform, with a significantly reduced localized high-field region at the junction edge. The applied surface field over the junction perimeter and the outer surface field over the N-well diffusion region work together to modulate the carrier concentration across a wider surface area, extending the field redistribution effect beyond the junction edge into the N-well region. This broader modulation region is a key distinction from the single-surface-field case in Section 3.1, where the field redistribution is confined primarily to the junction's immediate perimeter. The combined action of the two surface fields reshapes the electric field more uniformly across the device, promoting a more junction-wide, uniform breakdown condition while reducing the risk of localized PEB at the junction corner. Overall, the electric field distribution results confirm that the multiple-surface-field configuration provides more effective suppression of junction-edge field crowding.

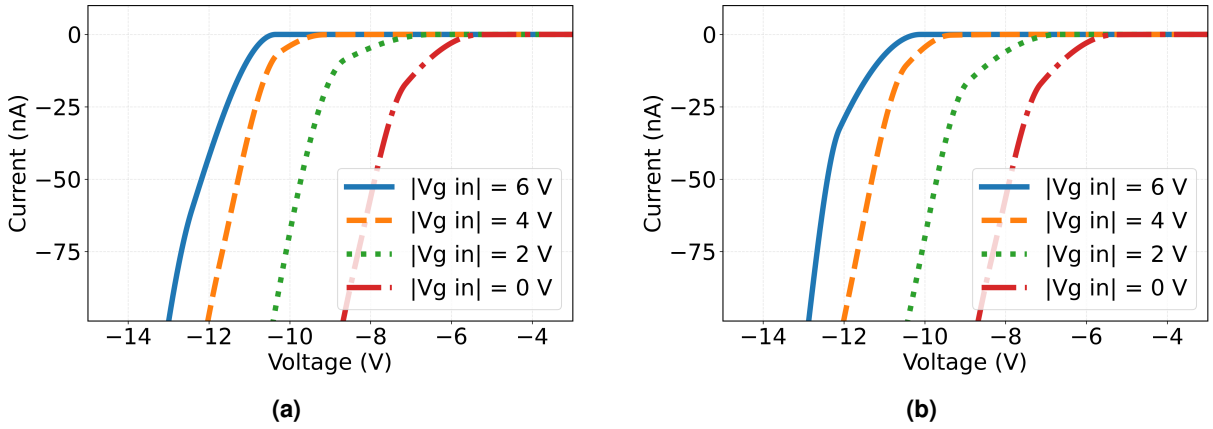


Figure 17. IV characteristics for double-gated SPAD for a constant outer gate voltage ($|Vg\ out|$) of (a) 0 V and (b) 6 V while the inner gate voltage ($|Vg\ in|$) was varied from 0 V to 6 V.

4.2 Effect of Surface Field on Breakdown Voltage with Varying Outer Gate Bias

Fig. 16 presents I–V characteristics of the designed SPAD device incorporating multiple surface fields with varying outer gate voltage while keeping the inner gate voltage ($|Vg\ in|$) fixed at 0 V (Fig. 16a) and at 6 V (Fig. 16b). In both cases, increasing the outer surface field shifts the breakdown voltage to higher reverse voltages, demonstrating that the outer surface field over the N-well region directly modulates V_{Br}. This behavior is consistent with the surface field effect described in Section 3, in which the applied surface field modulates the carrier concentration near the silicon–oxide interface, reshaping the electric field distribution and changing the breakdown voltage.

4.3 Effect of Surface Field on Breakdown Voltage with Varying Inner Gate Bias

Fig. 17a and Fig. 17b present the complementary simulations, where the inner surface field ($|Vg\ in|$) is varied from 0 V to 6 V while the outer surface field ($|Vg\ out|$) is held constant at 0 V (Fig. 17a) and 6 V (Fig. 17b), respectively. In both cases, as the inner surface field increases, the breakdown voltage also increases, confirming that the inner surface field over the junction independently and effectively controls V_{Br}. This behavior follows the same physical mechanism, where the inner surface field modulates the carrier concentration directly at the p^+/N-well junction, reshaping the local electric field distribution and raising the voltage required to achieve the avalanche condition[31].

Overall, the results from both surface field variations consistently demonstrate that the applied surface fields at the inner and outer gates modulate the breakdown voltage of the implemented SPAD device. Increasing either surface field leads to a rise in V_{Br}. When one surface field is fixed at a higher bias voltage, it effectively shifts the starting point of the sweep range for the other gate. This dual-gate tunability, together with the outer surface field's ability to suppress carrier migration toward the oxide interface, confirms the advantage of the multiple-surface-field configuration in achieving more controllable modulation of the breakdown voltage compared to a single-surface-field design.

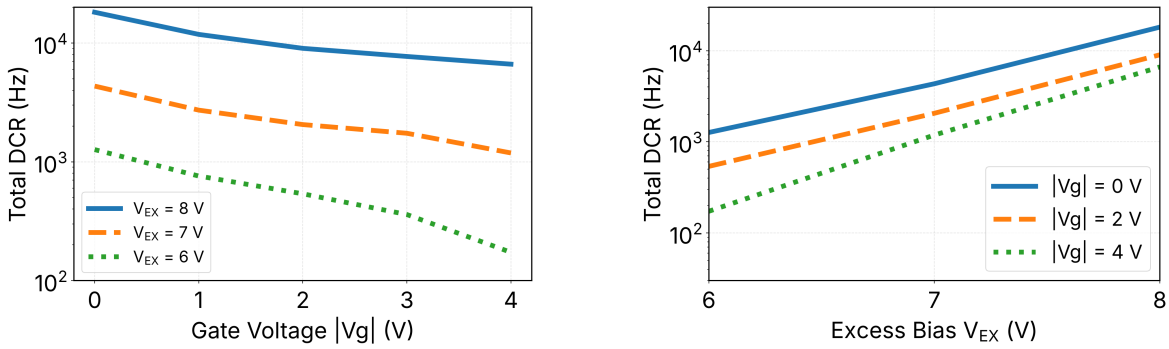
5 Investigation of the Impact of Surface Field on Noise Performance for SPAD Device

Since the breakdown voltage is a critical parameter influencing SPAD performance, the applied surface field provides a promising approach for tuning and enhancing device characteristics. To evaluate this potential improvement, we investigate the effect of the surface field on SPAD's noise performance as a representative example in this section. The dark count rate (DCR) is the effective noise of the SPAD devices. In the absence of photons, free carriers are generated within the device by thermal processes, inter-band (band-to-band) tunneling, and diffusion. Since the diffusion current is typically two to three orders of magnitude smaller than the other two processes, it is neglected here[51,54,67]. Each generated carrier has a finite probability of initiating a self-sustaining avalanche, and the DCR is therefore determined by the total carrier generation rate (CGR) and the avalanche triggering probability[51,54].

Using the Shockley–Read–Hall formulation and assuming that the carrier concentrations in the space-charge region are much lower than the intrinsic concentration, the net thermal generation rate of thermally generated carriers is[25,32]

$$G \approx \frac{n_i v_{th} \sigma_i N_t}{2} \tag{10}$$

where n_i is the intrinsic carrier concentration, v_{th} is the thermal velocity, σ_i is the capture cross section, and N_t is the density of generation–recombination centers.



(a) (b)

Figure 18. Simulated total DCR of the SPAD with a single surface field (a) as a function of the applied surface field, $|Vg|$, for different excess bias, V_{EX}, demonstrating the DCR improvement with increasing $|Vg|$, and (b) as a function of V_{EX} for different $|Vg|$, showing increase of DCR with V_{EX} at a fixed $|Vg|$ while decreases with increasing $|Vg|$ at a fixed V_{EX}.

For a device with an active area A_{Active} and a depletion layer thickness W_D, the thermal carrier generation rate is[25,32]

$$CGR_{Thermal} = G \times A_{Active} \times W_D \tag{11}$$

In band-to-band tunneling, carriers are generated by valence-band electrons tunneling through the potential barrier into the conduction band[68–70]. The corresponding carrier generation rate is[25,51]

$$CGR_{BTBT} = \frac{\sqrt{2m^*}\, q^2 F V_R}{h^2 \sqrt{E_g}} \exp\left(-\frac{8\pi\sqrt{2m^*}\, E_g^{3/2}}{3qFh}\right) A_{Active} \tag{12}$$

where m^* is the tunneling effective mass ($0.33\,m_0$, m_0 is effective mass)[70], q is the electron charge, V_R is the reverse bias voltage, h is Planck's constant, E_g is the silicon bandgap energy, and F is the mean electric field in the depletion region. In a SPAD with a surface field, F is modulated by the applied gate bias and, following the linear surface-field dependence established for planar p-n junctions[25,26], decreases linearly with $|Vg|$:

$$F = \kappa |Vg| + F_0 \tag{13}$$

where κ (< 0) and F_0 are constants determined from device simulation. The probability that a single generated carrier initiates an avalanche is[25,54,55,71]

$$P_{Av} = \begin{cases} 0, & V_{EX} < 0 \\ 1 - \exp\left(-\dfrac{V_{EX}}{\eta_T V_{Br}}\right), & V_{EX} \geq 0 \end{cases} \tag{14}$$

where η_T is an experimentally derived parameter and the excess bias is the excess voltage applied beyond the breakdown voltage, $V_{EX} = V_R - V_{Br}$. The total DCR is then[51,54]

$$DCR = P_{Av} \times (CGR_{Thermal} + CGR_{BTBT}) \tag{15}$$

Eqs. (10)–(15) show that the surface field affects the two noise components differently. The thermal carrier generation rate in Eq. (11) depends on n_i and its properties, so it depends primarily on temperature and is essentially independent of the gate bias. In contrast, CGR_{BTBT} depends on the electric field F, which is directly affected by the surface field through Eq. (13). The surface field therefore reduces the DCR through two routes: the suppression of band-to-band tunneling carrier generation and the reduction of the avalanche triggering probability, both of which originate from its modulation of the electric field and the breakdown voltage by the applied surface field.

Fig. 18 shows the simulated total DCR as a function of $|Vg|$ for V_{EX} of 6 V, 7 V, and 8 V (Fig. 18a) and as a function of V_{EX} for $|Vg|$ of 0 V, 2 V, and 4 V (Fig. 18b). For all bias conditions, the DCR decreases with increasing $|Vg|$. As $|Vg|$ increases from 0 V to 4 V, the DCR decreases from approximately 1.27×10^3 Hz to 1.73×10^2 Hz at V_{EX} of 6 V, and also decreases similarly

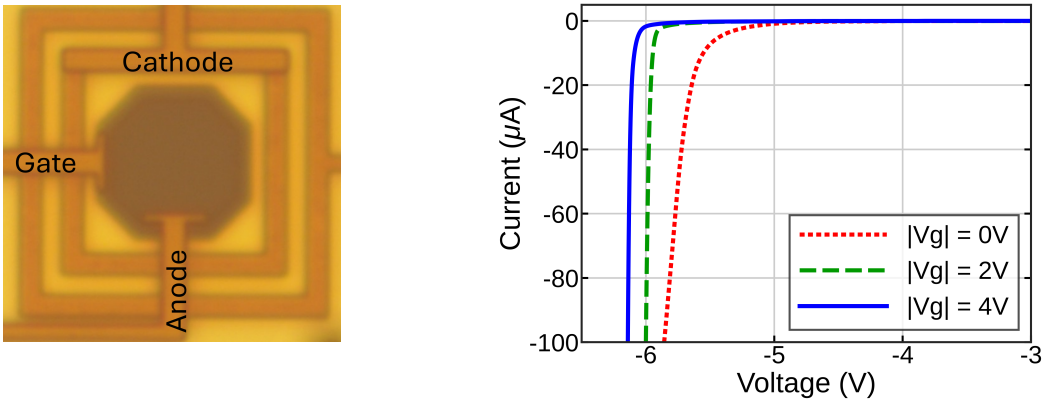


Figure 19. (a) Photomicrograph of the fabricated octagonal-shaped SPAD device with a single surface field implemented in a standard 180 nm CMOS process. (b) Measured reverse current–voltage characteristics of the fabricated SPAD varying the applied surface-field magnitudes, $|Vg|$, from 0 V, to 4 V, illustrating the gate-controlled modulation of the breakdown voltage.

with other V_{EX} of 7 V, and 8 V. Conversely, for every $|Vg|$, the DCR increases with V_{EX}, because a higher reverse bias increases both F, and therefore CGR_{BTBT}, and P_{Av}, as expected. Nevertheless, a higher $|Vg|$ yields a lower DCR at every V_{EX} considered, confirming that the surface field consistently improves the noise performance across the full operating range. Consequently, for a target DCR, the surface field allows the SPAD to operate at a higher V_{EX}, and thus with a higher photon detection probability.

These results agree with the previously reported observation that the gate bias suppresses the DCR primarily through band-to-band tunneling, while the thermally generated DCR depends on the temperature[25]. Together, the results presented in Figs. 18a and 18b confirm that the surface field directly controls the noise performance of the SPAD devices by modulating the electric field and the breakdown voltage. The observed DCR reduction verifies the noise performance improvement by the applied surface field. Therefore, surface field offers an effective and tunable approach to enhancing the noise performance of SPADs fabricated in standard CMOS technologies.

6 Experimental Results of Fabricated SPAD Devices with Surface Fields and Discussion

In order to investigate the impact of surface fields on the breakdown voltage of a real SPAD device and validate the developed TCAD model, we have fabricated two types of SPAD devices with surface fields, single and multiple surface fields, implemented in a standard 180 nm CMOS process. To the best of our knowledge, this work presents the first comprehensive investigation of single-photon avalanche diodes (SPADs) incorporating multiple surface fields, encompassing their design, modeling, fabrication, and experimental characterization. The first fabricated device type is an octagonal-shaped p^+/N-well junction SPAD shown in Fig. 19a, incorporating a single-surface field applied over the junction via a polysilicon gate. The second device is a double-gated p^+/N-well junction SPAD shown in Fig. 20a, representing the first prototype of a SPAD with multiple surface fields applied over the junction (inner gate) and the N-well diffusion region (outer gate).

The measured I–V characteristics presented in Fig. 19b show the current–voltage relationship for the fabricated SPAD device with a single surface field varying the $|Vg|$ from 0 V to 4 V. As the gate voltage increases, the breakdown voltage also increases, confirming that the applied surface field modulates the V_{Br}. This trend is consistent with the simulation results presented earlier in Section 3. The results also show that for 4 V increase in $|Vg|$, the measured breakdown voltage increases by approximately 1 V. Thus, the device performance can be tuned by adjusting the gate bias, which modulates the breakdown voltage and consequently influences the noise, sensitivity, and dynamic range.

The measured I–V characteristics presented in Fig. 20 show the current–voltage relationship for the fabricated SPAD device with multiple surface fields, where each surface field is biased independently while the other gate is kept at 0 V. As shown in Fig. 20b, as the inner gate voltage $|Vg\ in|$ increases from 0 V to 4 V, the breakdown voltage increases by approximately 1 V. Similarly, as shown in Fig. 20c, as the outer gate voltage $|Vg\ out|$ increases from 0 V to 4 V, the breakdown voltage increases by approximately 1 V. These results confirm that both the inner and outer surface fields independently modulate the breakdown voltage of the SPAD device. This trend is consistent with the simulation results of the SPAD device with multiple surface fields presented earlier in Section 4.

The I–V characteristics obtained from experimental measurement and simulation results follow a similar trend and are in

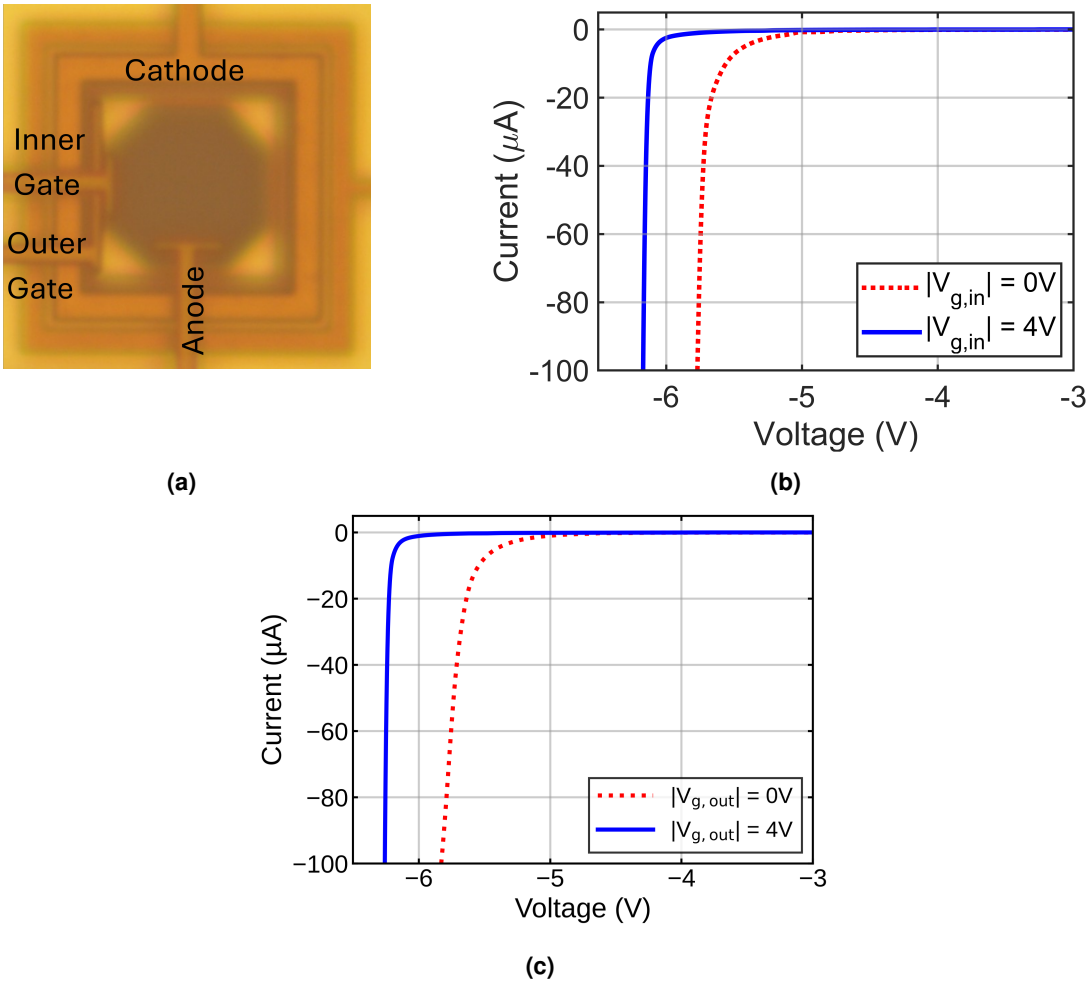


Figure 20. (a) Photomicrograph of the fabricated double-gated SPAD device with multiple surface fields implemented in a standard 180 nm CMOS process. Measured reverse current–voltage characteristics of the fabricated double-gated SPAD with (b) the inner gate bias magnitude $|Vg\ in|$ varying from 0 V and 4 V while the outer gate is held at 0 V, and (c) the outer gate bias magnitude $|Vg\ out|$ varying from 0 V and 4 V while the inner gate is held at 0 V, verifying independent breakdown voltage modulation by each gate.

good agreement. However, a quantitative discrepancy is observed between the measured and simulated breakdown voltage values, which is more pronounced for the higher gate voltage. This discrepancy is primarily attributed to the limited availability of process-specific parameters for the commercial 180 nm CMOS technology used in fabrication. Key information, such as detailed doping profiles, oxide characteristics, and implant parameters, is not fully disclosed by the foundry, resulting in unavoidable uncertainties in the calibration of the TCAD model. Therefore, the developed modeling framework is based primarily on parameters extracted from our previously fabricated SPAD device in a 500 nm CMOS process[16,23]. Applying these parameters to the 180 nm CMOS technology introduces additional uncertainty due to differences in process characteristics, device scaling, and fabrication-related effects. Furthermore, the discrepancy may also be attributed to design-level limitations of the initial fabricated prototype, particularly the double-gated SPAD, which was designed to comply with the design rules of a commercial CMOS process and, to the best of our knowledge, was fabricated for the first time in this work. As a continuation of our future work, we will perform comprehensive characterization and testing of this first prototype to identify and diagnose the design level issues to improve the design, fabricate the second prototype design, and perform comprehensive testing. Finally, we will use the parameters extracted from the measured data to refine the TCAD model parameters. The insights gained from this prototype evaluation will directly guide the development of an improved second-prototype design in the future fabrication cycle.

7 Conclusion

A comprehensive modeling, design, fabrication, and characterization of CMOS SPADs incorporating surface fields has been presented to fully examine their impact on the breakdown voltage. The investigation covered both single and multiple surface field configurations of SPAD devices and examined their effects across a wide range of key device parameters, including gate length, oxide thickness, active region, and N-well geometry and doping concentration. To the best of our knowledge, this is the first study to design, model, implement, and evaluate a SPAD device with multiple surface fields to comprehensively investigate their effects. The results verify that the applied surface field modifies the electric-field profile at the junction perimeter, lowering peak electric-field intensity and suppressing the onset of PEB. Across all simulated device configurations, the breakdown voltage exhibited a nearly linear increase as the gate voltage was increased, demonstrating the effectiveness of gate-voltage modulation. While exploring the impact of various device parameters on the SPAD device with surface field, we found that active-region and N-well doping concentrations significantly influence the breakdown voltage, with an increase in doping concentration resulting in a decrease in the depletion width, leading to a lower breakdown voltage. Increased gate oxide thickness and gate length led to a similar decrease in breakdown voltage. Increasing the active region thickness, however, increased breakdown voltage, whereas changes in N-well thickness and active region length had a negligible impact on the breakdown voltage. We further demonstrate that surface-field-controlled modulation of the SPAD breakdown voltage leads to improved noise performance.

For the SPAD device simulation with double surface fields, both the inner and outer surface fields were observed to independently modulate the breakdown voltage, while together providing improved control over charge migration at the oxide surface. Applied surface fields through both gate terminals consistently increase breakdown voltage as the gate voltage magnitude increases, confirming the concept of dual-gate modulation for enhanced and more stable performance. Therefore, by keeping the outer gate voltage constant at a level to prevent charge migration, the inner gate voltage can control both the electric field and the breakdown voltage. Finally, we investigated the impact of surface fields on real SPAD devices incorporating both single and multiple surface fields fabricated in a commercial deep-submicron CMOS process. The measured I–V characteristics confirmed the similar trend of breakdown voltage modulation observed in the simulation, validating the model accuracy. Results of this comprehensive investigation demonstrate the potential of surface fields, including multiple surface-field structures, for controlling the breakdown voltage of CMOS SPADs and ultimately enhancing their overall performance. Future work may explore the on-chip integration of time-to-digital converters (TDCs) with single- and multiple-surface-field SPADs for photon timing and jitter characterization, enabling compact CMOS-based sensing systems.

Data availability

The datasets used and analyzed during the current study are available from the corresponding author upon reasonable request.

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Author contributions statement

Conceptualization, S.H. and M.S.A.S.; methodology, S.H. and M.S.A.S.; investigation, S.H., S.S., and M.S.A.S.; resources, S.H. and M.S.A.S.; data curation, S.H., S.S., and M.S.A.S.; writing—original draft preparation, S.H., S.S., and M.S.A.S.; writing—review and editing, S.H., S.S, and M.S.A.S.; visualization, S.H., S.S., and M.S.A.S.; supervision, M.S.A.S.; project administration, M.S.A.S.; funding acquisition, M.S.A.S. All authors have read and agreed to the published version of the manuscript.

References

1. Cova, S., Ghioni, M., Lotito, A., Rech, I. & Zappa, F. Evolution and prospects for single-photon avalanche diodes and quenching circuits. *J. modern optics* **51**, 1267–1288 (2004).
2. Palubiak, D. P. & Deen, M. J. CMOS SPADs: Design issues and research challenges for detectors, circuits, and arrays. *IEEE J. Sel. Top. Quantum Electron.* **20**, 409–426 (2014).
3. Zappa, F., Tisa, S., Tosi, A. & Cova, S. Principles and features of single-photon avalanche diode arrays. *Sensors Actuators A: Phys.* **140**, 103–112 (2007).

4. Bronzi, D. *et al.* Fast sensing and quenching of CMOS SPADs for minimal afterpulsing effects. *IEEE Photonics Technol. Lett.* **25**, 776–779 (2013).
5. Bronzi, D., Villa, F., Tisa, S., Tosi, A. & Zappa, F. SPAD figures of merit for photon-counting, photon-timing, and imaging applications: a review. *IEEE Sensors J.* **16**, 3–12 (2016).
6. Gisin, N., Ribordy, G., Tittel, W. & Zbinden, H. Quantum cryptography. *Rev. modern physics* **74**, 145 (2002).
7. Nielsen, M. A. & Chuang, I. L. *Quantum computation and quantum information* (Cambridge university press, 2010).
8. Genovese, M. Real applications of quantum imaging. *J. Opt.* **18**, 073002 (2016).
9. Degen, C. L., Reinhard, F. & Cappellaro, P. Quantum sensing. *Rev. modern physics* **89**, 035002 (2017).
10. Becker, W. Fluorescence lifetime imaging–techniques and applications. *J. microscopy* **247**, 119–136 (2012).
11. Buller, G. & Collins, R. Single-photon generation and detection. *Meas. Sci. Technol.* **21**, 012002 (2009).
12. Stoppa, D., Mosconi, D., Pancheri, L. & Gonzo, L. Single-photon avalanche diode CMOS sensor for time-resolved fluorescence measurements. *IEEE Sensors J.* **9**, 1084–1090 (2009).
13. Kulkov, S. *et al.* Characterizing and exploiting cross-talk effect in spad arrays for two-photon interference. In *Quantum Optics and Photon Counting 2025*, vol. 13525, 1352502 (SPIE, 2025).
14. Efe, B. C. *et al.* Characterization of a 3-D stacked CMOS SPAD depth sensor in 45/22-nm technology. *Opt. Express* **34**, 11630–11651 (2026).
15. Dolenec, R. *et al.* SiPM and CMOS SPAD characterization at liquid nitrogen temperatures. *J. Instrumentation* **20**, P06052 (2025).
16. Dandin, M., Akturk, A., Nouri, B., Goldsman, N. & Abshire, P. Characterization of single-photon avalanche diodes in a 0.5 μm standard CMOS process—part 1: Perimeter breakdown suppression. *IEEE Sensors J.* **10**, 1682–1690 (2010).
17. Rochas, A. *et al.* Low-noise silicon avalanche photodiodes fabricated in conventional CMOS technologies. *IEEE Transactions on Electron Devices* **49**, 387–394 (2002).
18. Finkelstein, H., Hsu, M. J. & Esener, S. C. STI-bounded single-photon avalanche diode in a deep-submicrometer CMOS technology. *IEEE Electron Device Lett.* **27**, 887–889 (2006).
19. Dandin, M., Habib, M. H. U., Nouri, B., Abshire, P. & McFarlane, N. Characterization of single-photon avalanche diodes in a 0.5-μm standard CMOS process—part 2: Equivalent circuit model and geiger mode readout. *IEEE Sensors J.* **16**, 3075–3083, DOI: 10.1109/JSEN.2016.2526665 (2016).
20. Habib, M. H. U. & Mcfarlane, N. A tunable dynamic range digital single photon avalanche diode. *IEEE Electron Device Lett.* **38**, 60–63 (2017).
21. Habib, M. & McFarlane, N. Breakdown and optical response of CMOS perimeter gated single-photon avalanche diodes. *Electron. Lett.* **53**, 1323–1325 (2017).
22. Shawkat, M. S. A., Habib, M. H. U., Hasan, M. S., Haque, M. A. & McFarlane, N. Perimeter gated single photon avalanche diodes in sub-micron and deep-submicron CMOS processes. *Int. J. High Speed Electron. Syst.* **27**, 1840018 (2018).
23. Shawkat, M. S. A. & Mcfarlane, N. A digital CMOS silicon photomultiplier using perimeter gated single photon avalanche diodes with asynchronous AER readout. *IEEE Transactions on Circuits Syst. I: Regul. Pap.* **67**, 4818–4828 (2020).
24. Shawkat, M. S. A., Hasan, M. S. & Mcfarlane, N. Modeling and simulation of PGSPAD-based silicon photomultipliers. *IEEE Transactions on Nucl. Sci.* **68**, 279–291 (2021).
25. Shawkat, M. S. A., Habib, M. H. U. & McFarlane, N. An analog CMOS silicon photomultiplier using perimeter-gated single-photon avalanche diodes. *IEEE Transactions on Circuits Syst. I: Regul. Pap.* **65**, 3830–3841 (2018).
26. Grove, A. S., Leistiko, O. & Hooper, W. W. Effect of surface fields on the breakdown voltage of planar silicon pn junctions. *IEEE Transactions on Electron Devices* **14**, 157–162 (1967).
27. Temple, V. A. & Adler, M. S. Calculation of the diffusion curvature related avalanche breakdown in high-voltage planar pn junctions. *IEEE Transactions on Electron Devices* **22**, 910–916 (1975).
28. Dandin, M. & Abshire, P. High signal-to-noise ratio avalanche photodiodes with perimeter field gate and active readout. *IEEE electron device letters* **33**, 570–572 (2012).
29. Hasan, S. & Shawkat, S. A. Physical modeling of perimeter-gated SPADs in standard deep submicron CMOS processes. In *2024 IEEE 17th Dallas Circuits and Systems Conference (DCAS)*, 1–5, DOI: 10.1109/DCAS61159.2024.10539869 (2024).

30. Hasan, S., Mamun, K. M. & Shawkat, M. S. A. Improving performance of single-photon avalanche diodes for quantum photonics application. In *Quantum Information Science, Sensing, and Computation XVII*, vol. 13451, 81–88 (SPIE, 2025).

31. Hasan, S., Nizam, A., McFarlane, N. & Ara Shawkat, M. S. Effect of surface field on breakdown for CMOS single photon avalanche diodes. In *SoutheastCon 2023*, 736–743, DOI: 10.1109/SoutheastCon51012.2023.10115115 (2023).

32. Sze, S. M., Li, Y. & Ng, K. K. *Physics of semiconductor devices* (John Wiley & Sons, 2021).

33. Synopsys, Inc., Mountain View, CA. *Sentaurus Device User Guide* (2015). Ver. K-2015.06.

34. Streetman, B. G., Banerjee, S. *et al. Solid state electronic devices*, vol. 4 (Prentice hall New Jersey, 2000).

35. Moll, J. & Van Overstraeten, R. Charge multiplication in silicon pn junctions. *Solid-State Electron.* **6**, 147–157 (1963).

36. Synopsys, Inc., Mountain View, CA, USA. *Sentaurus Device User Guide* (2013).

37. Bludau, W., Onton, A. & Heinke, W. Temperature dependence of the band gap of silicon. *J. Appl. Phys.* **45**, 1846–1848 (1974).

38. Bennett, H. S. & Wilson, C. L. Statistical comparisons of data on band-gap narrowing in heavily doped silicon: Electrical and optical measurements. *J. applied physics* **55**, 3582–3587 (1984).

39. Klaassen, D., Slotboom, J. & De Graaff, H. Unified apparent bandgap narrowing in n-and p-type silicon. *Solid-State Electron.* **35**, 125–129 (1992).

40. Van Dort, M., Woerlee, P. & Walker, A. A simple model for quantisation effects in heavily-doped silicon MOSFETs at inversion conditions. *Solid-State Electron.* **37**, 411–414 (1994).

41. Neamen, D. A. & Biswas, D. *Semiconductor physics and devices* (McGraw-Hill higher education New York, 2011).

42. Lombardi, C., Manzini, S., Saporito, A. & Vanzi, M. A physically based mobility model for numerical simulation of nonplanar devices. *IEEE Transactions on Comput. Des. Integr. Circuits Syst.* **7**, 1164–1171, DOI: 10.1109/43.9186 (1988).

43. Canali, C., Majni, G., Minder, R. & Ottaviani, G. Electron and hole drift velocity measurements in silicon and their empirical relation to electric field and temperature. *IEEE Transactions on Electron Devices* **22**, 1045–1047, DOI: 10.1109/T-ED.1975.18267 (1975).

44. Caughey, D. M. & Thomas, R. Carrier mobilities in silicon empirically related to doping and field. *Proc. IEEE* **55**, 2192–2193 (1967).

45. Roulston, D. J., Arora, N. D. & Chamberlain, S. G. Modeling and measurement of minority-carrier lifetime versus doping in diffused layers of n+-p silicon diodes. *IEEE Transactions on Electron Devices* **29**, 284–291 (1982).

46. Fossum, J., Mertens, R., Lee, D. & Nijs, J. Carrier recombination and lifetime in highly doped silicon. *Solid-state electronics* **26**, 569–576 (1983).

47. Chynoweth, A. Ionization rates for electrons and holes in silicon. *physical review* **109**, 1537 (1958).

48. Van Overstraeten, R. & De Man, H. Measurement of the ionization rates in diffused silicon pn junctions. *Solid-State Electron.* **13**, 583–608 (1970).

49. McKay, K. G. Avalanche breakdown in silicon. *Phys. Rev.* **94**, 877–884, DOI: 10.1103/PhysRev.94.877 (1954).

50. Goossens, R. J., Beebe, S., Yu, Z. & Dutton, R. W. An automatic biasing scheme for tracing arbitrarily shaped IV curves. *IEEE transactions on computer-aided design integrated circuits systems* **13**, 310–317 (1994).

51. Cheng, Z., Zheng, X., Palubiak, D., Deen, M. J. & Peng, H. A comprehensive and accurate analytical SPAD model for circuit simulation. *IEEE Transactions on Electron Devices* **63**, 1940–1948 (2016).

52. Javitt, M., Savuskan, V., Merhav, T. & Nemirovsky, Y. Revisiting single photon avalanche diode current-voltage modeling and transient characteristics. *J. Appl. Phys.* **115**, 204503 (2014).

53. X-FAB Silicon Foundries. *0.18 Micron Modular RF Enabled CMOS Logic and Analog Technology*, rev. 3.0 edn. (2008).

54. Giustolisi, G., Mita, R. & Palumbo, G. Behavioral modeling of statistical phenomena of single-photon avalanche diodes. *Int. J. circuit theory applications* **40**, 661–679 (2012).

55. Qiuyang, H., Yue, X. & Feifei, Z. An accurate simulation model for single-photon avalanche diodes including important statistical effects. *J. Semicond.* **34**, 104007 (2013).

56. Maes, W., De Meyer, K. & Van Overstraeten, R. Impact ionization in silicon: A review and update. *Solid-State Electron.* **33**, 705–718 (1990).

57. Habib, M. H. U. & McFarlane, N. A perimeter gated single photon avalanche diode based silicon photomultiplier as optical detector. In *2015 IEEE 58th International Midwest Symposium on Circuits and Systems (MWSCAS)*, 1–4, DOI: 10.1109/MWSCAS.2015.7282084 (2015).

58. Habib, M. H. U., Quaiyum, F., Islam, S. K. & McFarlane, N. Optimization of perimeter gated SPADs in a standard CMOS process. In *SENSORS, 2014 IEEE*, 1668–1671, DOI: 10.1109/ICSENS.2014.6985341 (2014).

59. Xu, Y., Xiang, P. & Xie, X. Comprehensive understanding of dark count mechanisms of single-photon avalanche diodes fabricated in deep sub-micron CMOS technologies. *Solid-State Electron.* **129**, 168–174 (2017).

60. X-FAB Silicon Foundries SE. X-FAB. https://www.xfab.com/ (n.d.). Accessed: 2026-05-25.

61. Wuerdig, R., Franco, L., Scroferneker, R., Metzler, C. & Reis, R. Logical and physical synthesis of an hf-riscv core for X-FAB 180 nm technology. *ICCEEg* **1**, 16 (2020).

62. Lima, H. S. d. Fully non-volatile full adder design using memristors (2024). Thesis.

63. Hu, C. *Modern semiconductor devices for integrated circuits* (Prentice Hall, 2010).

64. Lombardo, S. *et al.* Dielectric breakdown mechanisms in gate oxides. *J. applied physics* **98** (2005).

65. Hu, C. PN and metal-semiconductor junctions. *UC, Berkeley, EE Cl. Note* 89–156 (2009).

66. Liu, F. *et al.* Doping engineering for PDP optimization in SPADs implemented in 55-nm BCD process. *IEEE J. Sel. Top. Quantum Electron.* **30**, 1–7 (2024).

67. Kindt, W. J. & van Zeijl, H. W. Modelling and fabrication of Geiger mode avalanche photodiodes. *IEEE Trans. Nucl. Sci.* **45**, 715–719 (1998).

68. Kane, E. O. Zener tunneling in semiconductors. *J. Phys. Chem. Solids* **12**, 181–188 (1960).

69. Hurkx, G. A. M. On the modelling of tunnelling currents in reverse-biased p-n junctions. *Solid-State Electron.* **32**, 665–668 (1989).

70. Fair, R. B. & Wivell, H. W. Zener and avalanche breakdown in as-implanted low-voltage Si n-p junctions. *IEEE Trans. Electron Devices* **23**, 512–518 (1976).

71. Cova, S., Lacaita, A. & Ripamonti, G. Trapping phenomena in avalanche photodiodes on nanosecond scale. *IEEE Electron Device Lett.* **12**, 685–687 (1991).