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Benjamin Hayden
University of Florida
Hsin-Yuan Lin
University of Florida
Abdolah Amirany
University of Florida
Hamed Dalir
hamed.dalir@ufl.edu

University of Florida

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RUBEZH: Ring-Based Unified Binary-Encoding Zero-Tuner Highly Linear Coherent Photonic Digital-to-Analog Converter

Benjamin Hayden[†], Hsin-Yuan Lin[†], Abdolah Amirany[*†], Hamed Dalir [*]

Department of Electrical and Computer Engineering, University of Florida, Gainesville, FL, 32611, USA .

*Corresponding author(s). E-mail(s): a.amirany@ufl.edu; hamed.dalir@ufl.edu;
Contributing authors: benjaminhayden@ufl.edu; hsinyuan.lin@ufl.edu;
[†]These authors contributed equally to this work.

Abstract

This paper presents RUBEZH, a 4-bit coherent photonic digital-to-analog converter (PDAC) designed for silicon-photonic neural-network accelerators. The architecture integrates a $\mathbf{1 \times 4}$ asymmetric multimode-interference (MMI) splitter, four single-bus microring modulators (MRMs), and a $\mathbf{4 \times 1}$ MMI combiner on a $\boldsymbol{270nm}$ silicon rib-waveguide platform. Single-wavelength coherent field superposition generates 16 linearly spaced power levels while remaining compatible with downstream $\boldsymbol{\pi}$-phase encoding for signed optical weights. To eliminate dedicated active phase tuners, this paper introduces an amplitude-phase-aware voltage lookup algorithm that exploits the intrinsic voltage-dependent amplitude and phase responses of the MRMs to determine optimized per-ring drive states. A three-level voltage set of $\boldsymbol{0V}$, $\boldsymbol{1.24V}$, and $\boldsymbol{2V}$ achieves 4-bit linearity with a root mean square error (RMSE) of $\boldsymbol{0.088\ LSB}$ and INL within $\boldsymbol{\pm 0.25\ LSB}$. Non-dominated sorting genetic algorithm II optimization of the MRM doping profile achieves $\boldsymbol{V_\pi . L = 0.39 V \cdot cm}$. Full-system Lumerical INTERCONNECT simulations demonstrate $\boldsymbol{30GHz}$ modulation bandwidth, $\boldsymbol{-2.2dB}$ insertion loss, approximately $\boldsymbol{39.42mW}$ total electrical power, and a compact $\boldsymbol{\sim 4,600 \mu m^2}$ photonic footprint.

Keywords: Coherent Combining, Microring Modulator, Multimode Interference, Photonic Digital-to-Analog Converter, Signed Weight Encoding, Silicon Photonics

1 Introduction

The growing computational demands of deep-learning inference continue to challenge conventional electronic hardware as CMOS scaling slows and the energy cost of matrix operations and data movement increases [1]. Photonic accelerators offer high bandwidth, low latency, and massive parallelism [2, 3]. In particular, photonic matrix-vector multiplication (MVM) exploits optical superposition for weighted accumulation directly in the photonic domain [4–6]. A key interface is the photonic digital-to-analog converter (PDAC), which maps digitally represented values onto optical carriers for subsequent computation [7, 8].

PDAC architectures can be broadly categorized as serial, intensity-summing parallel, and coherent field-superposition approaches. Serial PDACs employ temporal or dispersive encoding but face synchronization, dispersion, and timing-jitter constraints [9]. Intensity-summing parallel PDACs combine contributions from separate optical paths; wavelength-division-multiplexed implementations simplify independent modulation but require wavelength management and suffer from inter-channel crosstalk. In contrast, coherent PDACs combine weighted fields at a common wavelength, allowing both amplitude and phase to contribute to analog-level synthesis [7] and enabling constructive and destructive interference for signed-weight representation.

The principal limitation of coherent PDACs is sensitivity to relative phase. Prior electro-absorption-modulator- and microring-modulator-based implementations therefore employ dedicated thermo-optic or electro-optic phase tuners [10, 11], increasing footprint, static power, calibration burden, and control complexity [12]. Electronic DACs avoid optical phase management but require a subsequent electro-optic conversion stage [13], whereas a PDAC directly generates the required optical states for downstream photonic processing [6].

This paper presents RUBEZH, a 4-bit ring-based unified binary-encoding zero-tuner highly linear coherent PDAC based on silicon microring modulators. RUBEZH eliminates dedicated per-arm phase tuners through an amplitude-phase-aware voltage lookup algorithm that jointly exploits the intrinsic voltage-dependent transmission and phase responses of the MRMs to generate monotonic, uniformly spaced output levels. The MRM junction is optimized using non-dominated sorting genetic algorithm II (NSGA-II), and a multiphysics workflow combining finite-difference time-domain (FDTD), CHARGE, MODE, and INTERCONNECT simulations provides device- and system-level verification.

The remainder of this paper is organized as follows. Section 2 reviews existing PDAC architectures and coherent microring phase-control challenges. Section 3 presents the RUBEZH architecture, component design, simulation methodology, and optimization. Section 4 describes the amplitude-phase-aware voltage lookup and electrical-photonic co-design. Section 5 presents system-level results, fabrication-tolerance analysis, performance comparison, and discussion. Section 6 summarizes the main findings.

2 Background

2.1 Prior Approaches

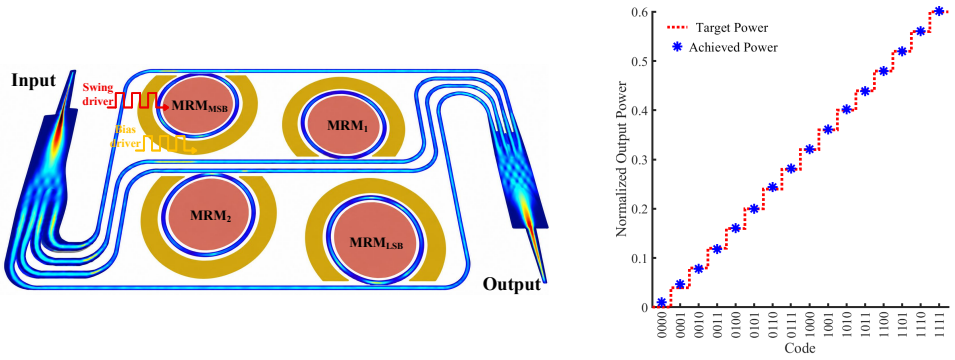
Photonic digital-to-analog converters map digitally represented electrical data into optical-domain states for direct processing in photonic computing systems. Existing PDACs can generally be categorized as serial, parallel intensity-summing, and coherent field-superposition architectures [7]. Serial PDACs generate analog optical levels through temporal or dispersive encoding, offering compact implementations but introducing synchronization, dispersion, and timing-jitter constraints as conversion rate and system parallelism increase [9]. Parallel intensity-summing architectures instead distribute digital contributions among multiple optical paths and combine the resulting optical powers.

In wavelength-division-multiplexed implementations, individual contributions are assigned to separate wavelength channels, simplifying independent modulation while introducing wavelength-management requirements, inter-channel crosstalk, and thermal-alignment overhead. Because these channels are accumulated incoherently, constructive and destructive field interference cannot be directly exploited for signed optical accumulation, introducing additional constraints for photonic matrix-vector multiplication [6]. Coherent PDACs instead combine optical fields at a common wavelength, allowing both amplitude and phase to contribute to analog-level synthesis [7].

2.2 Coherent Conversion and Phase-Control Challenges

Microring modulators are attractive for integrated PDACs because they provide compact electro-optic modulation on silicon-photonic platforms. Coherent field superposition further enables signed optical processing through constructive and destructive interference. Previous coherent PDAC implementations based on electro-absorption modulators and microring modulators have demonstrated the feasibility of this approach [10, 11]. However, coherent operation requires accurate control of the relative phases among parallel optical paths. Propagation-length variation, fabrication-induced dimensional errors, thermal drift, and the intrinsic modulator phase response can perturb the phase presented to the output combiner. Dedicated thermo-optic or electro-optic phase-tuning elements are therefore commonly introduced to restore the required phase relationships, increasing static power, photonic footprint, control complexity, and calibration overhead [12].

The phase-control problem is particularly important for microring modulators because electrical bias simultaneously modifies optical transmission and phase. The voltage-induced resonance shift therefore changes both components of the transmitted field, preventing the MRM from being treated as an ideal amplitude-only element in a coherent converter. Conventional coherent architectures compensate this coupled response using additional phase-control hardware. These limitations motivate a coherent PDAC architecture in which the intrinsic voltage-dependent amplitude and phase responses are considered jointly during digital-to-optical mapping, reducing



(a) (b)

Fig. 1: Proposed RUBEZH 4-bit coherent PDAC architecture. a) Schematic of top-level configuration comprising a 1×4 asymmetric MMI splitter, four independently driven microring modulators, and a 4×1 coherent MMI combiner without dedicated per-arm phase tuners. b) Target and achieved normalized output levels for the 16 digital codes (4-bit operation).

reliance on dedicated per-arm phase tuners while preserving single-wavelength operation and compatibility with signed optical accumulation.

3 Architecture, Component Design, and Optimization

3.1 Architecture and Operating Principle

The RUBEZH architecture employs four parallel optical arms whose complex fields are coherently combined to generate the $2^4 = 16$ output levels required for 4-bit conversion. As illustrated in Fig. 1, the photonic path consists of a 1×4 asymmetric multimode-interference (MMI) splitter, four independently driven single-bus MRMs, and a symmetric 4×1 MMI combiner. Unlike intensity-summing PDACs, the RUBEZH output depends jointly on the amplitude and phase contributions of all four optical fields; therefore, splitter weighting, MRM transmission and phase responses, propagation phases, and combiner characteristics must be considered together.

A continuous-wave carrier at 1550.64nm is applied to the asymmetric MMI splitter, which produces the output power fractions [0.333, 0.271, 0.203, 0.169], including splitter insertion loss. Rather than imposing a conventional binary-weighted 8:4:2:1 distribution, this asymmetric weighting provides additional degrees of freedom for the amplitude-phase-aware voltage-mapping procedure of Section 4. Each splitter output drives an individual MRM, where the reverse-bias voltage simultaneously controls optical transmission and phase. The four modulated fields are then routed to the coherent MMI combiner with the waveguide paths adjusted to establish the nominal combiner-input phase distribution $[0, +\pi/2, +\pi/2, 0]$.

The coherent combination can be described using the linear scattering relation of the output MMI. If the complex field entering arm k is $E_k = A_k e^{j\phi_k}$ and the complex

transfer coefficient from that input to the selected output port is S_{ok}, the output field is

$$E_{\text{out}} = \sum_{k=0}^{3} S_{ok} A_k e^{j\phi_k} \tag{1}$$

The fixed magnitude and phase contributions of S_{ok} can be absorbed into the effective arm amplitudes and phases, respectively. The normalized output-power relation therefore reduces to

$$P_{\text{out}} = \left| A_0 e^{j\phi_0} + A_1 e^{j\phi_1} + A_2 e^{j\phi_2} + A_3 e^{j\phi_3} \right|^2 \tag{2}$$

where A_k includes the splitter weighting, MRM transmission, propagation loss, and fixed combiner transfer magnitude, while ϕ_k contains the splitter-output phase, waveguide propagation phase, voltage-dependent MRM phase shift, and fixed combiner phase. Equation 2 is therefore a compact representation of the complete linear field-superposition process rather than an independent free-space interference approximation; the full-system simulations retain the numerically extracted complex splitter and combiner responses.

Because the MRM phase varies with voltage, binary ON/OFF modulation alone cannot generate uniformly spaced coherent output levels. RUBEZH instead selects discrete per-ring voltage states through the amplitude-phase-aware lookup procedure of Section 4, enabling highly linear binary-encoded 4-bit mapping while eliminating dedicated per-arm active phase tuners. This provides the zero-tuner coherent single-wavelength operation of the architecture.

3.2 Design Flow

The photonic components are designed on a silicon rib-waveguide platform consisting of a 200nm rib above a 70nm slab, giving a total silicon thickness of 270nm with oxide cladding. The overall design methodology follows the sequential workflow illustrated in Algo. 1. The MRM and MMI structures are first characterized independently, after which their complex optical responses are incorporated into the amplitude-phase-aware voltage lookup algorithm. The resulting operating states are then combined with waveguide path-length optimization before final device-level integration and system-level simulation.

A multiphysics simulation workflow is used because the electrical and optical responses of the MRM are strongly coupled. FDTD electromagnetic simulations characterize the passive optical structures and MMI components; CHARGE carrier-transport simulations determine the voltage-dependent carrier distribution and junction electrical characteristics; MODE eigenmode analysis extracts the corresponding changes in effective refractive index, optical loss, and propagation response; and INTERCONNECT circuit-level photonic simulation integrates the extracted component models into the complete PDAC architecture. Python scripting is used to automate parameter sweeps and exchange data among the individual simulation stages.

The optimization sequence consists of five coupled stages. First, the ring geometry and p-n junction are optimized to obtain the required voltage-dependent transmission

Algorithm 1 RUBEZH Design and Simulation Workflow

Require: Silicon rib platform, λ_0
Ensure: Optimized RUBEZH model
1: **MRM optimization**
    Run FDTD/CHARGE/MODE
    Optimize junction using NSGA-II
    Extract $T(V)$ and $\phi(V)$
2: **MMI optimization**
    Sweep 1×4 splitter geometry
    Extract $\{w_k, \phi_k^{\mathrm{MMI}}\}$
    Sweep 4×1 combiner geometry
    Extract complex transfer response
3: **Voltage-state search**
    Interpolate $T(V)$ and $\phi(V)$
    Enumerate candidate voltage states
    Generate monotonic LUT
4: **Phase matching**
    Tune R_2, R_3, and R_4
    Enforce target combiner-input phase
5: **System assembly**
    Build full model in INTERCONNECT
    Evaluate system-level performance
6: **return** Optimized RUBEZH model and LUT

and phase characteristics. Second, the asymmetric 1×4 MMI is optimized to establish the required nonuniform power distribution and associated output phases. Third, these responses are supplied to the amplitude-phase-aware lookup algorithm to identify the discrete MRM voltage states used for the binary-encoded output mapping. Fourth, the 4×1 MMI combiner and waveguide routing are optimized for coherent field collection and the target static combiner-input phase distribution. The resulting component models are then assembled in INTERCONNECT for complete system-level evaluation.

3.3 Microring Modulator Design and Optimization

The microring modulator is designed using the multiphysics workflow described in Section 3.2. The coupling gap and ring radius are first swept to approach critical coupling and maximize the OFF-state extinction ratio. The key optical figures of merit are the loaded quality factor, resonance-wavelength shift, and photon-lifetime-limited modulation bandwidth [14]:

$$Q_L = \frac{\omega_0}{\delta\omega} = \frac{\omega_0 n_g L}{c\,(\alpha_i L + \kappa^2)} \tag{3}$$

$$\Delta\lambda_{\mathrm{res}} = \frac{\lambda_{\mathrm{res}}}{n_g} \Delta n_{\mathrm{eff}} \frac{L_{\mathrm{mod}}}{L} \tag{4}$$

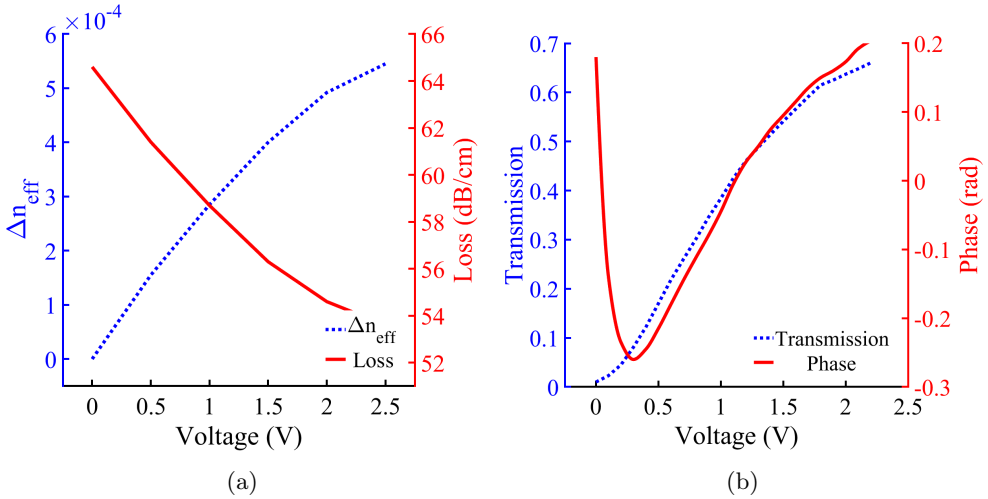


Fig. 2: Voltage-dependent electro-optic response of the optimized microring modulator. a) Effective refractive index change Δn_{eff} and optical loss versus applied reverse-bias voltage. b) Transmission and phase response versus voltage at the operating wavelength of 1550.64nm.

$$f_{\text{ph}} = \frac{1}{2\pi\tau_{\text{ph}}} \approx \frac{c}{\lambda_0 Q_L} \tag{5}$$

Here, ω_0 and λ_{res} denote the resonant angular frequency and wavelength, respectively; $\delta\omega$ is the resonance linewidth; n_g is the group index; L is the ring round-trip length; α_i is the intrinsic propagation-loss coefficient; κ is the bus-to-ring field-coupling coefficient; τ_{ph} is the photon lifetime; and L_{mod} is the electrically modulated portion of the ring. The system operating wavelength λ_0 is distinguished from λ_{res}.

The electro-optic modulation efficiency is characterized through

$$V_\pi L = \frac{\lambda_0}{2}\left[\frac{d(\Delta n_{\text{eff}})}{dV}\right]^{-1} \tag{6}$$

where Δn_{eff} is the voltage-induced variation in effective refractive index. Because the modulated region already occupies a substantial fraction of the ring circumference, further extension of L_{mod} provides diminishing improvement. The junction geometry is therefore optimized primarily to increase the carrier-induced refractive-index variation while limiting optical absorption. The simulated voltage-dependent effective-index variation and optical loss are shown in Fig. 2a, illustrating the electro-optic response and associated loss tradeoff.

To increase the overlap between the depletion region and optical mode, the lateral p-n junction employs three phosphorus and three boron implantation steps distributed through the 270nm silicon rib. The implantation conditions establish the required vertical carrier distribution while limiting excess optical loss. Since the

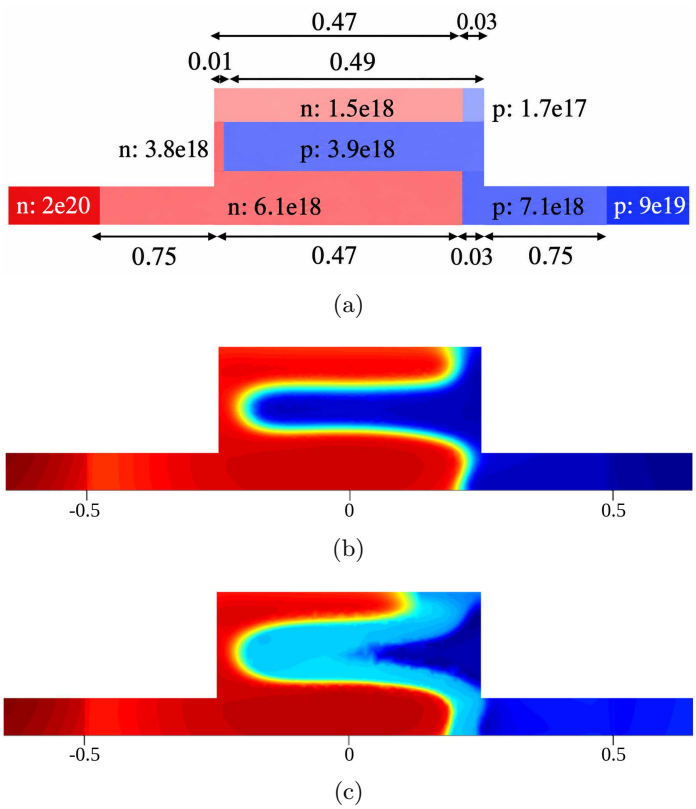


Fig. 3: Cross-section doping profile of the ring modulator p-n junction optimized using NSGA-II. a) Applied boron (p-type) and phosphorus (n-type) doping masks forming the "C"-shaped junction geometry. b) Simulated carrier distribution at 0V bias. c) Simulated carrier distribution at 2.4V reverse bias.

available implantation energies are fixed by the process assumptions, optimization is performed over the doping-mask geometry using NSGA-II [15]. The optimization simultaneously minimizes $V_\pi L$ and doping-induced optical loss. The resulting junction adopts the "C"-shaped profile illustrated in Fig. 3. The optimized junction achieves $V_\pi L \approx 0.39$ V·cm, comparing favorably with the representative junction geometries summarized in Table 1.

The voltage-dependent carrier distributions obtained from CHARGE are transferred to MODE to determine Δn_{eff} and optical loss, thereby producing the transmission and phase responses required by the coherent PDAC model. This link is important because the lookup procedure of Section 4 requires both $T(V)$ and $\phi(V)$ rather than transmission alone. The electrical characteristics of the optimized junction are extracted from the simulated S_{11} response and fitted to an equivalent-circuit model, with the resulting series resistance, junction capacitance, substrate resistance, oxide capacitance, pad capacitance, and series inductance

Table 1: Comparisons of doping profiles for $V_\pi L$

Shape	$V_\pi L$ (V·cm)
Lateral [16]	0.72
Z [17]	0.53
W [18]	0.44
RUBEZH	0.39

Table 2: Ring modulator design parameters, performance, and equivalent circuit model

Parameter	Symbol	Value
Optical and Geometric		
Radius	R	8.1µm
Waveguide width	w	0.5µm
Coupling gap	g	0.192µm
Loaded Q factor	Q_L	6400
Max. transmission	—	0.64 (−1.9 dB)
Min. transmission	—	0.011
Operating wavelength	λ_0	1550.64nm
Operating voltage	$V_{\max}$	2.0V
Electrical (equivalent circuit of the P-N junction)		
Series inductance	L_s	11.77pH
Pad capacitance	C_p	3.34fF
Series resistance	R_s	130.86Ω
Junction capacitance	C_j	10.47fF
Substrate resistance	R_{si}	1308.22Ω
Oxide capacitance	C_{ox}	79.28fF

summarized in Table 2. These parameters define the electrical load presented to the driver architecture and are included in the system-level bandwidth analysis. The final voltage-dependent transmission and phase responses are shown in Fig. 2b and provide the device-level inputs to the amplitude-phase-aware voltage optimization used to realize the binary-encoded, highly linear output mapping without dedicated per-arm phase tuners.

3.4 1×4 Asymmetric MMI Splitter

An asymmetric 1×4 MMI splitter is designed to generate the nonuniform optical weighting required by the coherent PDAC. The design follows the cascaded asymmetric MMI approach in [19], where arbitrary splitting ratios are obtained by breaking the lateral symmetry of the multimode-interference region. Unlike a conventional binary-weighted 8:4:2:1 distribution, the splitting ratio is not prescribed a priori but is selected together with the amplitude-phase-aware voltage mapping to provide sufficient degrees of freedom for linearizing the coherent output levels.

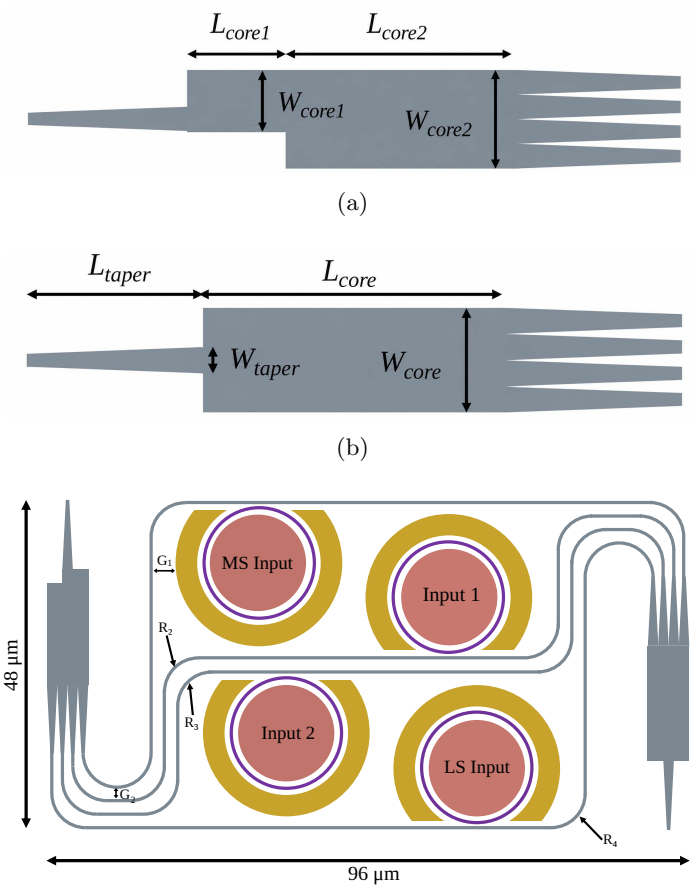


Fig. 4: Photonic layout components of the proposed RUBEZH PDAC. a) Optimized 1×4 asymmetric MMI splitter used to generate the nonuniform arm weights. b) Optimized 4×1 symmetric MMI combiner used for coherent field summation. c) To-scale layout of the complete 4-bit coherent PDAC.

The splitter employs a two-stage core geometry consisting of an inner section with width W_{core1} and length L_{core1}, followed by an outer section with width W_{core2} and length L_{core2}. The taper dimensions are shared with the output MMI structure. An FDTD parameter sweep over the four core dimensions yields the optimized geometry shown in Fig. 4a and summarized in Table 3. The resulting output power fractions are [0.333, 0.271, 0.203, 0.169], including splitter insertion loss. Because the splitter operates coherently, its port-dependent output phases are retained together with the power-splitting ratios. The extracted phases are $[0.4246\pi, -0.0767\pi, -0.0767\pi, 0.4246\pi]$ and are incorporated into the subsequent waveguide phase-matching procedure rather than neglected in the system-level model.

Table 3: Optimized MMI splitter and combiner parameters

Parameter	Symbol	Value
	Splitter	
Inner core length	L_{core1}	2.0µm
Inner core width	W_{core1}	3.8µm
Outer core length	L_{core2}	14.6µm
Outer core width	W_{core2}	6.0µm
Insertion loss	IL	0.11dB
Split ratio	—	[0.333, 0.271, 0.203, 0.169]
	Combiner	
Core length	L_{core}	15.58µm
Core width	W_{core}	6.0µm
Taper length	L_{taper}	10.0µm
Taper width	W_{taper}	1.5µm
Insertion loss	IL	0.15dB

3.5 4×1 Symmetric MMI Combiner

A symmetric 4×1 MMI combiner coherently sums the four modulated optical fields, allowing constructive and destructive interference at the common output according to their relative amplitudes and phases. The optimized combiner layout is shown in Fig. 4b. Its core length L_{core}, core width W_{core}, taper length L_{taper}, and taper width W_{taper} are swept to minimize insertion loss at the operating wavelength. The resulting dimensions and simulated insertion loss are summarized together with the splitter parameters in Table 3.

3.6 Waveguide Layout and Phase Matching

The complete RUBEZH photonic architecture is assembled by cascading the 1×4 asymmetric MMI splitter, four microring modulators, and the 4×1 coherent MMI combiner. The to-scale layout is shown in Fig. 4c. The two MMI devices are oriented perpendicular to the ring array to reduce routing length and overall photonic footprint, with the principal routing dimensions summarized in Table 4.

The 1×4 splitter introduces port-dependent phase offsets that, together with the propagation phase accumulated along each waveguide arm, determine the phase presented to the output combiner. The routing is therefore designed so that the total phases at the four combiner inputs satisfy the target distribution $[0, +\pi/2, +\pi/2, 0]$. This static phase engineering contributes to the zero-tuner operation of RUBEZH by establishing the required nominal phase relationships without dedicated per-arm phase-control elements. Each arm length is expressed in terms of its straight and curved waveguide segments as:

$$L_1 = 106.5 + 4L_{\text{bent}}$$

$$L_2 = \big(86.5 + 2(5 - R_2)\big) + 5L_{\text{bent}} + \frac{\pi R_2}{2}$$

$$L_3 = \big(86.5 + 2(5 - R_3)\big) + 5L_{\text{bent}} + \frac{\pi R_3}{2}$$
$$L_4 = \big(106.5 + 2(5 - R_4)\big) + 3L_{\text{bent}} + \frac{\pi R_4}{2} \tag{7}$$

where $L_{\text{bent}} = \pi(5)/2\mu$m is the arc length of a 90° bend with a reference radius of 5μm, and R_2, R_3, and R_4 denote the adjustable bend radii identified in Fig. 4c. A parametric sweep of R_2, R_3, and R_4 in INTERCONNECT, using the propagation data extracted from MODE, determines the optimized bend radii required to obtain the target combiner-input phase distribution, with the resulting values summarized in Table 4.

4 Amplitude-Phase-Aware Co-Design

4.1 Algorithm Formulation and Input Characterization

Conventional ring modulator drivers operate in a binary ON/OFF fashion, which is well suited to intensity-summing architectures where each arm contributes optical power independently. In the RUBEZH coherent architecture, however, the output depends jointly on the amplitude and phase responses of all four MRMs:

$$P_{\text{out}} = \left| \sum_{k=0}^{N_{\text{arms}}-1} a_k \sqrt{T(V_k)} e^{j[\theta_k + \phi(V_k)]} \right|^2 \tag{8}$$

where $a_k = \sqrt{w_k / \sum_j w_j}$ is the normalized field-amplitude weight derived from the splitter output power fraction w_k, $T(V_k)$ and $\phi(V_k)$ are the voltage-dependent power transmission and phase response of the kth MRM, respectively, and θ_k is the fixed phase contribution of that optical arm. The term θ_k includes the splitter-output phase, static waveguide propagation phase, and fixed output-combiner phase. The routing described in Section 3.6 is optimized so that the nominal static phases at the combiner inputs follow $[0, +\pi/2, +\pi/2, 0]$. Since $\phi(V)$ varies together with $T(V)$, arbitrary binary voltage combinations do not generally produce uniformly spaced or monotonically ordered output levels.

Table 4: RUBEZH PDAC photonic layout geometry

Parameter	Symbol	Value
Overall layout width	—	96µm
Overall layout height	—	48µm
Ring-to-routing clearance	G_1	3.0µm
Parallel waveguide spacing	G_2	1.5µm
Nominal waveguide bend radius	—	5.0µm
Upper inner bend radius	R_2	5.16µm
Lower inner bend radius	R_3	5.15µm
Outer routing bend radius	R_4	4.97µm

The algorithm uses the voltage-dependent $T(V)$ and $\phi(V)$ characteristics shown in Fig. 2b. Both responses are fitted using piecewise cubic Hermite interpolating polynomials (PCHIP) to preserve the simulated trends without interpolation overshoot. The splitter output power fractions are $[w_0, w_1, w_2, w_3] = [0.333, 0.271, 0.203, 0.169]$. Because these values include splitter insertion loss, they are normalized before conversion to field-amplitude weights according to $a_k = \sqrt{\frac{w_k}{\sum_j w_j}}$.

The optimization is parameterized by the number of DAC bits N_{bits}, the number of optical arms N_{arms}, and the number of allowable discrete voltage levels per MRM, K. A common voltage alphabet $\mathcal{V} = \{V^{(0)}, V^{(1)}, \ldots, V^{(K-1)}\}$ is used for all four MRMs in the present implementation; therefore, the complete search space contains $K^{N_{\text{arms}}}$ voltage tuples. Arm-specific voltage alphabets are not required for the 4-bit implementation considered here.

4.2 Voltage-State Optimization

The voltage-state optimization first establishes the available output dynamic range using the binary voltage set $\mathcal{V}_{\text{base}} = \{0, V_{\max}\}$. All $2^{N_{\text{arms}}}$ voltage combinations are evaluated using Eq. 8, and the largest output is taken as $P_{\max}$. The lower target bound is defined as the ideal zero-power reference, $P_{\min} = 0$, rather than as the minimum physically obtained output among the enumerated states. Consequently, finite MRM extinction may produce a nonzero achieved output for the lowest digital code while the corresponding ideal target remains zero. For the three-level implementation considered here, the common voltage alphabet is

$$\mathcal{V} = \{0, V_1, V_{\max}\} \tag{9}$$

where V_1 is optimized over $[0, V_{\max}]$. For each candidate V_1, all $K^{N_{\text{arms}}}$ voltage combinations are evaluated and compared with $2^{N_{\text{bits}}}$ uniformly spaced targets between $P_{\min}$ and $P_{\max}$. The candidate minimizing the staircase RMSE is selected. For $K \geq 4$, multiple intermediate voltage levels are optimized jointly using Differential Evolution [20] instead of the one-dimensional sweep. Once the voltage alphabet is fixed, all $K^{N_{\text{arms}}}$ output states are enumerated.

4.3 Lookup-Table Construction

After the voltage alphabet $\mathcal{V}$ is determined, all $K^{N_{\text{arms}}}$ voltage tuples are evaluated using the amplitude-phase-aware output model. Each tuple $\mathbf{v} = (V_0, V_1, \ldots, V_{N_{\text{arms}}-1})$ produces a coherent output power $P(\mathbf{v})$. The ideal DAC targets are $2^{N_{\text{bits}}}$ uniformly spaced power levels between $P_{\min}$ and $P_{\max}$. The lookup table (LUT) is constructed sequentially from the lowest to the highest digital code. For each target level, the candidate voltage tuple with the smallest absolute power error is selected, subject to the condition that its output power exceeds that selected for the preceding code. This monotonic-selection constraint prevents code reversals that could otherwise occur because different voltage combinations may produce similar output powers under

Algorithm 2 Amplitude-Phase-Aware Voltage Lookup Algorithm

Require: $T(V)$, $\phi(V)$, static phases $\{\theta_k\}$, split weights $\{w_k\}$, $V_{\max}$, N_{bits}, N_{arms}, K
Ensure: $\text{LUT}[c] \to (V_0, V_1, \ldots, V_{N_{\text{arms}}-1})$

$a_k \leftarrow \sqrt{w_k / \sum_j w_j}$ for all k
$\mathcal{P}_{\text{base}} \leftarrow \textsc{EnumeratePowers}(\{0, V_{\max}\}, T, \phi, \theta, \mathbf{a})$
$P_{\min} \leftarrow 0$
$P_{\max} \leftarrow \max(\mathcal{P}_{\text{base}})$
if $K = 3$ **then**
    $V^*_{\text{mid}} \leftarrow \arg\min_{V_{\text{mid}} \in [0, V_{\max}]} \textsc{StaircaseRMSE}(\{0, V_{\text{mid}}, V_{\max}\})$
    $\mathcal{V} \leftarrow \{0, V^*_{\text{mid}}, V_{\max}\}$
else
    Optimize $K-2$ intermediate voltages using Differential Evolution
    $\mathcal{V} \leftarrow \{0, V^{(1)}, \ldots, V^{(K-2)}, V_{\max}\}$
end if
$\mathcal{P} \leftarrow \textsc{EnumeratePowers}(\mathcal{V}, T, \phi, \theta, \mathbf{a})$ ▷ $K^{N_{\text{arms}}}$ states
$\mathbf{p}_{\text{tar}} \leftarrow \textsc{Linspace}(P_{\min}, P_{\max}, 2^{N_{\text{bits}}})$
$P_{\text{prev}} \leftarrow -\infty$
for $c = 0$ **to** $2^{N_{\text{bits}}} - 1$ **do**
    $\text{LUT}[c] \leftarrow \arg\min_{\mathbf{v} \in \mathcal{V}^{N_{\text{arms}}},\, P(\mathbf{v}) > P_{\text{prev}}} |P(\mathbf{v}) - \mathbf{p}_{\text{tar}}[c]|$
    $P_{\text{prev}} \leftarrow P(\text{LUT}[c])$
end for
return LUT

coherent amplitude-phase interference. The resulting mapping is

$$\text{LUT}[c] \to \left(V_0^{(c)}, V_1^{(c)}, \ldots, V_{N_{\text{arms}}-1}^{(c)}\right) \tag{10}$$

where $c \in \{0, \ldots, 2^{N_{\text{bits}}} - 1\}$ denotes the digital input code. At run time, each LUT entry directly specifies the junction-voltage state applied to every MRM, avoiding real-time numerical optimization. Algorithm 2 summarizes the complete amplitude-phase-aware procedure, including voltage-alphabet optimization, enumeration of the $K^{N_{\text{arms}}}$ candidate states, and monotonic LUT construction.

4.4 Electrical Driver Architecture

The amplitude-phase-aware LUT requires three discrete junction-voltage states for each MRM rather than conventional binary ON/OFF operation. These states are generated by two electronic paths per modulator, referred to as the *swing driver* and *bias driver*, implemented in a 28nm CMOS node and interfaced with the photonic chip through 3D heterogeneous integration [21, 22]. The two paths independently control the source and drain potentials of the p-n junction to establish the junction voltage specified by each LUT entry.

Both paths are supplied by an 8×64-bit static random-access memory (SRAM) operating at 469MHz [23, 24]. A six-stage transmission-gate MUX tree serializes the

stored control data to the 30GHz modulator operating rate. In the swing path, a three-stage inverter chain level-shifts the MUX output from 0.8V to 0.9V and then to 1.1V, followed by a two-stack cascode stage providing a 2.0V swing at the MRM junction. The bias path controls the opposite junction terminal from the 0.8V supply. The combined source-drain control realizes the common three-level voltage alphabet required by the LUT without a conventional multibit analog DAC for each MRM arm. Because the delivered MRM voltage is affected by the finite electronic-driver output impedance and junction impedance, the driver is included in the electrical-photonic co-design rather than treated as an ideal voltage source. The frequency-domain voltage transfer from the driver output to the junction is represented by

$$H(f) = \frac{V_{C_j}}{V_{\text{source}}} = \frac{1}{1 + j\omega\tau_1 - \omega^2\tau_2} \tag{11}$$

where

$$\tau_1 = R_{\text{out}}(C_{\text{out}} + C_j) + R_s C_j, \qquad \tau_2 = R_{\text{out}} R_s C_{\text{out}} C_j \tag{12}$$

where R_{out} and C_{out} denote the effective output resistance and capacitance of the electronic driver, respectively, while R_s and C_j are the MRM series resistance and junction capacitance listed in Table 2. This frequency-dependent transfer characteristic is incorporated into the voltage-state optimization so that the LUT uses the effective voltage delivered to the MRM junction rather than the nominal electronic-driver output.

4.5 Scalability to Higher Resolution

The amplitude-phase-aware framework is not restricted to the 4-bit, four-arm implementation considered here. In the general case, the resolution is specified by N_{bits}, while the number of optical arms N_{arms} and available voltage states per MRM, K, determine the number of candidate coherent states. The searchable state space scales as

$$N_{\text{states}} = K^{N_{\text{arms}}} \tag{13}$$

from which $2^{N_{\text{bits}}}$ monotonic states are selected to construct the final LUT. Higher resolution can be supported by increasing the number of optical arms, the number of allowable voltage states per MRM, or both. For $K > 3$, multiple intermediate voltage levels must be optimized jointly using the Differential Evolution procedure described in Section 4.3.

Hardware scaling introduces additional constraints beyond state-space size. Increasing N_{arms} requires a larger $1 \times N_{\text{arms}}$ splitter and $N_{\text{arms}} \times 1$ coherent combiner, additional MRMs and electronic driver channels, and more complex phase-matched routing. For a fixed input optical power, distributing the signal among more arms also reduces the power available to each branch, increasing the importance of splitter, combiner, and waveguide losses and detector signal-to-noise ratio. Increasing K instead preserves the number of optical arms but requires additional accurately controlled voltage states and a larger voltage-state search space. Consequently, higher bit resolution represents a joint optical-electrical design tradeoff rather than a purely algorithmic change. The same amplitude-phase-aware optimization remains

applicable, while the splitter/combiner topology, voltage alphabet, routing, and available optical-power budget must be re-optimized for the selected resolution.

5 Results and Discussion

5.1 Optical Functionality

The complete RUBEZH architecture is evaluated using the cascaded INTERCONNECT model, including the asymmetric MMI splitter, four MRMs, waveguide propagation phases, and coherent output combiner. The simulated optical-field distributions of the optimized 1×4 splitter and 4×1 combiner are shown in Fig. 5a and Fig. 5b, respectively, confirming the intended power distribution and coherent field recombination.

The operating wavelength is selected by jointly considering the voltage-dependent transmission and phase responses of the MRMs. Near the 0V resonance, rapid phase variation produces a large phase difference between the low- and high-voltage states, degrading coherent level synthesis. The operating wavelength of 1550.64nm is therefore selected where the phases associated with the 0V and 2V states approach one another while maintaining sufficient transmission contrast. The resulting full-system spectra for representative digital codes are shown in Fig. 5c.

Applying the amplitude-phase-aware optimization yields the three-level voltage alphabet $\mathcal{V} = \{0, 1.24, 2\}$V. The resulting $3^4 = 81$ candidate combinations are searched to identify the 16 monotonic states required for 4-bit operation. The corresponding LUT and numerical output levels are summarized in Table 5. The achieved levels closely follow the uniformly spaced target staircase, with a normalized RMSE of 0.088 LSB and integral nonlinearity within ± 0.25 LSB across all 16 codes, as shown in Fig. 5d. The finite MRM transmission produces a nonzero output for the lowest code, consistent with the definition $P_{\min} = 0$ used for the ideal target levels.

At this operating wavelength, the end-to-end insertion loss is approximately -2.2dB, while the coherent output phase remains within approximately $\pm 4.5^\circ$ across all 16 codes, as shown in Fig. 5d. This limited code-dependent phase excursion reduces residual phase modulation at the PDAC output and is therefore beneficial for subsequent coherent signed-weight accumulation.

The optical transfer characteristics reported here are normalized to the input optical power. Within the linear optical regime assumed in the simulations, variation of the input power scales all output levels proportionally and therefore does not alter the normalized RMSE, INL, insertion loss, or code-dependent phase response. Consequently, an intrinsic minimum input optical power is not imposed by the PDAC itself; in a complete system, the lower usable power is determined by the responsivity, noise, and required signal-to-noise ratio of the downstream photodetection circuitry.

5.2 Electrical Performance

The electrical bandwidth obtained from the driver-junction transfer function in Eq. 11 is approximately 100GHz, exceeding the photon-lifetime-limited MRM bandwidth of 30GHz. The electrical delivery network therefore does not determine the maximum

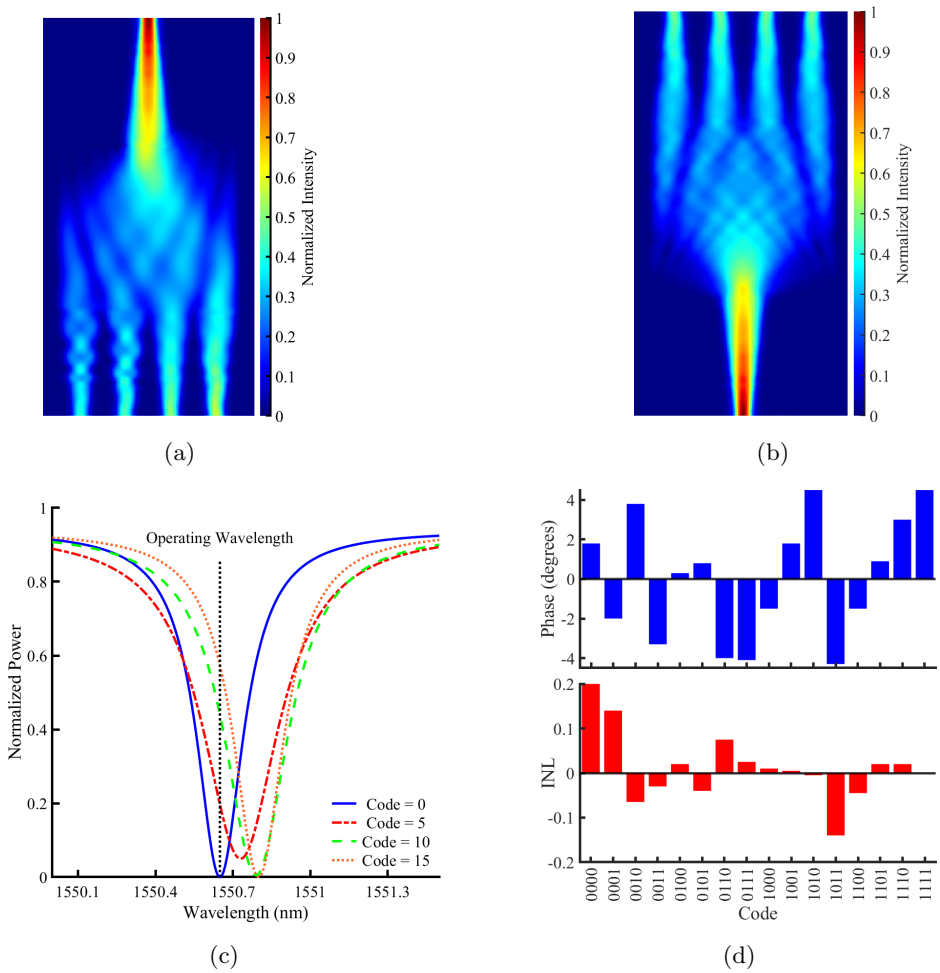


Fig. 5: Optical functionality of the RUBEZH PDAC. a) Simulated optical-field distribution through the optimized 1×4 asymmetric MMI splitter. b) Simulated coherent field combination in the optimized 4×1 symmetric MMI combiner. c) Simulated transmission spectra of the complete PDAC at digital codes 0, 5, 10, 15, with the dashed line indicating the operating wavelength of 1550.64nm. d) Output phase deviation and INL across the 16 digital codes at the operating wavelength.

modulation rate. At 30GHz, the swing-driver and MUX-driven bias paths provide $|H_{\text{amp}}| \approx 0.906$ and $|H_{\text{mux}}| \approx 0.917$, respectively. These values correspond to the effective voltage delivered to the MRM junction and are included in the amplitude-phase-aware optimization rather than assuming an ideal electrical drive.

Because voltage attenuation varies with operating frequency, the available maximum junction voltage changes slightly with data rate. The voltage-state optimization is therefore repeated using the corresponding V_{max} at each operating

Table 5: Simulated 4-bit RUBEZH PDAC output levels and corresponding lookup table at 1550.64nm

Code	Target $\|T\|^2$	Achieved $\|T\|^2$	INL (LSB)	Phase (°)	MSI	In1	In2	LSI
0	0.000	0.009	0.24	1.83	0	0	0	0
1	0.040	0.046	0.16	-2.09	0	0	0	1
2	0.080	0.077	-0.08	3.72	0	2	0	0
3	0.120	0.119	-0.03	-3.41	0	0	1	1
4	0.160	0.161	0.02	0.24	0	1	2	0
5	0.200	0.198	-0.05	0.76	2	1	0	0
6	0.240	0.244	0.09	-4.05	0	1	1	1
7	0.280	0.281	0.03	-4.09	1	1	0	1
8	0.320	0.321	0.01	-1.41	1	1	2	0
9	0.361	0.361	0.01	1.79	2	1	2	0
10	0.401	0.400	-0.01	4.35	2	2	2	0
11	0.441	0.435	-0.14	-4.38	1	1	1	1
12	0.481	0.479	-0.05	-1.46	2	1	1	1
13	0.521	0.522	0.02	0.93	2	2	1	1
14	0.561	0.562	0.03	2.83	2	2	2	1
15	0.601	0.601	0.00	4.47	2	2	2	2

point. As summarized in Table 6, $V_{\max}$ increases from 2V at 30GHz to 2.2V at low frequency, while the optimized intermediate state changes only from 1.24 to 1.28V. The resulting RMSE and insertion loss remain nearly unchanged over the investigated range, and only two LUT entries require modification, indicating that the selected voltage mapping is relatively insensitive to frequency-dependent driver attenuation.

The four swing/bias driver pairs consume 24.80mW at 30GHz. Including the shared differential clock and clock-divider chain, estimated at 5.00mW and 8.46mW, respectively [25, 26], gives a total electrical-driver power of 38.26mW, as summarized in Table 7. Using the three-level junction-voltage alphabet $\{0, 1.24, 2\}$V and the extracted junction capacitance $C_j = 10.47$fF, the average capacitive switching energy is estimated as

$$E_{\text{junc}} = \frac{1}{2} C_j \frac{0^2 + 1.24^2 + 2^2}{3} \approx 9.66 \text{ fJ/bit} \tag{14}$$

For four MRMs operating at 30GHz, this corresponds to approximately 1.16mW of junction-switching power. Including this contribution with the 38.26mW electronic-driver power gives an estimated total electrical power of approximately 39.42mW.

5.3 Fabrication Variability Analysis

Fabrication-induced dimensional and material variations can perturb the amplitude and phase responses required for coherent PDAC operation. Because RUBEZH relies on the relative optical amplitudes and phases of multiple arms, variations in the MMI splitter and combiner, MRM geometry, and waveguide path lengths can alter the optimized output states and degrade linearity. These elements are therefore evaluated individually and at the system level.

Table 6: Speed-dependent RUBEZH operating points

	≤1 GHz	17 GHz	30 GHz
$V_{\max}$ (V)	2.20	2.13	2.00
V_1 (V)	1.28	1.25	1.24
RMSE	0.089	0.091	0.088
IL (dB)	−2.06	−2.12	−2.20
Modified LUT entries			
Code 5	(0,0,2,0)	(1,0,2,0)	(2,1,0,0)
Code 8	(2,0,1,2)	(1,1,2,0)	(1,1,2,0)

Table 7: Electrical power consumption of the RUBEZH driver architecture at 30GHz

Component	Power (mW)	
	Swing Driver	Bias Driver
MUX tree	0.94	1.11
Inverter buffer chain	0.55	—
Cascode output stage	3.28	—
SRAM + registers	0.15	0.15
Subtotal per driver	4.93	1.26
Total per MRM	6.20	
Total for four MRMs	24.80	
Shared differential clock	5.00 [25]	
Shared clock-divider chain	8.46 [26]	
Total electrical-driver power	**38.26**	

Table 8: Fabrication sensitivity of the MMI splitter and combiner

Device	Geometrical Variation (nm)	Max. Ratio Error (%)	IL Variation (dB)
1×4 splitter	Core length (−40 to +60)	±1.1	0.098–0.102
	Core width (±30)	−2.9	0.070–0.122
4×1 combiner	Core length (−40 to +60)	±0.4	0.048–0.052
	Core width (±30)	−1.0	0.045–0.072

The fabrication sensitivity of the passive MMI structures is first evaluated through dimensional sweeps of the splitter and combiner geometries. Core-length biases from −40nm to +60nm and width biases of ±30nm are applied to the optimized structures. The splitter exhibits a maximum split-ratio deviation of approximately ±1.1% for length variation and −2.9% for width variation, while the corresponding combiner deviations remain within approximately ±0.4% and −1.0%, respectively. The associated insertion-loss variation does not exceed 0.122dB over the investigated ranges, as summarized in Table 8. These results indicate that the MMI splitter and combiner are comparatively tolerant to the investigated dimensional variations.

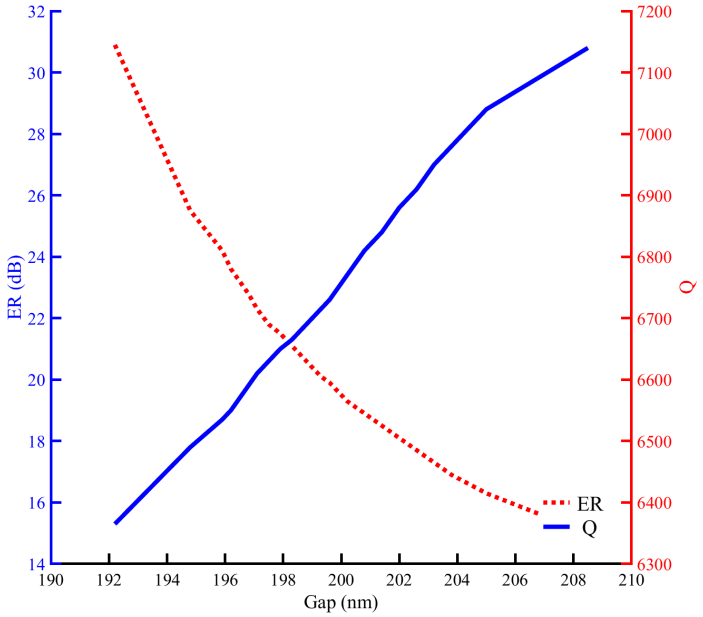


Fig. 6: Sensitivity of the MRM ER and loaded Q factor to coupling-gap variation.

The MRM fabrication sensitivity is evaluated through separate dimensional sweeps of the coupling gap and ring radius. The coupling gap is swept from 192nm to 208nm. As shown in Fig. 6, increasing the coupling gap reduces the extinction ratio while increasing the loaded Q factor, reflecting departure from the optimized coupling condition. The ring radius is independently varied from 8.0985µm to 8.1015µm, over which the resonance-wavelength shift remains approximately 0.149nm with only a small variation. These results indicate that coupling-gap control primarily affects the extinction ratio and loaded Q factor, while ring-radius variation primarily perturbs the resonance wavelength.

The sensitivity of the phase-matched routing network is next evaluated using correlated and independent waveguide path-length perturbations. In the independent model, the tuned arm lengths are perturbed separately by uncorrelated Gaussian variations, whereas the correlated model applies a common path-length shift together with an independent residual component having a standard deviation of 0.25σ. The path-length standard deviation σ is swept from 5nm to 60nm, with 50 Monte Carlo realizations evaluated at each value. Monotonic yield is defined as the percentage of realizations for which all 16 PDAC output levels remain strictly increasing with digital code.

As shown in Fig. 7, both models remain close to the nominal operating point at small σ, while larger independent variations produce greater degradation in RMSE and ENOB. At $\sigma = 60$nm, the independent case reaches approximately 0.25 LSB RMSE and 3.6-bit ENOB, compared with approximately 0.14 LSB and 3.84-bit ENOB for the correlated case. The corresponding monotonic yields are 38% and 68%, respectively.

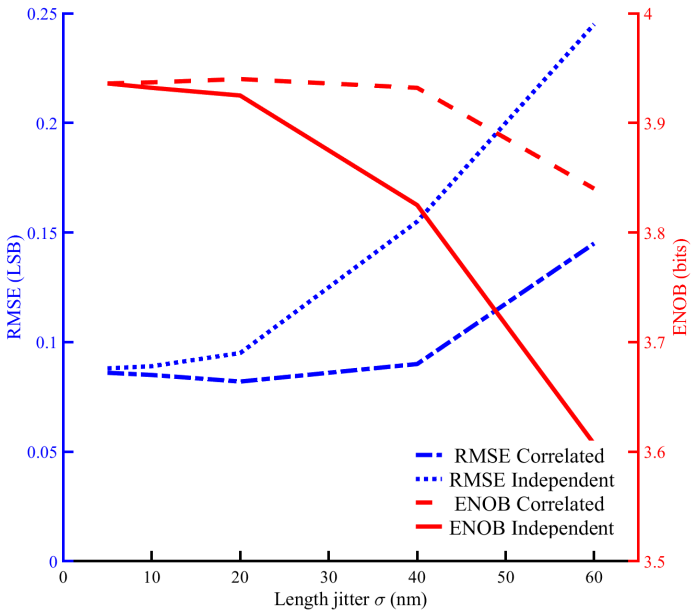


Fig. 7: Effect of correlated and independent waveguide path-length variations on the RMSE and ENOB of the RUBEZH PDAC.

This difference arises because common-mode path-length shifts largely preserve the relative phase relationships among the optical arms, whereas independent variations directly perturb the phase differences required for coherent summation.

Taken together, the variability analyses show that the passive MMI structures are comparatively insensitive to the investigated dimensional variations, whereas MRM geometry and differential waveguide path-length errors are more critical. In particular, independent path-length variations directly perturb the relative phases required for coherent field summation, identifying phase-matched routing and MRM dimensional control as the primary fabrication considerations for RUBEZH.

The amplitude-phase-aware voltage-lookup framework also provides a potential means of accommodating post-fabrication deviations without adding dedicated phase-tuning elements. After fabrication, the optical response can be re-characterized and the voltage alphabet, including the intermediate voltage level(s), re-optimized using the same lookup procedure of Section 4. The resulting candidate voltage combinations can then be re-evaluated to select the monotonic set of $2^{N_{\text{bits}}}$ states that best satisfies the linearity criterion. Because the number of available candidate states exceeds the number of required output levels, the LUT provides additional freedom to compensate for moderate deviations in the MRM, MMI, and relative path responses through electrical state selection. This post-fabrication LUT update can therefore support the zero-tuner architecture without introducing dedicated per-arm phase-tuning elements.

Table 9: Performance summary of the RUBEZH coherent PDAC

Metric	Value
Platform	270nm Si rib waveguide
Electronic integration	3D-stacked 28nm CMOS
Resolution	4 bits (16 levels)
Operating wavelength	1550.64nm
Modulation bandwidth	30GHz
End-to-end insertion loss	-2.2dB
Output dynamic range	18.0dB
INL	< 0.25 LSB
RMSE	0.088 LSB
Output phase variation	$\pm 4.5^\circ$
Ring loaded Q factor	~ 6400
Modulation efficiency ($V_\pi L$)	≈ 0.39V·cm
Avg. junction energy	9.66fJ/bit
Electrical driver power	38.26mW @ 30GHz
Total electrical power	39.42mW @ 30GHz
Photonic footprint	$4.6 \times 10^3 \mu$m^2

5.4 Comparison

Table 9 summarizes the principal simulated performance metrics of the RUBEZH PDAC, including its optical, electrical, and system-level characteristics. The architecture provides 4-bit resolution with 16 monotonic output levels, a 30GHz modulation bandwidth, -2.2dB end-to-end insertion loss, and output phase variation confined to approximately $\pm 4.5^\circ$. The optimized design achieves an RMSE of 0.088 LSB and INL below 0.25 LSB, demonstrating the highly linear mapping of the binary input codes to the optical output levels. The electrical-driver power is 38.26mW at 30GHz, corresponding to an estimated total electrical power of 39.42mW including MRM junction switching, while the photonic footprint is approximately $4.6 \times 10^3 \mu$m^2.

Table 10 compares the RUBEZH PDAC with representative electronic and photonic DAC architectures reported in the literature. Because these implementations target different applications and employ different modulation and signal-combination mechanisms, the comparison focuses on directly reported parameters including resolution, operating speed, reported footprint, insertion loss, wavelength configuration, and power or energy consumption where available.

Among the photonic implementations listed in Table 10, the coherent MRM-based PDAC employing dedicated phase shifters [11] provides the closest architectural comparison to RUBEZH. Both approaches use single-wavelength coherent field combination, whereas RUBEZH incorporates the intrinsic MRM amplitude-phase response directly into the voltage-state selection and therefore removes the dedicated per-arm phase-shifter stage. The resulting LUT maps the binary input codes to monotonic, nearly uniformly spaced optical levels without active per-arm phase tuning, directly combining the binary-encoding, zero-tuner, and highly linear features of the architecture. Together with the -2.2dB end-to-end insertion loss and $4.6 \times 10^3 \mu$m^2

Table 10: Comparison with representative state-of-the-art photonic and electronic DACs.

Architecture	Bits	Speed (Gb/s)	Footprint (μm^2)	IL (dB)	Single-λ?	Energy (fJ/bit)	Application
Electronic CMOS DAC [13]	4	112	6.2×10^2	N/A	N/A	114.0	Processors
Segmented Si MZM [27]	2	140	1.8×10^5	−2.9	Yes	1.2×10^3	Interconnect
Intensity-sum PAM4 [17]	2	200	6.3×10^3	−6.0	No	6.3	Interconnect
Intensity-sum PDAC [28]	4	40	3.0×10^4	−5.5	Yes	42.0	Interconnect
Photocurrent-sum PDAC [7]	4	400	N/R	N/R	Yes	660.0	Communication
Coherent PDAC (EAM) [10]	4	200	1.0×10^6	−4.2	Yes	1.3×10^3	Communication
Coherent PDAC (MRM + PS) [11]	4	50	N/R	−9.0	Yes	N/R	Communication
RUBEZH (MRM, no PS)	**4**	**120**	$\mathbf{4.6 \times 10^3}$	**−2.2**	**Yes**	**9.66**	**Artificial Intelligence Accelerator**

N/A: not applicable; N/R: not reported; IL: insertion loss; PS: phase shifter.

photonic footprint, these characteristics support the intended use of RUBEZH in densely integrated photonic accelerator systems.

6 Conclusion

This paper presented RUBEZH, a 4-bit single-wavelength coherent PDAC based on an asymmetric 1×4 MMI splitter, four silicon MRMs, and a coherent 4×1 MMI combiner. The amplitude-phase-aware voltage lookup method incorporates the intrinsic transmission and phase responses of the MRMs into the voltage-state selection, enabling 16 monotonic output levels without dedicated per-arm phase shifters. Using the three-level voltage set $\{0, 1.24, 2\}$V, the simulated architecture achieves an RMSE of 0.088 LSB and INL within ± 0.25 LSB. Full-system simulations further indicate a 30GHz modulation bandwidth, -2.2dB end-to-end insertion loss, approximately 38.26mW electrical-driver power at 30GHz, and a compact photonic footprint of approximately $4.6 \times 10^3 \mu\text{m}^2$. The fabrication-variability analysis identifies MRM geometry and differential waveguide path-length error as the dominant sensitivities, while the optimized MMI splitter and combiner remain comparatively tolerant over the investigated dimensional ranges. Together, the low insertion loss, compact footprint, single-wavelength operation, and elimination of dedicated per-arm phase shifters support the suitability of RUBEZH for integration in coherent photonic accelerator architectures.

Declarations

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Competing interests

The authors declare no competing interests.

Ethics approval and consent to participate

Not applicable. This study did not involve human participants, human tissue, animals, or personally identifiable information.

Consent for publication

Not applicable. This study does not contain identifiable information from human participants.

Data availability

The datasets generated and analyzed during the current study are available from the corresponding author upon reasonable request.

Materials availability

Not applicable. This study is based on computational modeling and simulation and did not involve the fabrication or use of physical experimental samples.

Code availability

The custom Python scripts and computational routines used for device optimization, voltage-state optimization, lookup-table generation, and data analysis are available from the corresponding author upon reasonable request.

Author contributions

B.H., H-Y.L., and A.A. contributed equally to the conception, methodology, simulation, analysis, and preparation of the manuscript. H.D. supervised the project and contributed to the conceptualization, interpretation of the results, and revision of the manuscript. All authors reviewed and approved the final manuscript.

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