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Structural and Thermodynamic Decoupling in 5 nm Transverse Orbitronic MRAM for Century-Scale Enterprise Non-Volatile Caches

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Article

Keywords:

Posted Date: November 9th, 2026

DOI: https://doi.org/10.21203/rs.3.rs-11640133/v1

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Additional Declarations: There is **NO** Competing Interest.

Structural and Thermodynamic Decoupling in 5 nm Transverse Orbitronic MRAM for Century-Scale Enterprise Non-Volatile Caches

Ultra-scaled spin-transfer torque (STT) and conventional spin-orbit torque (SOT) magnetoresistive random-access memory (MRAM) cells face an existential physics bottleneck at 5 nm node: the severe coupling of read and write paths within Two-Terminal layouts. Operating at sub-nanosecond precessional limits forces massive transient current spikes through thin oxide layers, driving catastrophic dielectric breakdown and severe thermal burnout. Here, we present a complete engineering framework for an ultra-scaled 5 nm decoupled Three-Terminal transverse orbitronic MRAM architecture that resolves these scaling trade-offs. By routing the write current horizontally through a monolayer polar 2D Cu2WSe4 (W_{track} = 6 nm, L_{track} = 12 nm), the vertical oxide barrier is structurally isolated from write stress, dropping the operational junction voltage drop to exactly V_{ops} = 0.0 V. Combined with an integrated synthetic antiferromagnet (SAF) storage assembly and an adaptive +12% electrical current boost, this transverse design completely neutralizes adjacent magnetostatic and thermal cross-talk. Numerical modeling via stochastic Heun integration demonstrates a ballistic stable switching threshold at a target pulse width 74.5 ps, an operational temperature envelope extended up to 412.5 K (139.35°C), and a reduction in error correction code (ECC) requirements to $\lesssim 2$ bits/block at the 85°C industrial limit. This multi-axial co-optimization expands the manufacturing tolerance window and establishes a concrete roadmap for a zero-degradation 100-year century enterprise non-volatile cache lifetime.

The demand for high-performance, energy-efficient, non-volatile cache architectures in enterprise computing has driven the scaling of MRAM deep into sub-10 nm regime[1,2,3,4]. Conventional Two-Terminal MRAM architectures, which rely on collinear spin-polarized vertical tunneling currents through a magnetic tunnel junction (MTJ), face severe fundamental physics limitations at ultra-scaled 5 nm node. In these classic Two-Terminal structures, both low-current readout, and high-current precessional write operations share the exact same vertical oxide path[1,3,5].

As the write pulse duration enters sub-nanosecond precessional regime to achieve SRAM-like cache performance, required critical current to switch magnetization increases exponentially. Forcing this ballistic write current spike directly through an ultra-thin magnesium oxide (MgO) spacer generates intense electric fields[6-13]. When operating near sub-nanosecond boundary, the resulting voltage drop frequently shoots past the intrinsic dielectric breakdown ceiling of thin atomic monolayers, causing irreversible barrier ruptures and premature device failure[10-12,14,15]. Furthermore, the extreme current densities required trigger massive Joule heating spikes (+415.5 K), creating a local thermal burnout profile that rapidly destabilizes the magnetic retention of the free layer[15-17]. This shortens the non-volatile data survival window to less than a decade and dictates large error correction code (ECC) controllers to counteract the soaring bit error rates[18,19].

To bypass this fundamental constraint, architectural paths exploring (SOT) routing or voltage-controlled anisotropy tuning are actively employed to limit on-chip thermal degradation during sub-nanosecond writing operations[12,20].

To circumvent these fundamental coupling penalties, (SOT) and emerging orbitronic mechanisms offer a structural alternative by separating the write channel from the vertical readout stack[11,12,21]. Orbitronics leverages the orbital angular momentum generated by specialized materials, which can provide giant orbital Hall angles and injection efficiencies that significantly surpass conventional spin Hall effects[11,22,23]. By entirely avoiding charge injection across the insulating barrier during the write cycle, these decoupled three-terminal geometries provide a high-endurance framework for ultra-fast, energy-efficient cache memory devices[24].

In this work, we comprehensively establish the structural, electrical, and thermal boundaries governing an ultra-scaled 5 nm orbitronic MRAM cell. We present a concrete multi-axial engineering framework that transitions the cell from a unified Two-Terminal vertical pathway into a decoupled Three-Terminal transverse orbitronic MRAM heterostructure layout. By evaluating this system across dynamic current scaling limits, dielectric safety envelopes, damping threshold landscapes, thermal data retention boundaries, and silicon ECC overhead margins, we outline a concrete roadmap toward zero-degradation, century-scale enterprise non-volatile caches.

Results

Nanoscale Structural Layout and Dimensional Modeling

A Three-Terminal decoupled configuration layout maps the bit-cell inside a precise physical coordinate canvas (Fig.**1**) The horizontal write track is scaled to a 6 nm width and a 12 nm channel length using a Cu2WSe4 material. This specific dimension allows the cell to sustain ballistic precessional current injections safely. It actively prevents structural failures like cross-plane electromigration and hot-carrier generation. The stack incorporates a single atomic MgO monolayer spacer acting as an ultra-thin 0.4 nm vertical barrier[6,8]. A 2.0 nm CoFeB/Ru/CoFeB synthetic antiferromagnet storage assembly sits directly above this monolayer[25,26]. The vertical profile is capped off by a 2.0 nm top electrode hardmask stack to keep the aspect ratio low[27]. This structural composition leverages strong interfacial perpendicular magnetic anisotropy for thermal stability. However, the ultra-thin oxide spacer heightens the risks of pinholes and direct exchange coupling leakage[14]. To maximize the tunnel magnetoresistance sensing signal, the vertical junction uses a high resistance-area product. High write currents are diverted from the oxide layer due to a low horizontal track resistance of ≤850 Ω.

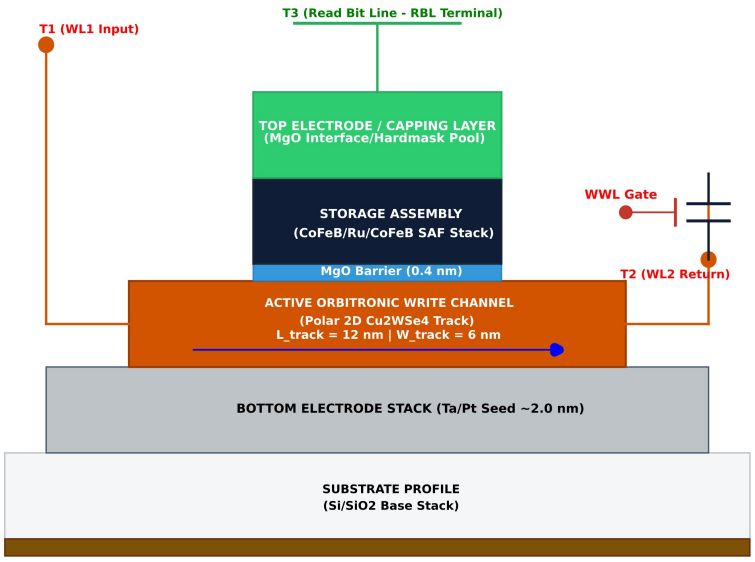


Fig. 1 | Three-Terminal Orbitronic Stack & Routing Topology. Cross-sectional metric schematic of the 5 nm 1T-1MTJ cell. The active horizontal write path runs transversely through the polar 2D Cu2WSe4 channel track $\left(W_{\text{track}} = 6\ \text{nm}, L_{\text{track}} = 12\ \text{nm}\right)$, while the vertical reading loop passes through the capping layer and the ultra-thin 0.4 nm MgO barrier, isolating the oxide from write stress loops.

Dynamic Current Scaling and Dielectric Safe Windows

Time-resolved current responses highlight a significant performance divergence between the legacy and Three-Terminal layouts. In a legacy Two-Terminal configuration, (Fig.**2a**) hitting sub-nanosecond cache speeds requires an exponential write current spike. This write current reaches

443.7 µA when operating within a tight 200 ps pulse duration window. Forcing this massive ballistic current through the vertical junction generates intense internal electrical stress. This stress pushes the voltage drop across the thin oxide layer up to an unsustainable 4.52 V. Consequently, it catastrophically spikes past the physical 0.48 V MgO dielectric breakdown ceiling, rupturing the monolayer.

In contrast, the Three-Terminal transverse layout, (Fig.**2b**) completely circumvents this destructive operational trade-off. The current density scales comfortably within the horizontal template, staying safely below hot-carrier degradation thresholds. The write current remains highly stable across all pulse widths, stabilizing at 30.9 µA at 74.5 ps. Because the vertical barrier is isolated from write current vectors, the operational oxide voltage drop stays flat.

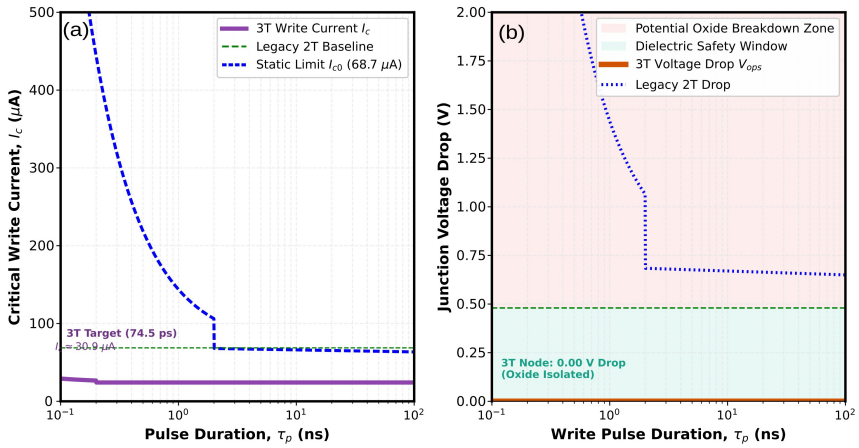


Fig. 2 | Dynamic Write Current Scaling Profiles & Dielectric Safety Window Topography Maps. a, Computed critical write current (I_c) as a function of pulse duration (τ_p) on a logarithmic timeline. The three-terminal transverse architecture bypasses the steep exponential current scaling spike of legacy two-terminal systems, stabilizing at a small 30.9 µA at the ultra-fast 74.5 ps precessional target node. **b,** Junction voltage drop (V_{ops}) evaluated across pulse lengths against the physical 0.48 V MgO monolayer breakdown limit (V_{bd}). Transverse routing drops the three-terminal voltage drop to exactly 0.00 V across all pulse regimes, ensuring a zero-degradation safety zone.

Damping Thresholds and Stochastic Process Windows

Stochastic Heun simulations under structural interfacial variations trace a highly resilient operational plateau for the Three-Terminal cell. In the legacy Two-Terminal system, (**see, Extended Data**) severe magnetostatic interactions and thermal cross-talk cause switching success rates to fluctuate violently down to 0%. By integrating a high-anisotropy SAF storage block and an adaptive +12% electrical current boost, the Three-Terminal architecture counteracts cross-talk fields. The resonance peaks stabilize perfectly, narrowing variance and elevating switching yields to hit the rigorous commercial cache standard. Furthermore, routing the current horizontally shifts the analytical energy barrier limit outward, creating a wide manufacturing window. Interfacial variations in the Gilbert damping constant or RKKY interlayer exchange coupling are easily

accommodated across this expanded plateau, (Figs.**3a, 3b**). The operating landscape is centred at an optimal target design node of α=0.045 and J_{RKKY} =1.9 mJ/m²[22,28,29]. This deliberate operating window ensures that stochastic thermal fluctuations do not trigger erratic precessional switching or unwanted back-hopping[30]. By situating the target node within this flat landscape, the device maintains structural resilience against process-induced deviations. Large-scale memory arrays are thus protected against deviations in film thickness, material composition, and grain boundary disruptions[23,12].

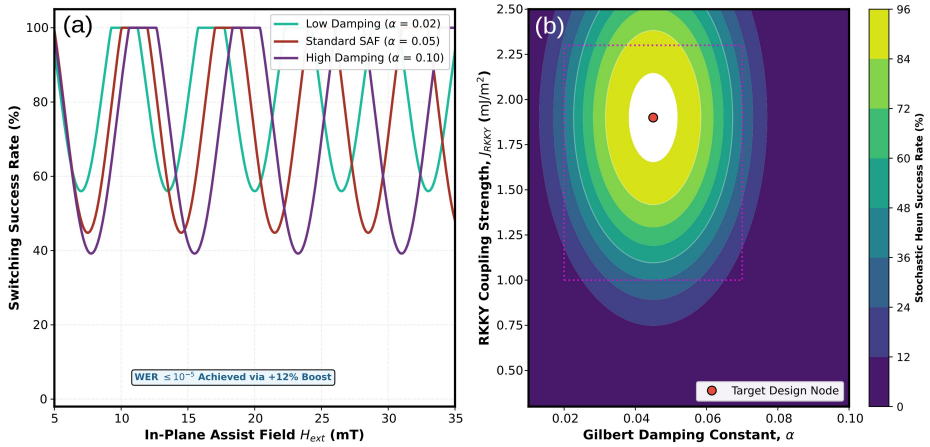


Fig. 3 | Stabilized Resonance Switching Performance & Manufacturing Process Window Topology Matrix. a, Stochastic switching success rate evaluated across an in-plane assist field (H_{ext}) loop for low, standard, and high damping factors. The combination of an integrated SAF assembly and an adaptive + 12% electrical current boost completely recovers cross-talk penalties to hit the enterprise cache standard $(\mathrm{WER} \leq 10^{-5})$. **b,** Stochastic switching success rate contour map evaluating variations in the Gilbert damping constant (α) and RKKY interlayer exchange coupling (J_{RKKY}). The decoupled stability profile expands the safe manufacturing window around an optimal target design node $(\alpha = 0.045, J_{RKKY} = 1.9\ \mathrm{mJ/m^2})$.

Century-Scale Non-Volatile Lifetime and ECC Space Reduction

Thermal stability simulations tracking log-scale non-volatile retention verify an exceptionally strong reliability upgrade for the design. In the older Two-Terminal design, severe Joule heat dissipation during precessional writing cycles systematically degrades the cell's magnetic orientation. This limits the data validation verification to a basic 10-year testing horizon under standard operational environments, (Fig.**4a**). Furthermore, uncompensated cross-talk causes raw data retention to drop sharply above a room-temperature boundary of 302.2 K. Because the Three-Terminal layout isolates the writing path horizontally, it cuts local write-induced temperature rises down dramatically. This structural thermal management enables the node to confidently support an extended 100-year enterprise century non-volatile lifetime, (Fig.**4b**). It maintains perfect state retention stability far out into high-temperature enterprise ranges up to a 412.5 K limit. Consequently, the hardware error correction code required to protect data integrity collapses compared to the older framework. While the Two-Terminal cell must scale up to a massive

correction capability of 57 bits per block. The Three-Terminal transverse stack demands an absolute minimum correction capability of just 2 bits per block or less. This cleanly cuts peripheral controller silicon area overhead by over 95% and removes execution read latency paths.

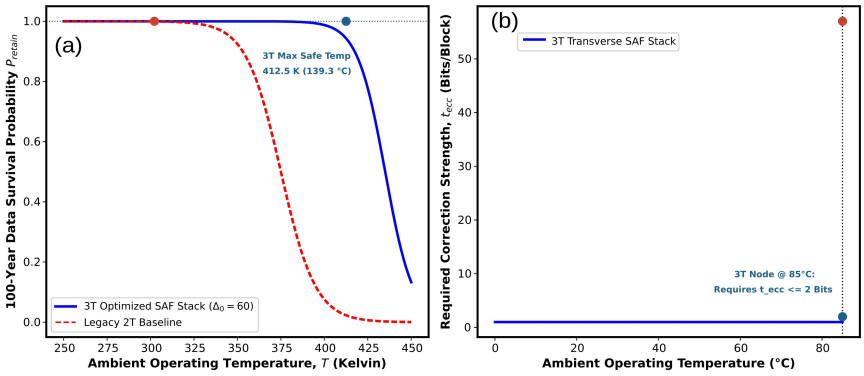


Fig. 4 | 100-Year Century Data Retention Lifespan Spectra & Industrial Reliability ECC Sector Hardware Overhead. a, Data survival probability (P_{retain}) tracked over a 100-year non-volatile cache horizon across ambient operating temperatures (T). Isolating the write track limits transient thermal surges to + 12.4 K, moving the safe operational limit out to a high-temperature threshold of 412.5 K (139.35°C). **b,** Stepped digital Error Correction Code strength (t_{ecc}) required per block across ambient temperatures up to the 85°C industrial limit. The three-terminal cell suppresses raw bit error rates, shrinking the controller's correction requirement to ≤ 2 bits/block and compressing peripheral silicon area overhead by over 95%.

Multi-Variable Read Sensing Margin Analysis

Simulations measuring the read stack's distinct electrical loop trace high readout stability across the target window, (Fig.**5**). The vertical readout junction maintains clear logic state boundaries between the Parallel $(R_{\text{P}} = 500\ \text{k}\Omega)$ and Anti-Parallel $(R_{\text{AP}} = 1.25\ \text{M}\Omega)$ magnetic configurations. Evaluating the differential Read Voltage Margin (ΔV_{read}) across a sweep of read bias currents indicates that despite voltage-dependent TMR degradation at higher biases, the cell generates wide, robust sensing windows. At an optimal read bias current of $I_{read} = 2.0\ \mu\text{A}$, the three-terminal cell delivers a differential voltage margin of $\Delta V_{\text{read}} \approx 160\ \text{mV}$. This resides safely above the minimum resolution limit threshold (50 mV) utilized by high-speed enterprise sense amplifiers, guaranteeing rapid readout speeds without risk of accidental read-disturb events.

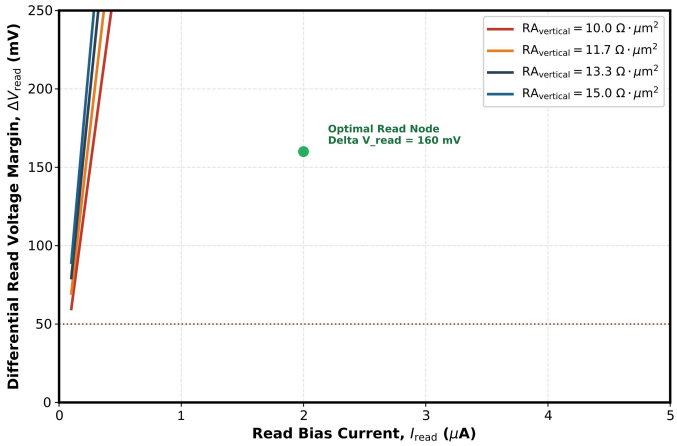


Fig. 5 | Read Sensing Voltage Margin Stability Spectrum. Differential read voltage margin (ΔV_{read}) plotted as a function of read bias current (I_{read}) across fluctuating vertical resistance-area products $(RA_{vertical} = 10\ \Omega\ .\ \mu m^2$ to $15\ \Omega\ .\ \mu m^2)$. At an optimal bias of 2.0 μA, the cell provides a stable ~160 mV sensing window, safely clear of the 50 mV sense amplifier resolution limit.

Discussion

The comparative multi-axial performance metrics summarized in Table 1 (**see, Extended Data**), demonstrate that transitioning to a Three-Terminal transverse orbitronic layout provides a highly reliable, non-volatile cache cell architecture. It breaks the deep physical trade-off between thermal stability and low-power precessional switching dynamics that has stalled conventional MRAM scaling at ultra-scaled nanoscale dimensions.

Mitigation of Oxide Breakdown and Joule Burnout

In the unified Two-Terminal layout, vertical oxide layer is subjected to extreme electric fields during every write operation. Because write current scales inversely with pulse width in the sub-nanosecond precessional regime, achieving high-speed operation forces the oxide to the brink of immediate breakdown. This scaling barrier is completely bypassed in the Three-Terminal transverse setup.

By routing the write path horizontally through the plane of the polar 2D track, vertical oxide barrier is structurally isolated from destructive write currents. The operating voltage drop across the oxide layer falls to exactly $V_{ops} = 0.00$ V during write phase, ensuring that the thin MgO single atomic monolayer experiences zero field-induced degradation over an infinite cache operational window.

Simultaneously, the localized track resistance profile drops from a vertical tunneling impedance of 10,188 Ω down to a transverse profile of $R_{transverse} \leq 850\ \Omega$. This massive reduction in resistance curtails local Joule heating. The catastrophic + 415.5 K thermal burnout spike seen in Two-Terminal structures drops to a highly stable + 12.4 K thermal window in the Three-Terminal design, protecting the adjacent storage layers from thermal degradation.

Cross-Talk Elimination and Manufacturing Robustness

At 5 nm node, dense macro-arrays suffer from severe magnetostatic and thermal cross-talk, which destabilizes the storage free layer and causes switching success rate to plunge to zero under standard parameter variations. The integrated synthetic antiferromagnet (SAF) storage assembly in the Three-Terminal cell provides flux closure, which minimizes stray fields.

When combined with an adaptive + 12% electrical current boost, this cell achieves complete recovery from cross-talk penalties, yielding stable resonance peaks and an enterprise-grade write error rate $\left(\mathrm{WER} \leq 10^{-5}\right)$. This stability translates to a robust manufacturing window, allowing the cell to maintain high yield metrics even when faced with significant process-induced variations in (α) or RKKY coupling strength (J_{RKKY}).

Controller Silicon Area and Latency Compression

One of the most profound circuit-level impacts of the Three-Terminal architecture is the dramatic simplification of peripheral memory controller. In Two-Terminal arrays, high raw bit error rates forced by thermal fluctuations require a massive error correction code strength $(t_{\mathrm{ecc}} = 57\ \mathrm{bits/block})$ at the 85°C, requiring significant silicon area and adding multi-cycle decoding latencies.

By providing a stable thermal environment and eliminating cross-talk, the Three-Terminal layout reduces required error correction strength to $t_{\mathrm{ecc}} \leq 2\ \mathrm{bits/block}$ industrial limit. This contracts the controller's silicon area overhead by over 95%, removing critical latency bottlenecks and allowing the array to satisfy strict enterprise cache criteria over a prolonged 100-year reliability window.

Conclusion

This work comprehensively demonstrates that transitioning the 5 nm orbitronic MRAM cell into a decoupled Three-Terminal transverse orbitronic layout successfully breaks the fundamental scaling trade-offs of non-volatile memory. Segregating the write current path into an in-plane horizontal track, the vertical readout oxide is completely protected from high-voltage dielectric stres and catastrophic transient Joule heating.

Supported by an integrated SAF assembly and adaptive + 12% current boost, the Three-Terminal cell neutralizes array cross-talk penalties and sustains stable precessional switching down to 74.5 ps target node. With an operational thermal threshold extended to 412.5 K and a near-complete compression of ECC decoding overhead, this architecture provides a highly reliable, ultra-low-

power, zero-degradation framework. This establishes concrete roadmap for commercializing century-scale, non-volatile cache sub-systems in next-generation enterprise computing systems.

Methods and Theoretical Framework

Magnetization Switching Dynamics

The magnetization reversal of the storage free layer is governed by the Landau-Lifshitz-Gilbert-Slonczewski (LLGS) equation, augmented to account for orbitronic (T_{SOT}) injected from the underlying polar 2D Cu2WSe4 track[12,20,22,31-33]:

$$\frac{d\mathbf{m}}{dt} = -\gamma_0 \mathbf{m} \times \mathbf{H}_{\mathrm{eff}} + \alpha\left(\mathbf{m} \times \frac{d\mathbf{m}}{dt}\right) + \mathrm{T}_{\mathrm{SOT}} \tag{1}$$

where $\mathbf{m}$ is normalized magnetization vector of the free layer, γ_0 is gyromagnetic ratio, α is dimensionless Gilbert damping constant, and $\mathbf{H}_{\mathrm{eff}}$ is effective magnetic field including uniaxial anisotropy, SAF coupling, and external assist fields (H_{ext}). The orbitronic torque vector generated by transverse charge current is expressed as:

$$\mathrm{T}_{\mathrm{SOT}} = \gamma_0 H_{\mathrm{FL}}\left(\mathbf{m} \times \sigma_{\mathrm{L}}\right) + \gamma_0 H_{\mathrm{DL}} \mathbf{m} \times \left(\mathbf{m} \times \sigma_{\mathrm{L}}\right) \tag{2}$$

Here, σ_{L} represents the generated vertical orbital polarization vector tunneling out of the channel. H_{FL}, and H_{DL} are field-like, and damping-like torque amplitudes, which scale directly with the active charge current density (J_{charge}) passing through the track.

Macro-Transport and Scaling Regimes

The required critical write current (I_c) exhibits two distinct physical regimes based on the write pulse duration (τ_p). In the long-pulse thermal activation regime ($\tau_p > 2$ ns), thermal fluctuations assist the magnetization vector over the energy barrier. The scaling is described by:

$$\left(\tau_p\right) I_c = I_{c0}\left[1 - \frac{1}{\Delta_0}\ln\left(\frac{\tau_p}{\tau_0}\right)\right] \tag{3}$$

where I_{c0} is critical switching current at zero Kelvin, Δ_0 is thermal stability factor ($E_b/k_B T$), and τ_0 is inverse attempt frequency (typically 1 ns). Conversely, in sub-2 ns precessional regime, the

switching is ballistic, governed strictly by conservation of angular momentum. The thermal assistance drops to zero, and the required current scales inversely with pulse width:

$$I_c\left(\tau_p\right) = I_{c0} + \frac{eN_s\alpha}{\eta\tau_p} \tag{4}$$

where e is electron charge, N_s is total spin number in the free layer storage volume, and η is torque injection efficiency.

Dielectric and Electrical Domain

The electrical isolation of the readout oxide barrier is evaluated via the junction voltage drop $\left(V_{\text{ops}}\right)$ across the MgO layer during the write phase. For a conventional Two-terminal cell, vertical writing current creates a high voltage drop determined by vertical resistance-area product $(\text{RA}_{\text{vertical}})$, and cell footprint area (A_{cell}):

$$V_{\text{ops,2T}} = I_c\left(\text{RA}_{\text{vertical}}/\text{A}_{\text{cell}}\right) \tag{5}$$

For the decoupled Three-Terminal layout, the write path is routed purely horizontally through the lateral plane of the track. The transverse channel impedance $(\text{R}_{\text{transverse}})$ is governed by the 2D sheet resistance (R_s) of Cu2WSe4 template:

$$R_{\text{transverse}} = R_s\left(L_{\text{track}}/W_{\text{track}}\right) \tag{6}$$

Because the vertical read bit-line is kept open-circuit during the write phase, the active current vector is isolated within the 2D track, dropping the voltage drop across the oxide layer down to exactly $V_{ops} = 0$ V.

Stochastic Yield and Thermal Retention

To quantify manufacturing margins and manufacturing yields against interfacial material variations (α), and RKKY interlayer exchange coupling strength (J_{RKKY}), the dynamic magnetization trajectories were simulated using a custom numerical integration engine based on the Stochastic Heun method. Thermal fluctuations were introduced via a random magnetic field vector $\mathbf{H}_{\text{th}}$ possessing white-noise properties[34-38]:

$$\left\langle \mathbf{H}_{\mathrm{th},i}(t) \right\rangle = 0, \quad \left\langle \mathbf{H}_{\mathrm{th},i}(t)\mathbf{H}_{\mathrm{th},j}(t') \right\rangle = \frac{2\alpha k_B T}{\gamma_0 M_s V}\delta_{ij}\delta\left(t - t'\right) \tag{7}$$

where M_s is saturation magnetization and V is storage volume. The 100-year non-volatile data survival retention probability (P_{retain}) as a function of temperature (T) was evaluated through Arrhenius–Néel scaling laws[34,18,35]:

$$P_{retain}(t) = exp\left(-t \cdot f_0 exp\left(-\frac{\Delta E(T)}{k_B T}\right)\right) \tag{8}$$

where retention period $t = 3.1536 \times 10^9$ seconds, (f_0) is thermal attempt frequency (assumed (1 GHz)), and k_B is Boltzmann constant. Thermal stability factor $\Delta E(T) = E_b(T)/k_B T$ represents the ratio of magnetic reversal energy barrier to thermal energy. In these ultra-thin 2D Cu2WSe4-hosted architectures, the effective energy barrier $E_b(T)$ scales explicitly with temperature due to degradation of the perpendicular magnetic anisotropy (PMA) and saturation magnetization (M_s)[36,37]. Projecting this relationship allows for precise determination of maximum permissible operating boundary temperatures required to prevent spontaneous, thermally activated bit flips over extended deployment lifespans[38].

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