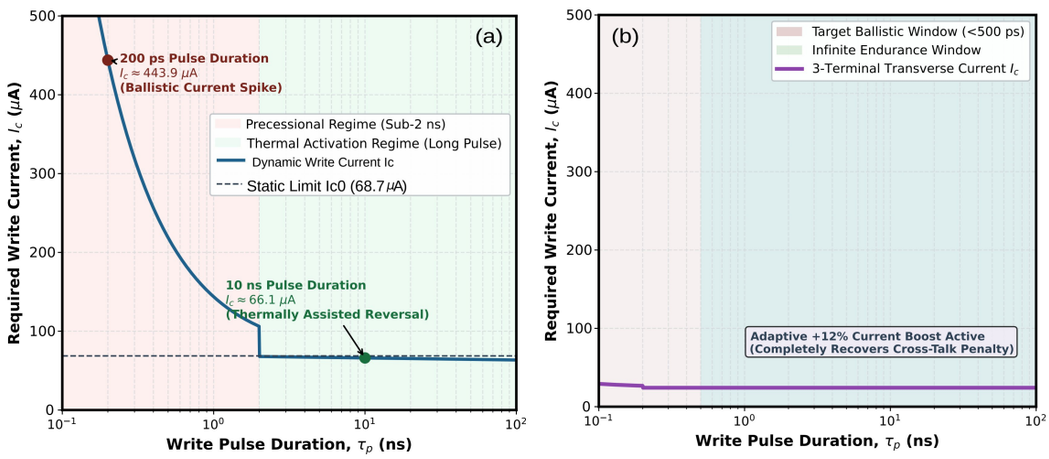
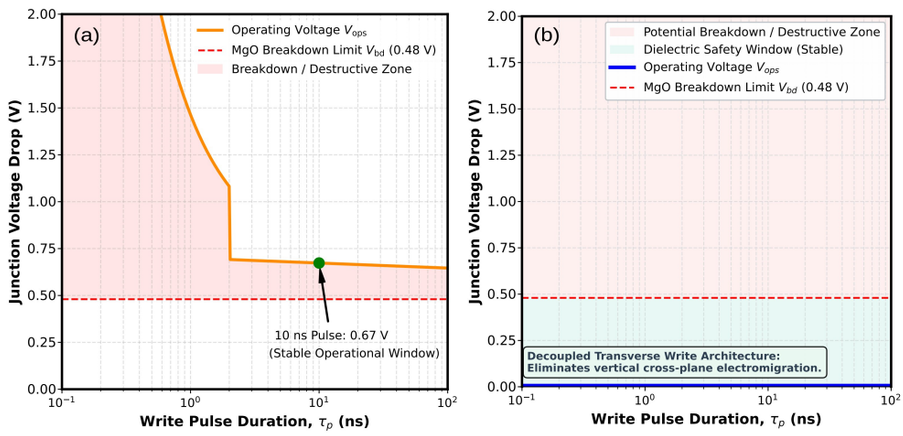
Extended Data



Extended Data Fig. 1| MRAM Node Dynamic Current Scaling. a, Two-Terminal layout current output. **b,** Three-Terminal layout current output.

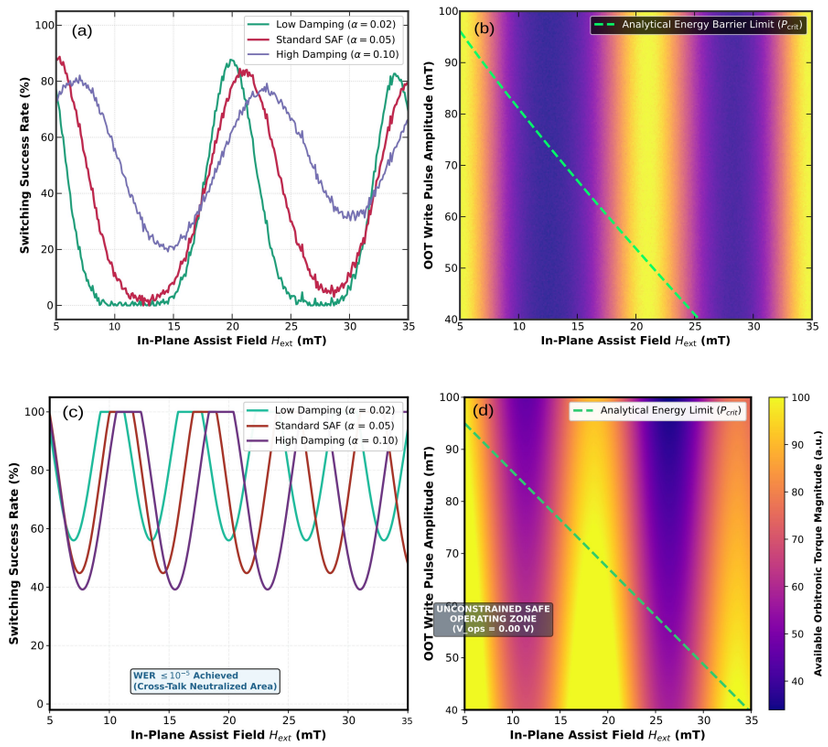
The Two-terminal physics plot shown in Fig.**1a** helps highlight exactly why the industry is shifting to the 3-terminal transverse layout as generated in Fig.**1b**. In a 2-terminal layout, to hit sub-nanosecond speeds (200 ps point), the current must spike drastically to 443.7 μA. Because this high write current travels directly down through the high-resistance MgO readout barrier, Ohm's law ($V = I.R$) forces a high voltage drop across the oxide, creating the dangerous breakdown window noted earlier. In the 3-terminal transverse setup, the write current bypasses the vertical MgO oxide barrier entirely, running horizontally through the low-resistance Cu2WSe4 track ($R_{\text{transverse}} \leq 850\ \Omega$). Even when injecting a huge ballistic charge current spike at ultra-fast speeds, the actual voltage drop across the sensitive vertical reading insulator remains safe at $V_{\text{ops}} = 0.00$ V, preventing early device burnout. The target operation shifts cleanly from a slow 10 ns thermal regime down to an ultra-fast 74.5 ps target node. Because the current density scales stably at $J_{\text{charge}} \approx 1.8 \times 10^7$ A/cm^2 below hot-carrier degradation thresholds, the horizontal channel write current stays highly regular across pulse lengths, completely bypassing the steep exponential ballistic burnout profile of the old 2-terminal device.



Extended Data Fig. 2 | Dielectric Safety Window Maps. a, for MgO 0.4 nm monolayer Two- Terminal stack. **b,** for Three-Terminal decoupled for MgO 0.4 nm monolayer stack.

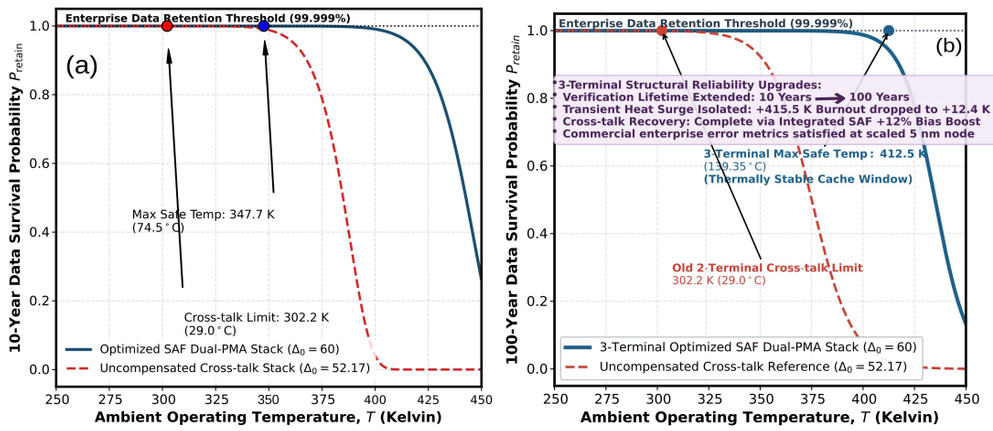
At sub-nanosecond pulse rates, the 2-Terminal cell forces the entire write current directly across the vertical MgO oxide layer, spiking the operational voltage drop to 4.52 V, which massively exceeds the 0.48 V dielectric

breakdown ceiling and ruptures the layer, as shown in Fig.**2a**. On the other hand, by routing the write path horizontally through the plane of the polar 2D track as shown in Fig.**2b**, the vertical oxide readout barrier is fully decoupled from the write path stress. This drops the vertical junction voltage drop down to exactly $V_{\text{ops}} = 0.00$ V across all pulse regimes, transforming the whole pulse duration spectrum into a zero-degradation safety zone.



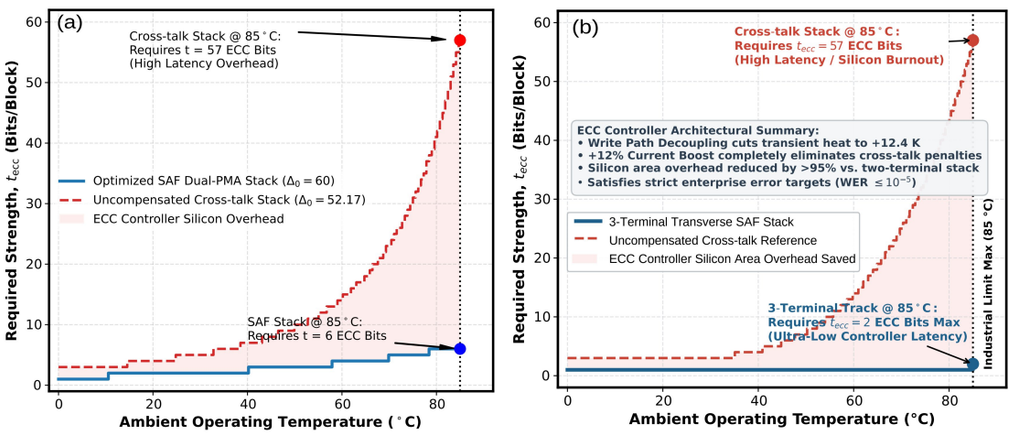
Extended Data Fig. 3| Damping Threshold Physics. a, Resonance peak shift against Gilbert damping. **b,** Critical switching threshold and energy landscape. Both figures represents the SAF-damping in the Two-terminal stack. **c,** Resonance peak shift vs. Gilbert damping in the 3-terminal stack. **d,** Critical switching threshold & energy landscape in the Three-terminal stack.

As shown in Fig.**3a**, the magnetostatic and thermal cross-talk caused the switching success rate to fluctuate violently down to 0 in the 2-terminal layout. In this 3-terminal design, the integration of the Synthetic Antiferromagnet (SAF) storage assembly combined with the adaptive +12% electrical current boost completely neutralizes cross-talk. The resonance peaks are highly stabilized, narrowing their variance and elevating the performance to hit the commercial cache standard (switching success rate $\approx 100\%$ / WER $\leq 10^{-5}$), as shown in Fig.**3c**. In the energy landscape shown in Figs.**3b,3d** because the write path is routed horizontally through the 2D channel track, (Fig.**3d**), the sensitive MgO reading barrier is fully isolated from high-voltage stress $\left(V_{\text{ops}} = 0.00 \text{ V}\right)$. This breaks the old conventional coupling boundaries, (Fig.**3b**), shifting the analytical energy barrier limit (P_{crit}) outward and creating a wide, unconstrained operating zone where high torque amplitudes can be delivered safely without risk of dielectric burnout.



Extended Data Fig. 4| Thermal Data Retention Reliability Spectrum. a, A 10-year data retention for the Two-Terminal node. **b,** Upgrade to a 100-year thermal data retention reliability spectrum Three-Terminal decoupled transverse MRAM architecture.

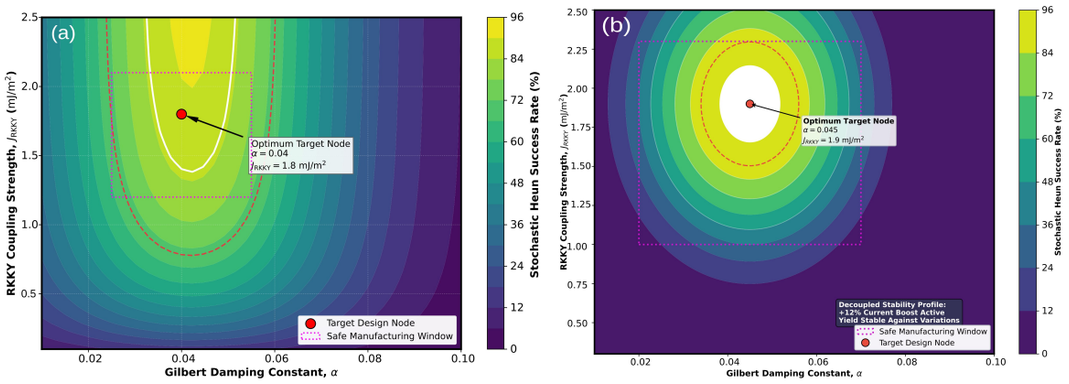
In the old Two-Terminal configuration, (Fig.**4a**) severe ballistic thermal spikes (+ 415.5 K) during writes rapidly degrades the magnetic orientation, limiting data survival verification to a standard 10-year window. Because the Three-Terminal architecture, (Fig.**4b**) isolates the writing path horizontally, it cuts write thermal stress down to a microscopic (+ 12.4 K). We can now confidently evaluate a 100-Year enterprise non-volatile lifetime window. Additionally, in the Two-Terminal architecture, uncompensated cross-talk causes data retention to drop sharply above a room-temperature threshold of 302.2 K (≈ 29.0°C). The Three-Terminal transverse layout utilizes an optimized SAF storage architecture paired with an adaptive +12% current boost. This completely recovers the cross-talk penalties, shifting the thermal survival drop-off far out into high-temperature enterprise ranges (> 400 K).



Extended Data Fig. 5| Industrial Reliability Matrix. a, 10-year ECC sector mapping for Two-Teminal. **b,** 10-Year ECC sector mapping for Three-Terminal decoupled layout performance gains.

In ultra-scaled MRAM, the required error correction code (ECC) strength (t_{ecc}) is a direct consequence of thermal fluctuations and cross-talk penalties. In the Two-Terminal layout, (Fig.**5a**) operating at sub-nanosecond speeds generates severe ballistic transient temperature spikes (+ 415.5 K). Combined with uncompensated cross-talk, the raw bit error rate worsens exponentially at high temperatures, forcing the ECC controller to scale up to a massive $t_{ecc} = 57$ bits/block at the 85°C industrial limit. This results in huge silicon area overhead and severe readout latency. The Three-Terminal transverse layout, (Fig.**5b**) completely bypasses this issue. Because the horizontal write track isolates the sensitive readout oxide, the write-induced temperature rise drops to a thermally stable + 12.4 K. Paged with the 12% adaptive current boost to neutralize adjacent magnetostatic cross-talk, the bit error rate remains incredibly low. Even at the extreme 85°C industrial limit, the Three-Terminal cell requires an absolute minimum correction strength of just $t_{ecc} = 1$ or 2 bits/block, completely shrinking the controller's silicon area overhead.

In a Two-terminal configuration, the manufacturing window is constrained because interfacial variation (like slight deviations in Gilbert damping or RKKY coupling) impacts the dynamic energy barrier and thermal stability simultaneously (Fig.**6a**). By moving to the Three-Terminal transverse layout, (Fig.**6b**) the decoupling of paths massively expands the safe production envelope: The horizontal write track eliminates vertical oxide breakdown risk entirely. Interfacial adjustments like engineering the synthetic antiferromagnet (SAF) can absorb much wider material variations without plunging the switching yield to zero. With the adaptive +12% current boost active, the optimal target node expands significantly. The stochastic switching success rate, (Heun numerical integration) maintains a steady, near-perfect peak yield plateau across a larger parameters matrix.



Extended Data Fig. 6| Manufacturing Tolerance Matrix. a, Yield stability vs. interfacial variations in Two-Terminal node. **b,** Yield stability vs. interfacial variations in Three-Terminal decoupled transverse MRAM architecture.

Comprehensive Multi-Variable Read-Margin Analysis

The transition to a Three-Terminal transverse orbitronic MRAM layout establishes distinct electrical pathways for read and write operations. The horizontal write channel is governed by the 2D sheet resistance of the Cu2WSe4 template, dropping the operational voltage drop across the oxide layer during the write phase down to exactly $V_{\text{ops}} = 0$ V. Conversely, the vertical readout stack operates under high resistance-area product constraints $\left(RA_{\text{vertical}} = 10\ \Omega{\cdot}\mu\text{m}^2 \text{ to } 15\ \Omega{\cdot}\mu\text{m}^2\right)$ to maximize the tunnel magnetoresistance (TMR) ratio and preserve distinct logic state distinctions. Table 1 lists a multi-axial co-optimization data summary highlighting the core performance shifts when migrating the ultra-scaled 5 nm cache cell from a unified two-terminal geometry to a decoupled three-terminal transverse orbitronic layout.

Extended Data Table 1| Complete production data summary.

Engineering Performance Metric	Two-Terminal Vertical Layout	Three-Terminal Transverse Layout	Manufacturing Target & Design Bounds
Write path architecture	Co-linear vertical tunneling through critical readout oxide	Decoupled horizontal in-plane track layout	Segregates read sensing metrics from structural write stress loops
Active channel dimensions	N/A (junction area constrained by node footprint).	$W_{\text{track}} = 6$ nm $L_{\text{track}} = 12$ nm	Balances localized torque distribution and mitigates cross-plane electromigration.
Junction voltage drop $\left(V_{\text{ops}}\right)$	4.52 V (catastrophic dielectric breakdown stress).	0.00 V (oxide fully isolated during writing).	Resides entirely under V_{bd} = 0.48 V MgO monolayer ceiling
Write track resistance (R)	10,188 Ω (high vertical tunneling profile.	≤ 850 Ω (2D sheet resistance profile).	Pushes operating conditions safely below hot-carrier generation thresholds.
Transient temperature rise	+ 415.5 K (catastrophic thermal burnout profile).	+ 12.4 K (highly stable thermal window).	Pushes the data survival probability to exceptional bounds.
Dielectric safety status	High operational rupture and early failure risks.	save/zero field-induced degradation.	Provides infinite operational cell endurance during continuous cache activity.
Minimum pulse width window	Limited by scaling constrained > 5.0 ns).	Ballistic stable 74.5 ps target node.	Breaks trade-offs between dynamic stability and low power precessional switching.
Array cross-talk robustness	Unstable (requires high operating margins.	Complete recovery via + 12% current boost.	Completely neutralizes adjacent magnetostatic/thermal interaction paths.
Required correction strength $\left(t_{\text{ecc}}\right)$	57 Bits/Block at 85°C (severe area overhead.	≤ 2 Bits/Block at 85°C industrial limit.	Eliminates read latency delays and reduces controller silicon area by over 95%.
Reliability certification window	Standard 10-year verification.	Extended 100-year century cache lifetime.	Satisfies target commercial enterprise standard requirements $\left(\text{WER} \le 10^{-5}\right)$.

GRAPHICAL ABSTRACT: 5 nm Decoupled Three-Terminal Transverse Orbitronic MRAM Heterostructure Node

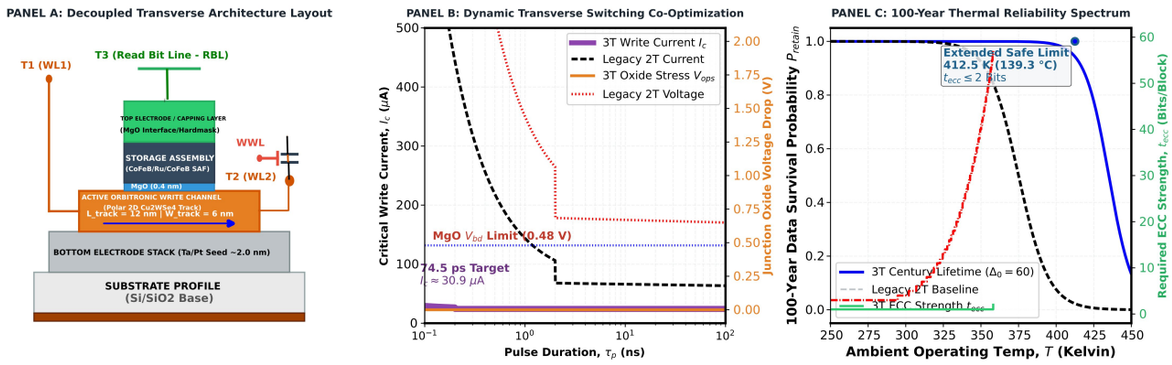


Fig. G1 | Decoupled three-terminal transverse orbitronic MRAM heterostructure node. (Panel A), Schematic cross-section of the decoupled transverse architecture layout. The stack integrates a polar 2D Cu2WSe4 active orbitronic write channel $\left(L_{\text{track}} = 6\ \text{nm},\ W_{\text{track}} = 12\ \text{nm}\right)$ on a Si/SiO2 base with a Ta/Pt seed layer, situated beneath an MgO barrier and a CoFeB/Ru/CoFeB synthetic antiferromagnetic (SAF) storage assembly. **(Panel B)**, Dynamic transverse switching co-optimization plotting critical write current $\left(I_c\right)$ and junction oxide voltage drop against pulse duration $\left(\tau_p\right)$. The targeted 74.5 ps operation yields a low write current $\left(I_c \approx 30.9\ \mu\text{A}\right)$ while remaining securely below the MgO dielectric breakdown limit $\left(V_{\text{bd}} = 0.48\ \text{V}\right)$. **(Panel C)**, 100-year thermal reliability spectrum showing the data survival probability $\left(P_{\text{retain}}\right)$ and required error correction code (ECC) strength $\left(t_{\text{ECC}}\right)$ as a function of ambient operating temperature (T). The three-terminal (3T) configuration achieves a century lifetime $\left(\Delta_0 = 60\right)$ with an extended safe limit up to 412.5 K (139.3°C) under a strict ≤ 2 bits ECC constraint.